1990/1991

POWER PRODUCTS DATA BOOK

Siliconix incorporated

Siliconix incorporated reserves the right to make changes in the circuitry or specifications at any time without notice and assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Warning Regarding Life Support Applications

Siliconix products are not sold for applications in any medical equipment intended for use as a component of any life support system unless a specific written agreement pertaining to such intended use is executed between the manufacturer and Siliconix. Such agreement will require the equipment manufacturer either to contract for additional reliability testing of the Siliconix parts and/or to commit to undertake such testing as a part of its manufacturing process. In addition, such manufacturer must agree to indemnify and hold Siliconix harmless from any claims arising out of the use of the Siliconix parts in life support equipment.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Siliconix incorporated

TABLE OF CONTENTS

Section 4. MOSPOWER Data Sheets (Cont'd)

Siliconix incorporated

Section 5. Power IC Data Sheets

Section 9. Application Notes

Siliconix incorporated

ALPHA-NUMERIC INDEX

Cross Reference

Siliconix Part Number

Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Siliconix Approximate Replacement

Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeablity is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
BSM151F(2)	SPMB50A500	
BSM151F(2)	SPMF50A500	
BSM254F	SPMB50A500	
BUK637-500A	SMW14N50F	
BUK637-500B	SMW14N50F	
BUK655-500A	SMP5N50F	
BUK655-500B	SMP5N50F	
BUK657-500A	SMP8N50F	
BUK657-500B	SMP8N50F	
BUZ11S2	SMP50N06-25	
BUZ210		SMW14N50F
BUZ211		SMW8N50F
BUZ215	SMP5N50F	
BUZ216	SMP5N50F	
BUZ384	SMW14N50F	
BUZ385	SMW14N50F	
EUM099-M221	SPMB50A500	
FBA50AA	SPMF50A500	
FCA50AA	SPMB50A500	
GF8A40	SMW45N10	
IRF9140	SMM20P10	
IRF9141	SMM20P10	
IRF9142	SMM20P10	
IRF9143	SMM20P10	
IRF9240	SMM11P20	
IRF9241	SMM11P20	
IRF9242	SMM11P20	
IRF9243	SMM9P15	
IRF9510	SMP3P10	
IRF9511	SMP3P10	
IRF9512	SMP3P10	
IRF9513	SMP3P06	
IRF9540	SMP20P10	
IRF9541	SMP20P10	
IRF9542	SMP20P10	
IRF9543	SMP20P10	
IRF9610	SMP2P20	
IRF9611	SMP2P20	
IRF9612	SMP2P20	
IRF9613	SMP2P20	
IRF9640	SMP11P20	
IRF9641	SMP11P20	
IRF9642	SMP11P20	
IRF9643	SMP9P15	
IRFD9110	SMV1P10	
IRFD9113	SMV1P06	
IRFD9210	SMV1P20	
IRFD9213	SMV1P15	
IRFK2D450(2)	SPMB50A500	
IRFK4H450	SPMF50A500	
IRFK4H450(2)	SPMB50A500	
IRFP040	SMW60N06	
IRFP042	SMW60N06	
IRFP044	SMW60N06	
IRFP045	SMW60N06	
IRFP050	SMW60N06	
IRFP054	SMW70N06-14	
IRFP150	SMW45N10	
IRFP151	SMW45N10	
IRFP152	SMW45N10	
IRFP153	SMW45N10	
IRFP9140	SMW20N10	
IRFP9141	SMW20N10	
IRFP9142	SMW20N10	
IRFP9143	SMW20N10	
IRFP9240	SMW12N20	
IRFP9241	SMW12N20	
IRFP9242	SMW12N20	
IRFP9243	SMW12N20	
IRFR010	SMD15N05	
IRFR020	SMD15N05	
IRFR9010	SMD10N05	
IRFR9020	SMD10P05	
IRFU010	SMD10P05	
IRFU020	SMD15N05	
IRFU9020	SMD10P05	
IRFZ20		BUZ71
IRFZ22		BUZ71A
IRFZ24		BUZ71
IRFZ30		BUZ11
IRFZ32		SMP25N05
IRFZ34		SMP25N06
IRFZ40	SMP50N05	
IRFZ42	SMP50N05	
IRFZ44	SMP50N06	
IRFZ45	SMP50N06	
IXFH12N50	SMW14N50F	
IXFH13N50	SMW14N50F	
IXFH67N10		SMW60N10
IXFH75N10		SMW60N10
IXTP4N60	SMP4N60	
IXTP4N60A	SMP4N60	
IXTP6N60	SMP7N60	
IXTP6N60A	SMP7N60	
JD225005	SPMB50A500	

Cross Reference

Siliconix incorporated

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
JS525075	SPMB50A500	
JS525075(2)	SPMF50A500	
JT225005	SPMF50A500	
MG50G2DM1	SPMF50A500	
MG50G2YM1	SPMB50A500	
MPF930		2N7010*
MPF960		2N7010*
MT50BY45	SPMB50A500	
MTD4P05	SMD10P05	
MTD4P05-1	SMU10P05	
MTD10N05E	SMD15N05	
MTD10N05E-1	SMU15N05	
MTD2955	SMD10P05	
MTD2955-1	SMU10P05	
MTD3055E	SMD15P05	
MTD3055E-1	SMU15P05	
MTH8P20	SMW12P20	
MTH20P10	SMW20P10	
MTH35N05	SMW60N06	
MTH35N06	SMW60N06	
MTH35N06E	SMW60N06	
MTH40N06	SMW60N06	
MTH40N08	SMW45N10	
MTH40N10	SMW45N10	
MTH50N05	SMW60N06	
MTM20P08		SMM20P10
MTM20P10		SMM20P10
MTM40N20	SMM40N20*	
MTM50N05E	SMM60N05	
MTM60N05	SMM60N05	
MTM60N06	SMM60N06	
MTP2N55		SMP4N60
MTP2N60		SMP4N60
MTP3N55	SMP4N60	
MTP3N60	SMP4N60	
MTP10N05	BUZ71A	
MTP12N05	BUZ71A	
MTP15P05	BUZ71	
MTP15P06	SMP25N06	
MTP25N05	SMP25N05	
MTP25N10		SMP30N10
MTP50N05	SMP50N06-25	
MTP50N05E	SMP50N06-25	
PM50502C	SPMF50A500	
RFD10N05	SMU15N05	
RFD10N05SM	SMD15N05	
RFD14N05	SMU15N05	
RFD14N05SM	SMD15N05	
RFD16N05LSM	SMD25N05-45L	
RFD16N05SM		SMD25N05-45L
RFG50N05	SMW60N06-18	
RFK45N05	SMM60N05	
RFK45N06	SMM60N05	
RFP25N05	SMP25N05	
RFP25N05L	SMP25N05-45L	
RFP25N06	SMP25N06	
RFP50N05	SMP60N06-18	

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
SSM6N55		SMP7N60
SSM6N60		SMP7N60
SSM10N70		SMM14N65*
SSM15N55		SMM14N65*
SSM15N60		SMM14N65*
SSM20N45		SMM20N50*
SSM20N50		SMM20N50*
SSM25N34		SMM24N40*
SSM25N40		SMM24N40*
SSM40N15		SMM40N20*
SSP4N55	SMP4N60	
SSP4N60	SMP4N60	
STVHD90	SMP60N06-18	
TSC4469EOD	D469ADJ	
TSC4469EPD	D469ADJ	
TSC9100ENP	SI9100DN	
TSC9100EPF	SI9100DJ	
TSC9101ENP	SI9101DN	
TSC9101EPF	SI9101DJ	
TSC9102ENP	SI9102DN	
TSC9102EPF	SI9102DJ	
TSC9105ENP	SI9105DN	
TSC9105EPF	SI9105DJ	
TSC9110EOF	SI9110DY	
TSC9110EPF	SI9110DJ	
TSC9110MJF	SI9110AK	
TSC9111EOF	SI9111DY	
TSC9111EPF	SI9111DJ	
TSC9112EPF	SI9112DJ	
TSC9120EPF	SI9120DJ	
TSD4M450V	SPMB50A500	
TSD4M450(2)	SPMF50A500	
UNF220		BUZ71
VNC003A	SMM60N06	
VNG004A	SMM40N20*	
VNJ004A	SMM40N20*	
VNL005A	SMM24N40*	
VNM005A	SMM24N40*	
VNN006A	SMM20N50*	
VNP006A	SMM20N50*	
VNT012A	SMM14N65*	
VNT013A	SMM14N65*	
2M150F050	SPMF50A500	
2M150S050	SPMF50A500	
2N6803	IRF9130	
2N6804	IRF9130	
2N6805	IRF9230	
2N6806	IRF9230	
2N7054	SMW45N10	
2N7055	IRFP250	
2N7057	IRFP350	
2N7058	IRFP450	
2SK562		SMP50N05
2SK682	IRFP450	
2SK683	IRFP450	

This Cross Reference material is accurate to the best knowledge and belief of Siliconix, incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.

*Contact your local sales office for a data sheet, see selector guide for critical specifications.

PROCESS OPTION FLOW CHARTS

Manufacturing Process Option Flows for Discrete Devices

Test & Condition		U.S. Build Only If Specified	U.S. Build U.S. Test	Off Shore Build
Description	Methods Per MIL-STD-19500	Space Rated Extended Hi-Rel	S/S JANTXV or -1 Devices	100% Screening & Test U.S. JANTX/SS or -2 Devices
Traceability to W/L		X	N/A	N/A
SEM	2077	X	N/A	N/A
Internal Visual	2069	Inhouse Spec Cond A	Inhouse Spec Cond B	Inhouse Spec Cond B
Bond Strength** Cert/Data	2037	X	N/A	N/A
Stab Bake	1032	X	X	X
Temp Cycle	1051	X	X	X
Centrifuge	2006	X	X	X
PIND	2052	X	N/A	N/A
Fine Leak (See Note)	1071	Cond G or H	Cond G or H	Cond G or H
Gross Leak (See Note)	1071	Cond C or K	Cond C or K	Cond C or K
Thermal Response	3161	X	X	X
Inductive Load	3470	X	X	X
1st Electrical	Per Spec	Read/Record	Go/No-Go	Go/No-Go
Burn-in	1042 Cond B	48 Hrs Per Dwg	48 Hrs Per Dwg	48 Hrs Per Dwg
Interim Electrical Post Burn-in	Per Spec	Read/Record Per Spec	Read/Record Per Spec	Read/Record Per Spec
Burn-in	1042 Cond A	160 Hrs Min	160 Hrs	160 Hrs
Burn-in	1042 Cond C	240 Hrs Min	N/A	N/A
Intermin Electrical Post Burn-in	Static* Per Spec	Read/Record 25°C PDA = 10%	Read/Record 25°C PDA = 10%	Read/Record 25°C PDA = 10%
Final Electrical	Static 25°C	25°C, -55°C, +125°C	25°C	25°C
X-ray	2076	X	N/A	N/A
External Visual	2012	X	X	X
QCI A 19500 MIL Spec	Per Spec	X	X Note	X Note
QCI B 19500 MIL Spec	Per Spec	X	X Note	X Note
QCI C 19500 MIL Spec	Per Spec	X	X Note	X Note
B/I Deltas Option	Per Spec	Option	Per Spec	Per Spec
Solder Dip Option	Per Spec	Option	Per Spec	Per Spec
Note: Fine/gross leak test may be done at either steps after centrifuge or after final electrical. ** = Test performed on line during assembly procedure (monitor).	* = PDA applies to both burn-ins.	Notice: On U.S. builds unless otherwise specified by 19500 or dwg. Parts may be assembled off shore.	Note: -1 & -2 devices QCI B & C will be performed by dwg and/or P.O. only. All S/S devices will be tested accordingly.	

Process Option Flows for Discrete Chip/Wafer

Standard Die/Chip, and Chip Samples with Element Evaluation		
Die ship element evaluation Method 5008 Class B Subgroup 1 & 3 performed in-line screen.	**Die ship. No canned samples.**	**Die Wafer Form**
Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec.
Canned samples: Per MIL-STD-883, Class B device. Subgroup 1 (ss-10/0) internal visual Method 2069 Cond B inhouse spec. Subgroup 2 (ss-10/1) final electrical static @ 25°C, elevated temperature per device spec. Subgroup 3 (5 die min) (s/s = 10/0 or 20/1 wires) NDT Method 2023 wire bond eval (bond pull). Method 2011 (cert & data). *SEM available	Die Prep Process	

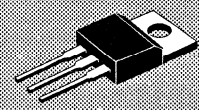
Manufacturing Process Option Flows for Integrated Circuits

Test & Condition		Parts Shall Be Marked PN/883
Description	**Method Per MIL-STD-883**	**/883 Compliant Non-JAN Method 5004/5005**
Traceability Wafer Lot		X
Internal VIS	2010	Cond B
Stab Bake	1008-C	X
Temp Cycle	1010-C	X
Centrifuge	2001-E	X
Fine Leak	1014 A or B	X
Gross Leak	1014-C	X
1st Electrical	Per Spec	X
Burn-in	1015 A or C	160 Hrs A or C
Interim Electrical Post Burn-in		Static 25°C, PDA = 5%
Final Electrical	Min Temp	X
Final Electrical	Max Temp	X
QCI A	5005	X
QCI B	5005	X
QCI C	5005	X
QCI D	5005	X
External Visual	2009	X
Deltas		Option
Solder Dip		Option
		Note: Parts not qualified for /883 must not be marked as such. A special flow for this product will be generated as custom.

TABLE OF CONTENTS

Selector Guide
Plastic Packages

TO-220



N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
650	5.8	1.5	VNT008D[1]
650	5.0	2.0	VNT009D[1]
600	7.0	1.1	SMP7N60
600	4.0	2.0	SMP4N60
500	8.0	0.85	SMP8N50F[2]
500	4.5	1.5	SMP5N50F[2]
500	2.5	3.0	SMP3N50F[2]
200	20	0.16	SMP20N20
100	40	0.040	SMP40N10
100	30	0.060	SMP30N10
60	60	0.014	SMP60N06-14
60	60	0.018	SMP60N06-18
60	60	0.023	SMP60N06
60	46	0.025	SMP50N06-25
60	50	0.028	SMP50N06[1]
60	25	0.060	SMP25N06
50	60	0.023	SMP60N05[1]
50	50	0.028	SMP50N05[1]

N-Channel (Cont'd)

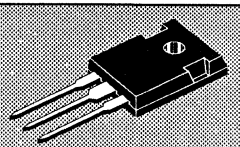
$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
50	30	0.040	BUZ11
50	25	0.060	BUZ11A[1]
50	25	0.060	SMP25N05[1]
50	25	0.045	SMP25N05-45L[3]
50	14	0.10	BUZ71
50	14	0.12	BUZ71A

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-11	0.50	SMP11P20
-100	-20	0.20	SMP20P10
-100	-3.0	1.2	SMP3P10
-60	-16	0.30	SMP16P06[1]
-60	-2.5	1.6	SMP3P06[1]
-50	-7.0	0.40	BUZ171

3

TO-247



N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
500	14	0.40	SMW14N50F[2]
100	60	0.025	SMW60N10
100	45	0.040	SMW45N10
60	70	0.014	SMW70N06-14
60	70	0.018	SMW70N06[1]
60	60	0.018	SMW60N06-18

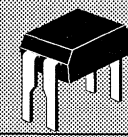
P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-12	0.50	SMW12P20
-100	-20	0.20	SMW20P10

[1]Not recommended for new designs
[2]F Suffix = Integral fast reverse recovery diode
[3]Logic level device. $r_{DS(on)}$ specified at V_{GS} = 5 V

Plastic Packages (Cont'd)

4-Pin FETDIP



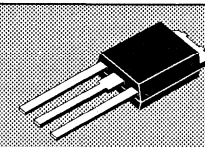
P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-0.40	3.0	SMV1P20
-150	-0.30	4.5	SMV1P15

P-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-100	-0.70	1.2	SMV1P10
-60	-0.60	1.6	SMV1P06

TO-251



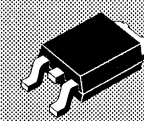
N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
50	15	0.100	SMU15N05

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-50	10	0.280	SMU10P05

TO-252



N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
50	24	0.045	SMD25N05-45L[3]
50	15	0.100	SMD15N05

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
50	10	0.280	SMD10P05
50	10	0.280	SMD10P05L[3]

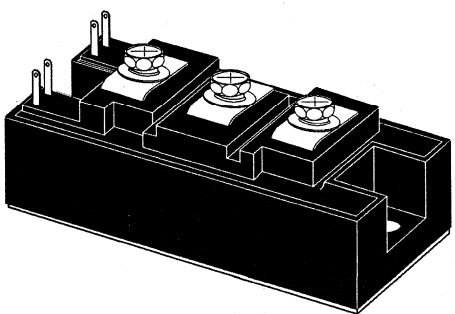
[1]Not recommended for new designs
[2]F Suffix = Integral fast reverse recovery diode
[3]Logic level device. $r_{DS(on)}$ specified at V_{GS} = 5 V

Plastic Packages (Cont'd)

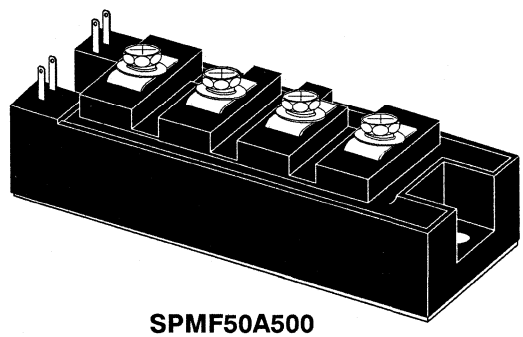
Industrial Modules

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Configuration	Part Number
500	50	0.100	Half-Bridge	SPMB50A500
500	50	0.100	2 Individual	SPMF50A500



SPMB50A500

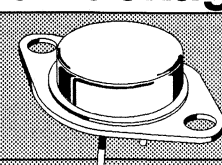


SPMF50A500

3

Hermetic Packages

TO-204 (TO-3)



N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
650	14	0.60	SMM14N65[1]
500	20	0.30	SMM20N50[1]
400	24	0.23	SMM24N40[1]
200	40	0.060	SMM40N20[1]
100	70	0.025	SMM70N10
60	70	0.018	SMM70N06[1]

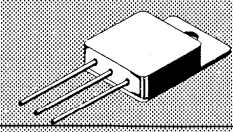
P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-11	0.50	SMM11P20[1]
-100	-20	0.20	SMM20P10[1]
-60	-16	0.30	SMM16P06[1]

[1]Not recommended for new designs

Hermetic Packages (Cont'd)

TO-254



N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
500	13	0.40	2N7078
500	7	0.85	2N7074
400	15	0.30	2N7077
400	9	0.55	2N7073
200	28	0.1	2N7076
200	16	0.2	2N7072

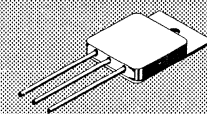
N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
100	30	0.065	2N7075
100	23	0.100	2N7071

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-9.5	0.5	2N7080
-100	-17	0.210	2N7079

TO-257



N-Channel

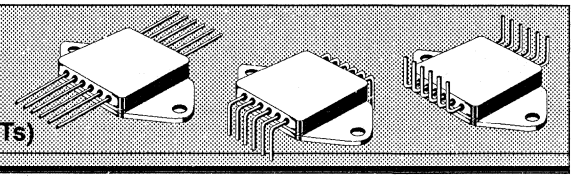
$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
200	14	0.160	2N7086
200	9	0.300	2N7082
100	20	0.075	2N7085
100	12	0.150	2N7081

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Part Number
-200	-8	0.500	2N7092
-200	-5.7	0.800	2N7090
-100	-14	0.200	2N7091
-100	-10	0.300	2N7089

MOD Package

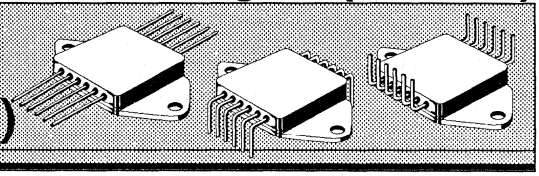
(4 Electrically-Isolated N-Channel MOSFETs)



$V_{(BR)DSS}$ (V)	Single Die I_D (Cont) (A)	Single Die I_D (Pulse) (A)	Single Die $r_{DS(ON)}$ (Ω)	Lead Configuration	Part Number
500	13	52	0.43	Straight	MOD500A
500	13	52	0.43	Formed Down	MOD500B
500	13	52	0.43	Formed Up	MOD500C
400	15	60	0.35	Straight	MOD400A
400	15	60	0.35	Formed Down	MOD400B
400	15	60	0.35	Formed Up	MOD400C

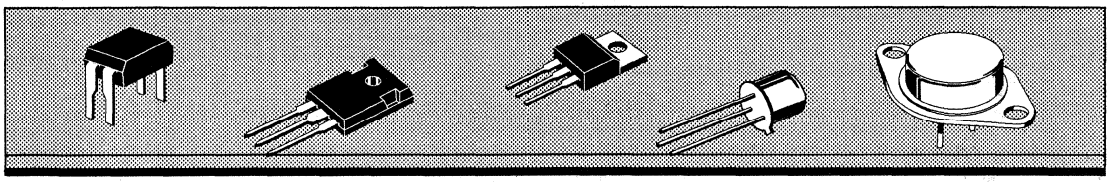
Hermetic Packages (Cont'd)

MOD Package (Cont'd)



$V_{(BR)DSS}$ (V)	Single Die I_D (Cont) (A)	Single Die I_D (Pulse) (A)	Single Die $r_{DS(ON)}$ (Ω)	Lead Configuration	Part Number
200	21	100	0.11	Straight	MOD200A
200	21	100	0.11	Formed Down	MOD200B
200	21	100	0.11	Formed Up	MOD200C
100	21	125	0.08	Straight	MOD100A
100	21	125	0.08	Formed Down	MOD100B
100	21	125	0.08	Formed Up	MOD100C

Industry Standard Commercial MOSFETs



Part Number	$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Package
IRF130[1]	100	14	0.18	TO-204
IRF131[1]	60	14	0.18	TO-204
IRF132[1]	100	12	0.25	TO-204
IRF133[1]	60	12	0.25	TO-204
IRF140[1]	100	27	0.085	TO-204
IRF141[1]	60	27	0.085	TO-204
IRF142[1]	100	24	0.11	TO-204
IRF143[1]	60	24	0.11	TO-204
IRF150[1]	100	40	0.055	TO-204
IRF151[1]	60	40	0.055	TO-204
IRF152[1]	100	33	0.080	TO-204
IRF153[1]	60	33	0.080	TO-204
IRF230[1]	200	9.0	0.40	TO-204
IRF231[1]	150	9.0	0.40	TO-204
IRF232[1]	200	8.0	0.60	TO-204
IRF233[1]	150	8.0	0.60	TO-204
IRF240[1]	200	18	0.18	TO-204
IRF241[1]	150	18	0.18	TO-204
IRF242[1]	200	16	0.22	TO-204
IRF243[1]	150	16	0.22	TO-204
IRF250[1]	200	30	0.085	TO-204
IRF251[1]	150	30	0.085	TO-204
IRF252[1]	200	25	0.12	TO-204
IRF253[1]	150	25	0.12	TO-204
IRF330[1]	400	5.5	1.0	TO-204
IRF331[1]	350	5.5	1.0	TO-204
IRF332[1]	400	4.5	1.5	TO-204
IRF333[1]	350	4.5	1.5	TO-204
IRF340[1]	400	10	0.55	TO-204
IRF341[1]	350	10	0.55	TO-204
IRF342[1]	400	8.0	0.80	TO-204
IRF343[1]	350	8.0	0.80	TO-204
IRF350[1]	400	15	0.30	TO-204
IRF351[1]	350	15	0.30	TO-204
IRF352[1]	400	13	0.40	TO-204
IRF353[1]	350	13	0.40	TO-204
IRF430[1]	500	4.5	1.5	TO-204
IRF431[1]	450	4.5	1.5	TO-204
IRF432[1]	500	4.0	2.0	TO-204
IRF433[1]	450	4.0	2.0	TO-204
IRF440[1]	500	8.0	0.85	TO-204
IRF441[1]	450	8.0	0.85	TO-204
IRF442[1]	500	7.0	1.1	TO-204
IRF443[1]	450	7.0	1.1	TO-204
IRF450[1]	500	13	0.40	TO-204
IRF451[1]	450	13	0.40	TO-204
IRF452[1]	500	12	0.50	TO-204
IRF453[1]	450	12	0.50	TO-204
IRF510	100	4.0	0.60	TO-220
IRF511[1]	60	4.0	0.60	TO-220
IRF512[1]	100	3.5	0.80	TO-220
IRF513[1]	60	3.5	0.80	TO-220
IRF520	100	8.0	0.30	TO-220
IRF521[1]	60	8.0	0.30	TO-220
IRF522[1]	100	7.0	0.40	TO-220
IRF523[1]	60	7.0	0.40	TO-220
IRF530	100	14	0.18	TO-220
IRF531[1]	60	14	0.18	TO-220
IRF532[1]	100	12	0.25	TO-220
IRF533[1]	60	12	0.25	TO-220
IRF540	100	27	0.085	TO-220
IRF541[1]	60	27	0.085	TO-220
IRF542[1]	100	24	0.11	TO-220
IRF543[1]	60	24	0.11	TO-220
IRF610	200	2.5	1.5	TO-220
IRF611[1]	150	2.5	1.5	TO-220
IRF612[1]	200	2.0	2.4	TO-220
IRF613[1]	150	2.0	2.4	TO-220
IRF620	200	5.0	0.80	TO-220
IRF621[1]	150	5.0	0.80	TO-220
IRF622[1]	200	4.0	1.2	TO-220
IRF623[1]	150	4.0	1.2	TO-220
IRF630	200	9.0	0.40	TO-220
IRF631[1]	150	9.0	0.40	TO-220
IRF632[1]	200	8.0	0.60	TO-220
IRF633[1]	150	8.0	0.60	TO-220

[1]Not recommended for new designs

Industry Standard Commercial MOSFETs (Cont'd)

Part Number	$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Package
IRF640	200	18	0.18	TO-220
IRF642[1]	200	16	0.22	TO-220
IRF643[1]	150	16	0.22	TO-220
IRF710[1]	400	1.5	3.6	TO-220
IRF711[1]	350	1.5	3.6	TO-220
IRF712[1]	400	1.3	5.0	TO-220
IRF713[1]	350	1.3	5.0	TO-220
IRF720	400	3.0	1.8	TO-220
IRF721[1]	350	3.0	1.8	TO-220
IRF722[1]	400	2.5	2.5	TO-220
IRF723[1]	350	2.5	2.5	TO-220
IRF730	400	5.5	1.0	TO-220
IRF731[1]	350	5.5	1.0	TO-220
IRF732[1]	400	4.5	1.5	TO-220
IRF733[1]	350	4.5	1.5	TO-220
IRF740	400	10	0.55	TO-220
IRF741[1]	350	10	0.55	TO-220
IRF742[1]	400	8.0	0.80	TO-220
IRF743[1]	350	8.0	0.80	TO-220
IRF820	500	2.5	3.0	TO-220
IRF821[1]	450	2.5	3.0	TO-220
IRF822[1]	500	2.0	4.0	TO-220
IRF823[1]	450	2.0	4.0	TO-220
IRF830	500	4.5	1.5	TO-220
IRF831[1]	450	4.5	1.5	TO-220
IRF832[1]	500	4.0	2.0	TO-220
IRF833[1]	450	4.0	2.0	TO-220
IRF840	500	8.0	0.85	TO-220
IRF841[1]	450	8.0	0.85	TO-220
IRF842[1]	500	7.0	1.1	TO-220
IRF843[1]	450	7.0	1.1	TO-220
IRF9130[1]	-100	-12	0.30	TO-204
IRF9131[1]	-60	-12	0.30	TO-204
IRF9132[1]	-100	-10	0.40	TO-204
IRF9133[1]	-60	-10	0.40	TO-204
IRF9230	-200	-6.5	0.80	TO-204
IRF9231[1]	-150	-6.5	0.80	TO-204
IRF9232[1]	-200	-5.5	1.2	TO-204
IRF9233[1]	-150	-5.5	1.2	TO-204
IRF9520[1]	-100	-6.0	0.60	TO-220
IRF9521[1]	-60	-6.0	0.60	TO-220
IRF9522[1]	-100	-5.0	0.80	TO-220
IRF9523[1]	-60	-5.0	0.80	TO-220
IRF9530	-100	-12	0.30	TO-220
IRF9531[1]	-60	-12	0.30	TO-220
IRF9532[1]	-100	-10	0.40	TO-220
IRF9533[1]	-60	-10	0.40	TO-220
IRF9620	-200	-3.5	1.5	TO-220
IRF9621[1]	-150	-3.5	1.5	TO-220
IRF9622[1]	-200	-3.0	2.4	TO-220
IRF9623[1]	-150	-3.0	2.4	TO-220
IRF9630	-200	-6.5	0.80	TO-220
IRF9631[1]	-150	-6.5	0.80	TO-220
IRF9632[1]	-200	-5.5	1.2	TO-220
IRF9633[1]	-150	-5.5	1.2	TO-220
IRFD110	100	1.0	0.60	TO-250
IRFD113[1]	60	0.80	0.80	TO-250
IRFD120	100	1.3	0.30	TO-250
IRFD123	60	1.1	0.40	TO-250
IRFD210	200	0.60	1.5	TO-250
IRFD213[1]	150	0.45	2.4	TO-250
IRFD220	200	0.80	0.80	TO-250
IRFD223[1]	150	0.70	1.2	TO-250
IRFD020	50	2.4	0.10	TO-250
IRFD022[1]	50	2.2	0.12	TO-250
IRFD9020	-50	-1.6	0.28	TO-250
IRFD9022[1]	-50	-1.4	0.33	TO-250
IRFD9120	-100	-1.0	0.60	TO-250
IRFD9123[1]	-60	-0.80	0.80	TO-250
IRFD9220	-200	-0.6	1.5	TO-250
IRFD9223[1]	-150	-0.45	2.4	TO-250
IRFF110[1]	100	3.5	0.60	TO-205
IRFF111[1]	60	3.5	0.60	TO-205
IRFF112[1]	100	3.0	0.80	TO-205
IRFF113[1]	60	3.0	0.80	TO-205
IRFF120[1]	100	6.0	0.30	TO-205
IRFF121[1]	60	6.0	0.30	TO-205
IRFF122[1]	100	5.0	0.40	TO-205
IRFF123[1]	60	5.0	0.40	TO-205
IRFF130[1]	100	8.0	0.18	TO-205
IRFF131[1]	60	8.0	0.18	TO-205
IRFF132[1]	100	7.0	0.25	TO-205
IRFF133[1]	60	7.0	0.25	TO-205

[1]Not recommended for new designs

NOTE: Negative voltage indicates P-Channel MOSFET

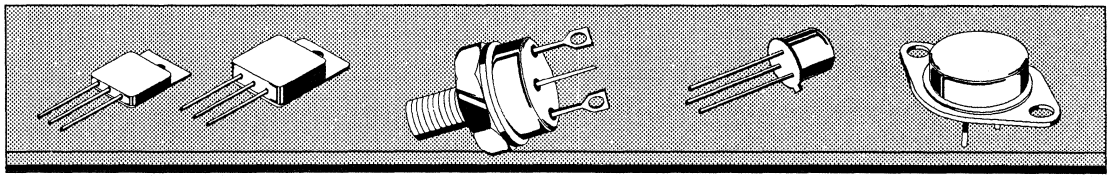
Industry Standard Commercial MOSFETs (Cont'd)

Part Number	$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	Package
IRFF210[1]	200	2.2	1.5	TO-205
IRFF211[1]	150	2.2	1.5	TO-205
IRFF212[1]	200	1.8	2.4	TO-205
IRFF213[1]	150	1.8	2.4	TO-205
IRFF220[1]	200	3.5	0.80	TO-205
IRFF221[1]	150	3.5	0.80	TO-205
IRFF222[1]	200	3.0	1.2	TO-205
IRFF223[1]	150	3.0	1.2	TO-205
IRFF230[1]	200	5.5	0.40	TO-205
IRFF231[1]	150	5.5	0.40	TO-205
IRFF232[1]	200	4.5	0.60	TO-205
IRFF233[1]	150	4.5	0.60	TO-205
IRFF310[1]	400	1.35	3.6	TO-205
IRFF311[1]	350	1.35	3.6	TO-205
IRFF312[1]	400	1.15	5.0	TO-205
IRFF313[1]	350	1.15	5.0	TO-205
IRFF320[1]	400	2.5	1.8	TO-205
IRFF321[1]	350	2.5	1.8	TO-205
IRFF322[1]	400	2.0	2.5	TO-205
IRFF323[1]	350	2.0	2.5	TO-205
IRFF330[1]	400	3.5	1.0	TO-205
IRFF331[1]	350	3.5	1.0	TO-205
IRFF332[1]	400	3.0	1.5	TO-205
IRFF333[1]	350	3.0	1.5	TO-205
IRFF420[1]	500	1.6	3.0	TO-205
IRFF421[1]	450	1.6	3.0	TO-205
IRFF422[1]	500	1.4	4.0	TO-205
IRFF423[1]	400	1.4	4.0	TO-205
IRFF430[1]	500	2.75	1.5	TO-205
IRFF431[1]	450	2.75	1.5	TO-205
IRFF433[1]	450	2.25	2.0	TO-205
IRFF9120[1]	-100	-4.0	0.60	TO-205
IRFF9121[1]	-60	-4.0	0.60	TO-205
IRFF9122[1]	-100	-3.5	0.80	TO-205
IRFF9123[1]	-60	-3.5	0.80	TO-205
IRFF9130[1]	-100	-6.5	0.30	TO-205
IRFF9131[1]	-60	-6.5	0.30	TO-205
IRFF9132[1]	-100	-5.5	0.40	TO-205
IRFF9133[1]	-60	-5.5	0.40	TO-205
IRFF9220[1]	-200	-2.5	1.5	TO-205
IRFF9221[1]	-150	-2.5	1.5	TO-205
IRFF9222[1]	-200	-2.0	2.4	TO-205
IRFF9223[1]	-150	-2.0	2.4	TO-205
IRFF9230[1]	-200	-4.0	0.80	TO-205
IRFF9231[1]	-150	-4.0	0.80	TO-205
IRFF9232[1]	-200	-3.5	1.2	TO-205
IRFF9233[1]	-150	-3.5	1.2	TO-205
IRFP250	200	33	0.085	TO-247
IRFP350	400	16	0.30	TO-247
IRFP450	500	14	0.40	TO-247

[1]Not recommended for new designs

NOTE: Negative voltage indicates P-Channel MOSFET

Industry Standard Military MOSFETs

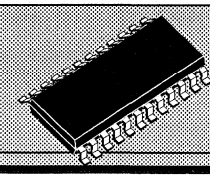


Part Number	$V_{(BR)DSS}$ (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	P_D (W)	Package	Equivalent Commercial Part Number	QPL Product in accordance with 19500/
2N6756	100	14	0.18	75	TO-204	IRF130	542
2N6758	200	9.0	0.40	75	TO-204	IRF230	542
2N6760	400	5.5	1.0	75	TO-204	IRF330	542
2N6762	500	4.5	1.5	75	TO-204	IRF430	542
2N6764	100	38	0.055	150	TO-204	IRF150	543
2N6766	200	30	0.085	150	TO-204	IRF250	543
2N6768	400	14	0.30	150	TO-204	IRF350	543
2N6770	500	12	0.40	150	TO-204	IRF450	543
2N6788	100	6.0	0.30	20	TO-205	IRFF120	555
2N6790	200	3.5	0.80	20	TO-205	IRFF220	555
2N6792	400	2.0	1.8	20	TO-205	IRFF320	555
2N6794	500	1.5	3.0	20	TO-205	IRFF420	555
2N6796	100	8.0	0.18	25	TO-205	IRFF130	557
2N6798	200	5.5	0.40	25	TO-205	IRFF230	557
2N6800	400	3.0	1.0	25	TO-205	IRFF330	557
2N6802	500	2.5	1.5	25	TO-205	IRFF430	557
2N6962	100	30	0.060	150	TO-210	-	568
2N6963	200	30	0.090	150	TO-210	-	568
2N6964	400	15	0.30	150	TO-210	-	568
2N6965	500	13	0.40	150	TO-210	-	568
2N7071	100	23	0.10	100	TO-254	-	-
2N7072	200	16	0.200	100	TO-254	-	-
2N7073	400	9	0.55	100	TO-254	-	-
2N7074	500	7	0.85	100	TO-254	-	-
2N7075	100	30	0.065	150	TO-254	-	-
2N7076	200	28	0.10	150	TO-254	-	-
2N7077	400	15	0.30	150	TO-254	-	-
2N7078	500	13	0.40	150	TO-254	-	-
2N7079	-100	-17	0.21	100	TO-254	-	-
2N7080	-200	-9.5	0.51	100	TO-254	-	-
2N7081	100	12	0.150	45	TO-257	-	-
2N7082	200	9	0.300	50	TO-257	-	-
2N7085	100	20	0.075	60	TO-257	-	-
2N7086	200	14	0.160	60	TO-257	-	-
2N7089	-100	-10	0.300	60	TO-257	-	-
2N7090	-200	-5.7	0.800	60	TO-257	-	-
2N7091	-100	-14	0.200	70	TO-257	-	-
2N7092	-200	-8	0.500	70	TO-257	-	-

NOTES: Negative voltage indicates P-Channel MOSFET. For processing options on products with no QPL specifications see Section 3 "Process Option Flow Charts".

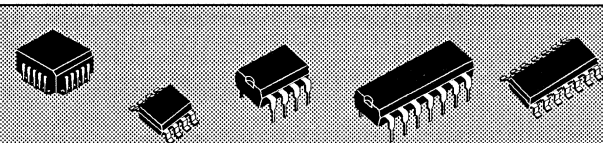
Power ICs

VCM & Spindle Drivers



Part Number	Functional Description	Peak Output Current (A)	Supply Voltage (V)	Target Application	Package Type
Si9961CY	Transconductance Amplifier for Voice Coil Motors	1	12	Hard Disk Drives & Optical Disk Drives	24 Pin SOIC
Si9962CY	Transconductance Amplifier for Voice Coil Motors	0.2	5	Hard Disk Drives & Optical Disk Drives	24 Pin SOIC
Si9985CY	Sensorless, 3 Phase Spindle Motor Driver	1	5	Hard Disk Drives	24 Pin SOIC

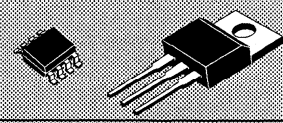
MOSFET Drivers



Part Number	Functional Description	Peak Output Drive Current (A)	Target Application	Package Type
D469AAP	Quad CMOS Driver with Complementary Inputs	1.5	Motor Drives & Power Supplies	14 Pin Ceramic Dip
D469ADJ		1.5		14 Pin Plastic Dip
D469ADN		1.5		20 Pin PLCC
Si9910DJ	Adaptive High or Low Side Drivers with Protection Features	1.0	Motor Drives & UPS	8 Pin Plastic Dip
Si9910DY		1.0		8 Pin SOIC
Si9975DY	N-Channel Half-Bridge Driver With 20 to 40 V Supply Range	0.5	Motor Drives	8 Pin SOIC
Si9976DY		0.5		14 Pin SOIC
Si9901DJ	Adaptive Driver With 500 V Level Shift for Use With Si9911 & Si9914	1.0	Motor Drives & UPS	16 Pin Dip
Si9901DY		1.0		16 Pin SOIC
Si9911DJ	Adaptive High Side Drivers with for Use with Si9901	1.0	Motor Drives & UPS	8 Pin Dip
Si9911DY		1.0		8 Pin SOIC
Si9914DJ	Adaptive High Side Drivers for Use with Si9901	1.0	Motor Drives & UPS	8 Pin Dip
Si9914DY		1.0		8 Pin SOIC

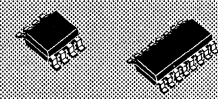
Power ICs (Cont'd)

High Voltage Linear Regulators



Part Number	Input Voltage (V)	Output Voltage	Load Reg.	Line Reg.	Output Current (mA)	Package Type
Si9905DD	50 to 450	5 V ±5%	±2%	±1%	20	TO-220
Si9905DY	50 to 450	5 V ±5%	±2%	±1%	10	8 Pin SOIC
Si9912DD	50 to 450	12 V ±5%	±2%	±1%	20	TO-220
Si9912DY	50 to 450	12 V ±5%	±2%	±1%	10	8 Pin SOIC
Si9915DD	50 to 450	15 V ±5%	±2%	±1%	20	TO-220
Si9915DY	50 to 450	15 V ±5%	±2%	±1%	10	8 Pin SOIC

MOSFET Half-Bridges

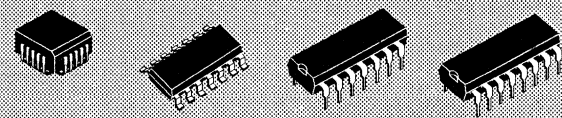


Part Number	Functional Description*	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ N-Channel (Ω)	$r_{DS(ON)}$ P-Channel (Ω)	I_D (A)**	Package Type
Si9950DY	Half-Bridge	50	0.3	0.3	2.0	16 Pin SOIC
Si9951DY	Half-Bridge	18	0.6	0.7	1.5	8 Pin SOIC
Si9952DY	Dual N-& P-Channel	20	0.1	0.4	2.2	8 Pin SOIC
Si9954DY	Half-Bridge	50	0.1	0.25	3.0	16 Pin SOIC
Si9955DY	Dual N-Channel	50	0.13 each		3.0	8 Pin SOIC
Si9956DY	Dual N-Channel	20	0.1 each		3.5	8 Pin SOIC

* Half-Bridges connect drains internal to package. Duals are electrically isolated MOSFETs
** Surface Mounted continuous current rating

Power ICs (Cont'd)

Switchmode Products



Part Number	Functional Description*	Operating Range (V)	Converter Range (W)	Target Market Segment	Package Type
Si9100DJ	CMOS Regulator	10 to 70	< 3	Telecom	14 Pin Plastic Dip
Si9100DN	CMOS Regulator	10 to 70	< 3	Telecom	20 Pin PLCC
Si9101DJ	CMOS Regulator	10 to 70	< 3	Telecom	14 Pin Plastic Dip
Si9101DN	CMOS Regulator	10 to 70	< 3	Telecom	20 Pin PLCC
Si9102DJ	CMOS Regulator	10 to 120	< 3	Telecom	14 Pin Plastic Dip
Si9102DN	CMOS Regulator	10 to 120	< 3	Telecom	20 Pin PLCC
Si9105DJ	CMOS Regulator	10 to 120	< 1	Telecom	14 Pin Plastic Dip
Si9105DN	CMOS Regulator	10 to 120	< 1	Telecom	20 Pin PLCC
Si9110AK	CMOS Controller	10 to 120	< 35	Military	14 Pin Ceramic Dip
Si9110DJ	CMOS Controller	10 to 120	< 35	Telecom	14 Pin Plastic Dip
Si9110DY	CMOS Controller	10 to 120	< 35	Telecom	14 Pin SOIC
Si9111DJ	CMOS Controller	10 to 120	< 35	Telecom	14 Pin Plastic Dip
Si9111DY	CMOS Controller	10 to 120	< 35	Telecom	14 Pin SOIC
Si9112DJ	CMOS Controller	9 to 80	< 35	Computer/Industrial	14 Pin Plastic Dip
Si9112DY	CMOS Controller	9 to 80	< 35	Computer/Industrial	14 Pin SOIC
Si9120DJ	CMOS Controller	50 to 450	< 50	Computer/Industrial	16 Pin Plastic Dip

* Regulators have on board MOSFETs. Controllers drive external MOSFETs.

CAN BUS Driver

Part Number	Functional Description*	Supply Voltage (V)	Output Current (mA)	Application	Package Type
Si9200AY	Transciever IC that Interfaces Between a BUS Controller and the Physical BUS	4.5 to 5.5	35	Automobiles and Industrial Controllers	8 Pin SOIC

Siliconix incorporated

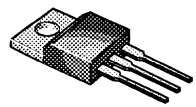
BUZ11

N-Channel Enhancement Mode Transistor

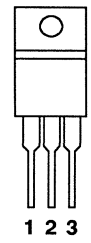
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
50	0.040	30

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		19	
Pulsed Drain Current[1]		I_{DM}	120	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		75	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.1	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		30		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A	0.030		0.040	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	0.045		0.070	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 15 A	8.0	4.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1900		2000	pF
Output Capacitance	C_{oss}		1000		1100	
Reverse Transfer Capacitance	C_{rss}		260		400	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A	52		75	nC
Gate-Source Charge[2]	Q_{gs}		14			
Gate-Drain Charge[2]	Q_{gd}		22			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω	30		45	ns
Rise Time[2]	t_r		50		110	
Turn-Off Delay Time[2]	$t_{d(off)}$		100		230	
Fall Time[2]	t_f		110		170	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				30	A
Pulsed Current[3]	I_{SM}				120	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	65			ns
Reverse Recovery Charge	Q_{rr}		0.16			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

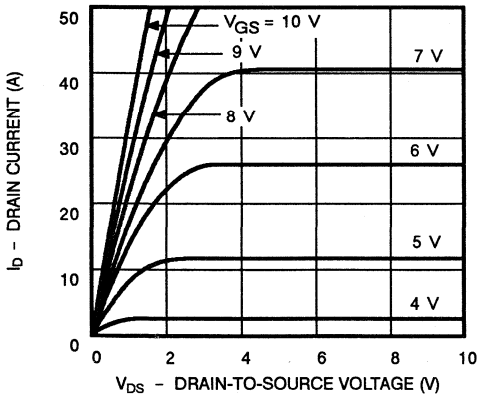


Figure 2. Transfer Characteristics

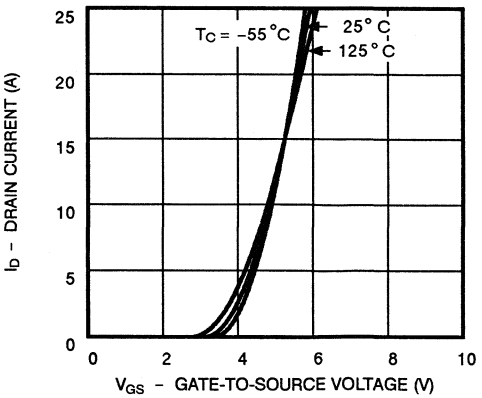


Figure 3. Transconductance

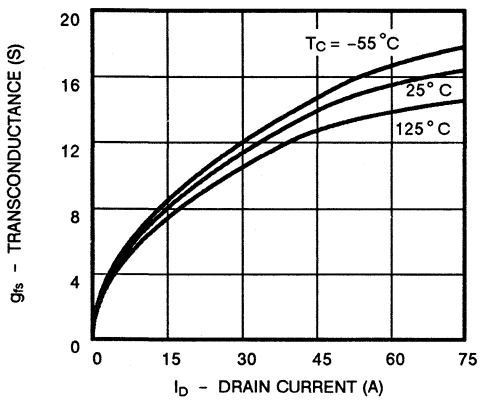


Figure 4. On-Resistance

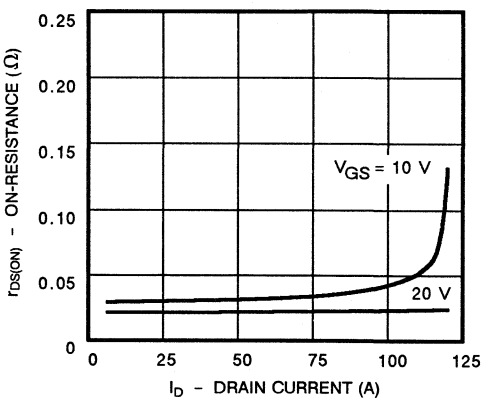


Figure 5. Capacitance

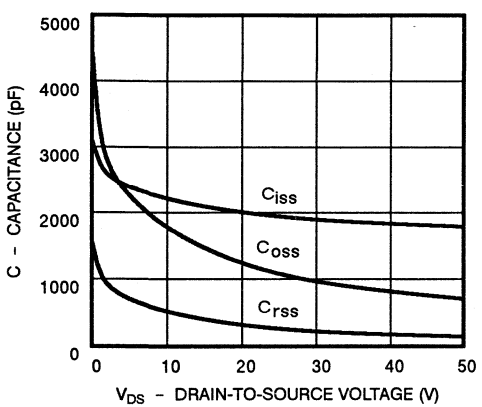
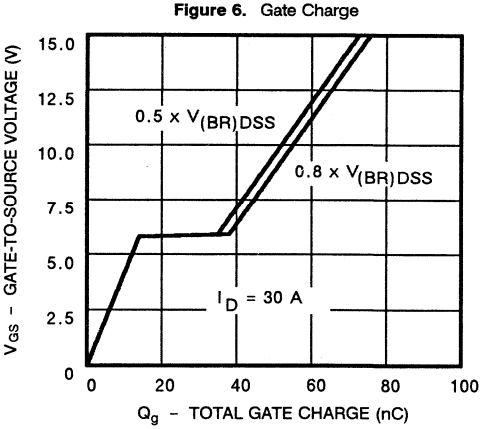


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

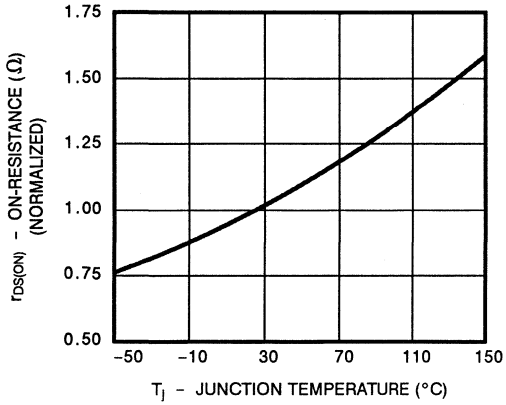
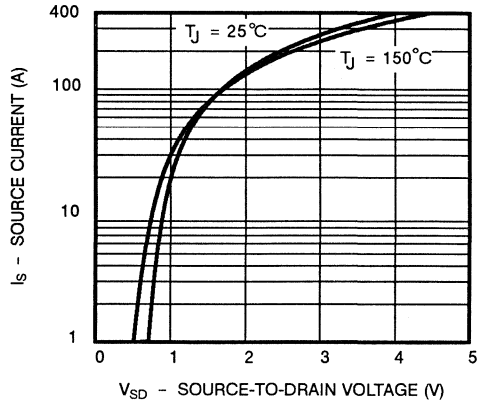


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

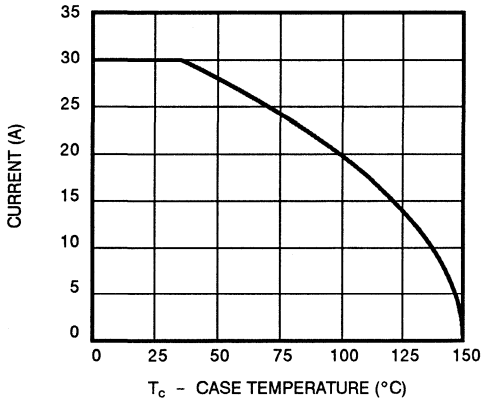
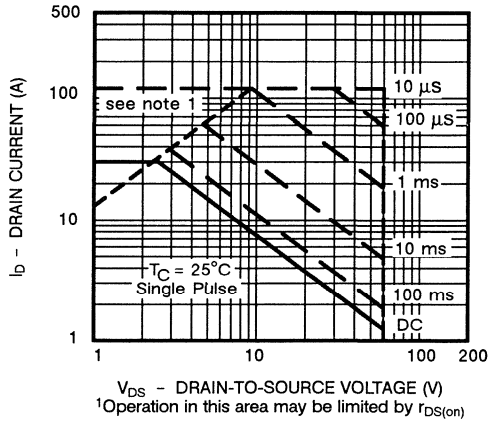
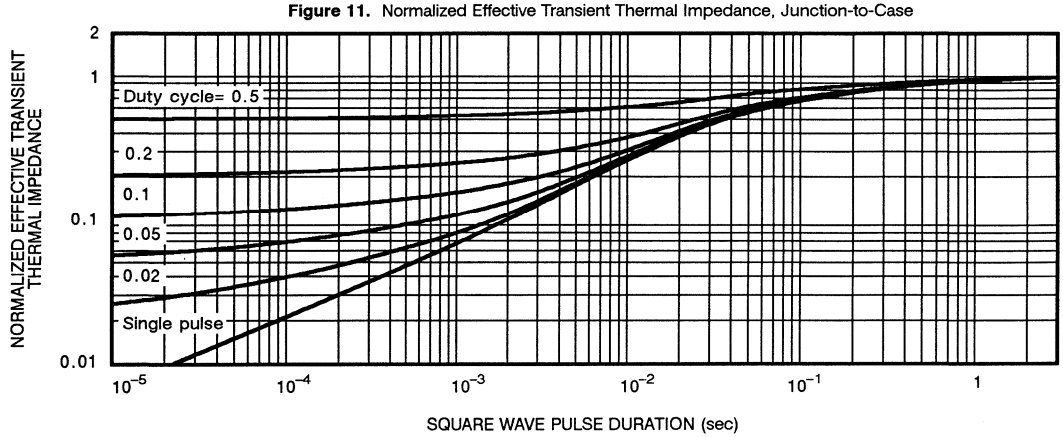


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

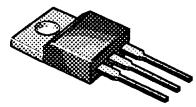
BUZ11A

N-Channel Enhancement Mode Transistor

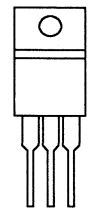
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
50	0.060	25

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		17	
Pulsed Drain Current[1]		I_{DM}	100	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		75	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.1	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		25		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A	0.050		0.060	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	0.080		0.10	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 15 A	10.0	4.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1050		2000	pF
Output Capacitance	C_{oss}		500		1100	
Reverse Transfer Capacitance	C_{rss}		125		400	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	27		50	nC
Gate-Source Charge[2]	Q_{gs}		8			
Gate-Drain Charge[2]	Q_{gd}		15			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω	20		45	ns
Rise Time[2]	t_r		50		110	
Turn-Off Delay Time[2]	$t_{d(off)}$		60		230	
Fall Time[2]	t_f		55		170	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				25	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.4	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	65			ns
Reverse Recovery Charge	Q_{rr}		0.12			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

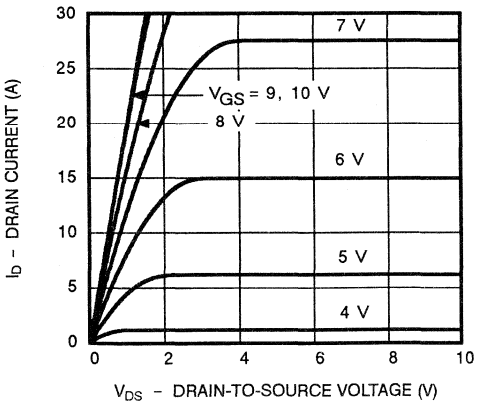


Figure 2. Transfer Characteristics

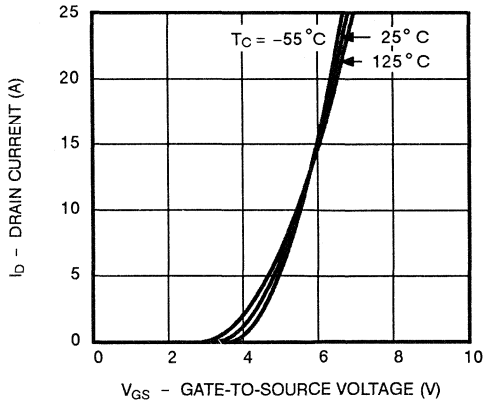


Figure 3. Transconductance

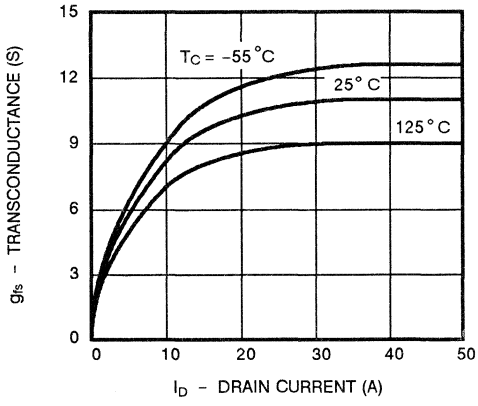


Figure 4. On-Resistance

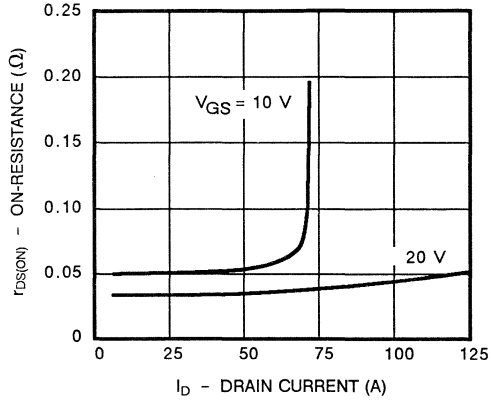


Figure 5. Capacitance

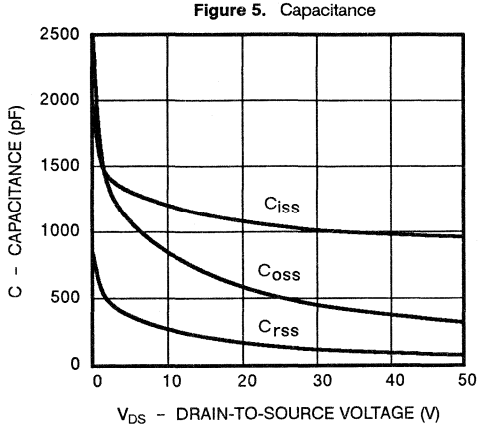
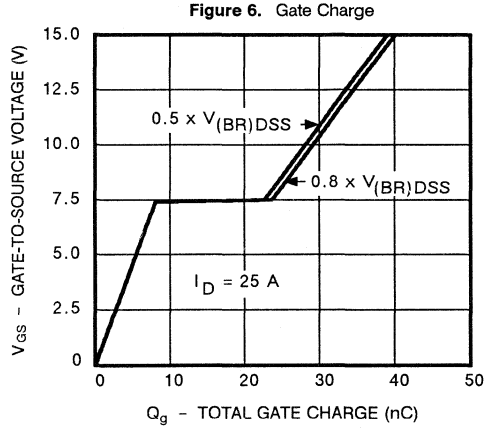


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

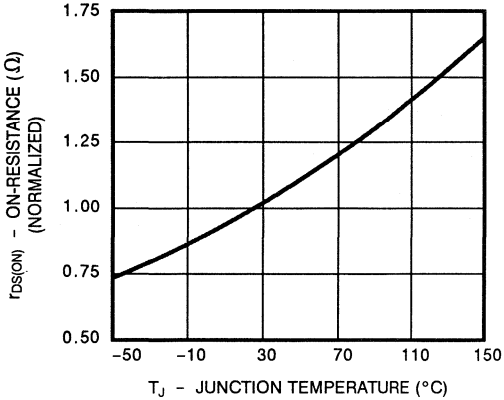
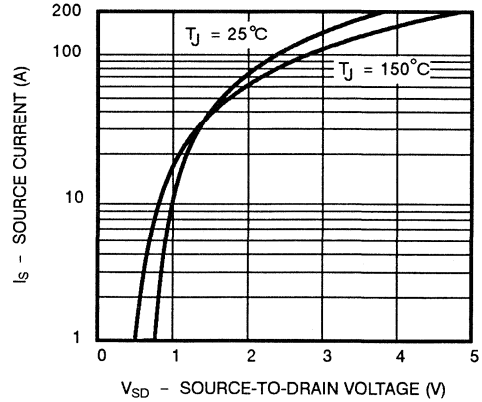


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

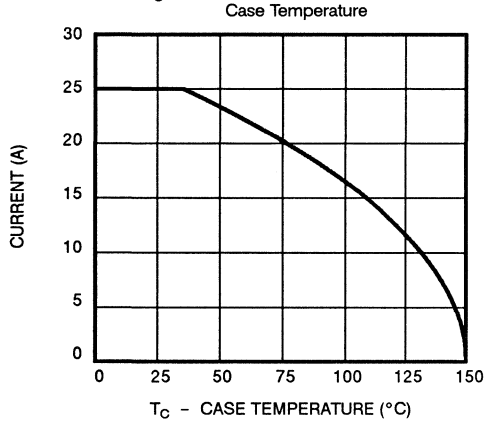
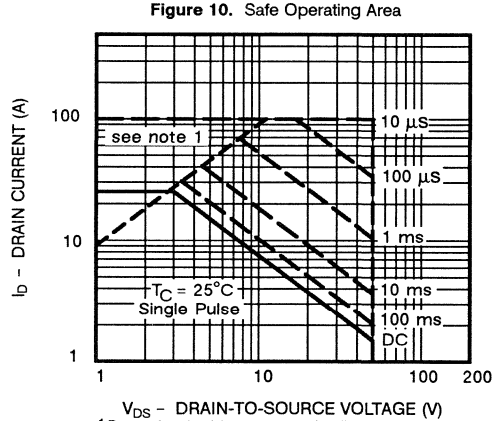
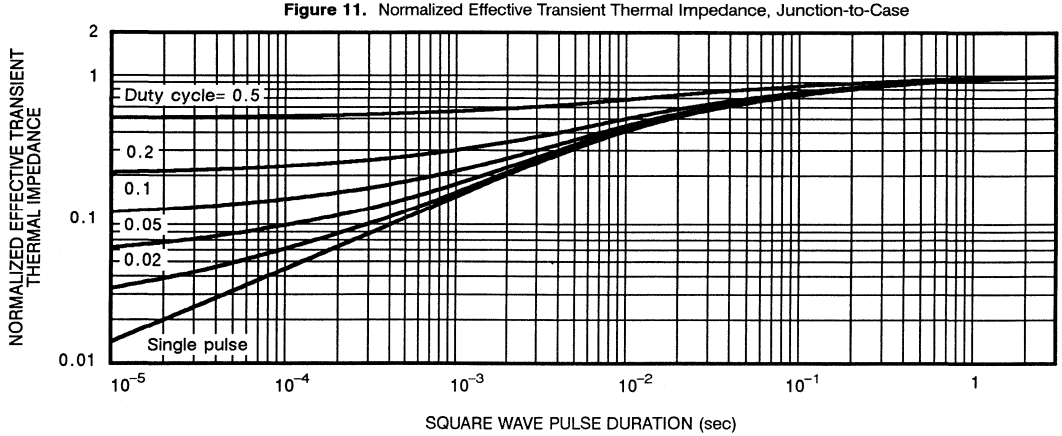


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

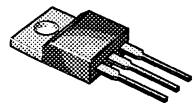
BUZ71, BUZ71A

N-Channel Enhancement Mode Transistors

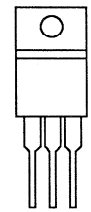
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
BUZ71	50	0.10	14
BUZ71A	50	0.12	13

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS BUZ71	LIMITS BUZ71A	UNITS
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	14	13	A
	T_C = 100°C		9	8.2	
Pulsed Drain Current[1]		I_{DM}	56	48	
Power Dissipation	T_C = 25°C	P_D	40	40	W
	T_C = 100°C		16	16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		3.1	K/W
Junction-to-Ambient	R_{thJA}		75	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.1	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	BUZ71 BUZ71A	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		14 13		A
Drain-Source On-State Resistance[1]	BUZ71 BUZ71A	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 6 A	0.07 0.10		0.10 0.12	Ω
	BUZ71 BUZ71A		V_{GS} = 10 V, I_D = 6 A T_J = 125°C	0.13 0.17		0.18 0.20	
Forward Transconductance[1]		g_{fs}	V_{DS} = 15 V, I_D = 6 A	8.0	3.0		S
DYNAMIC							
Input Capacitance		C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	400		650	pF
Output Capacitance		C_{oss}		150		450	
Reverse Transfer Capacitance		C_{rss}		35		280	
Total Gate Charge[2]		Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A	14		30	nC
Gate-Source Charge[2]		Q_{gs}		3			
Gate-Drain Charge[2]		Q_{gd}		4			
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 3 A, V_{GEN} = 10 V, R_G = 25 Ω	10		30	ns
Rise Time[2]		t_r		20		85	
Turn-Off Delay Time[2]		$t_{d(off)}$		40		90	
Fall Time[2]		t_f		25		110	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	BUZ71 BUZ71A	I_S				14 13	A
Pulsed Current[3]	BUZ71 BUZ71A	I_{SM}				56 48	
Forward Voltage[1]	BUZ71 BUZ71A	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.8 2.2	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	120			ns
Reverse Recovery Charge		Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

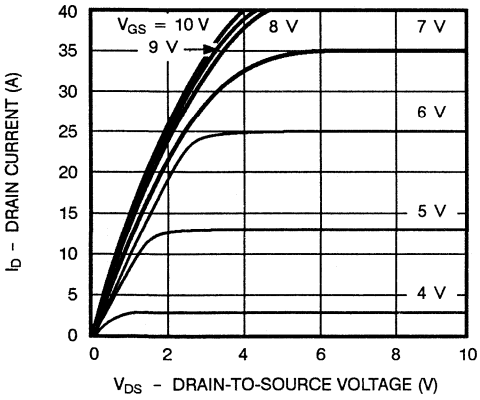


Figure 2. Transfer Characteristics

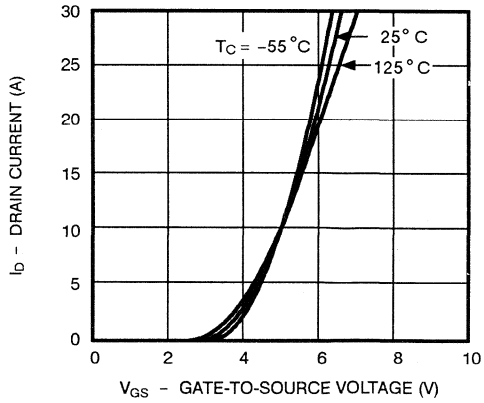


Figure 3. Transconductance

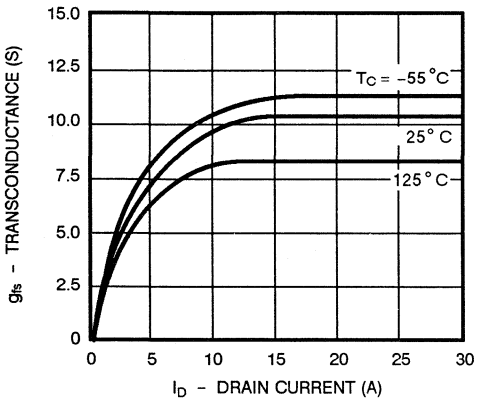


Figure 4. On-Resistance

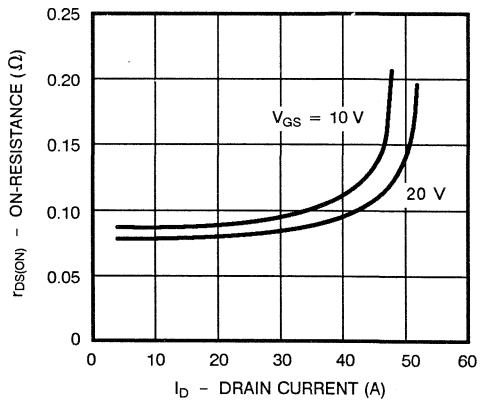


Figure 5. Capacitance

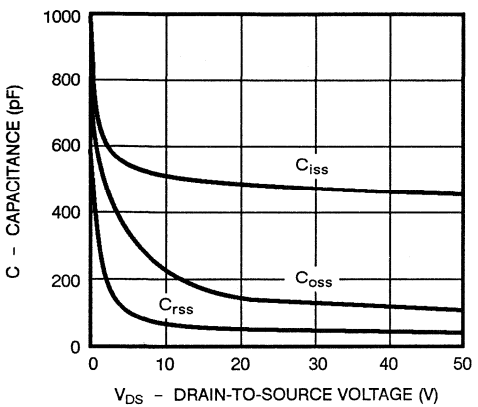
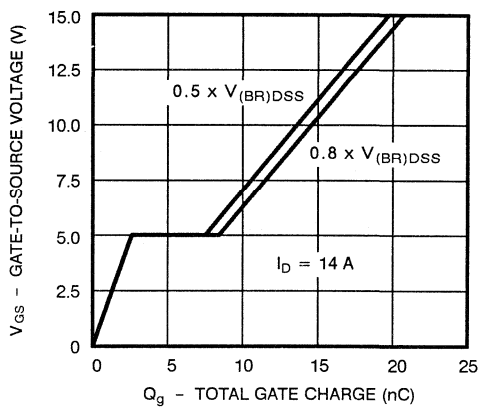


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

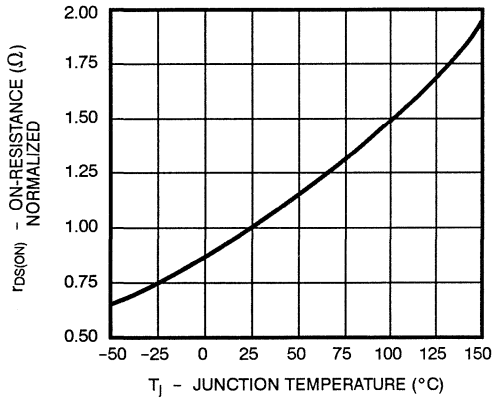
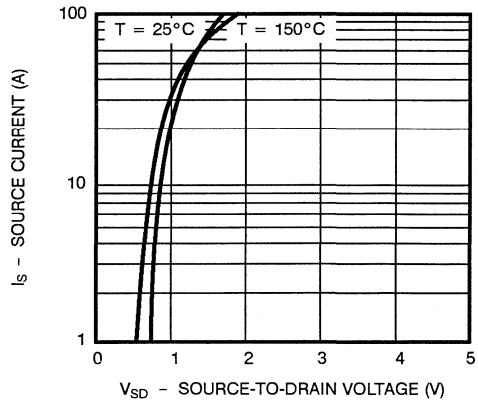


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

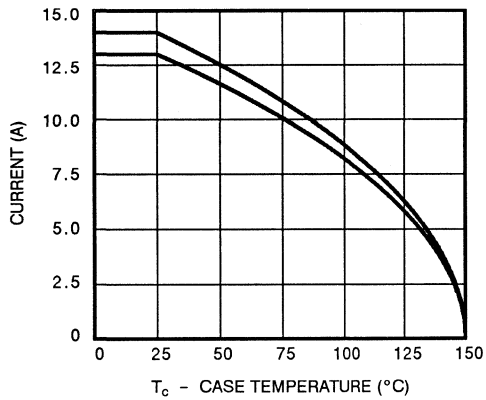
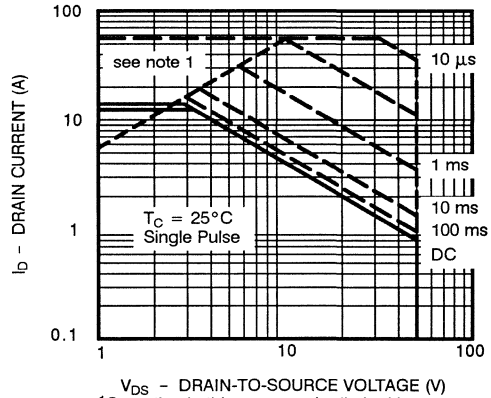
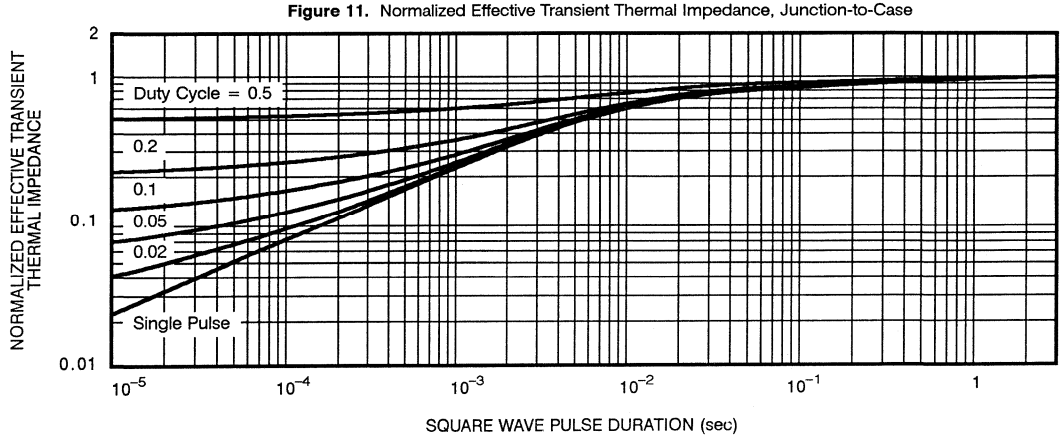


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

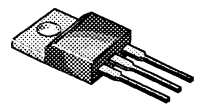
Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



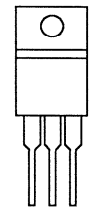
BUZ171

P-Channel Enhancement Mode Transistor

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-50	0.40	-7.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.5	
Pulsed Drain Current[2]		I_{DM}	28	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_C = 100°C		16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		3.1	K/W
Junction-to-Ambient	R_{thJA}		75	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.1	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		7.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 4.5 A	0.24		0.40	Ω
		V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C	0.40		0.72	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A	2.8	1.5		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	600		1200	pF
Output Capacitance	C_{oss}		325		500	
Reverse Transfer Capacitance	C_{rss}		100		230	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7 A	12		20	nC
Gate-Source Charge[2]	Q_{gs}		3.6			
Gate-Drain Charge[2]	Q_{gd}		8.2			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.9 A, V_{GEN} = 10 V, R_G = 25 Ω	10		30	ns
Rise Time[2]	t_r		50		95	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		90	
Fall Time[2]	t_f		50		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				7.0	A
Pulsed Current[3]	I_{SM}				28	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	70			ns
Reverse Recovery Charge	Q_{rr}		0.15			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

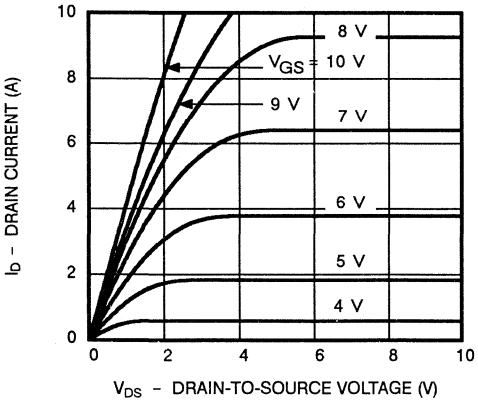


Figure 2. Transfer Characteristics

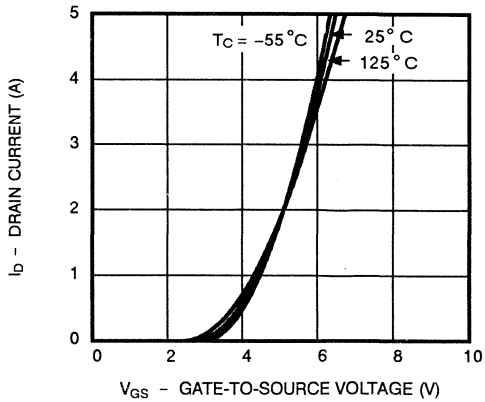


Figure 3. Transconductance

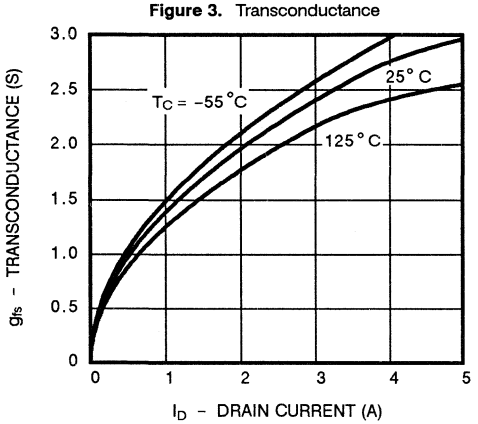


Figure 4. On-Resistance

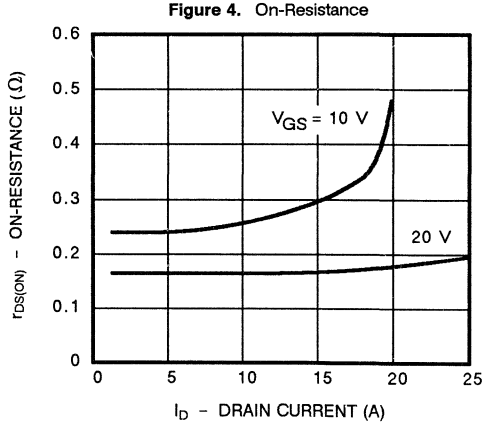


Figure 5. Capacitance

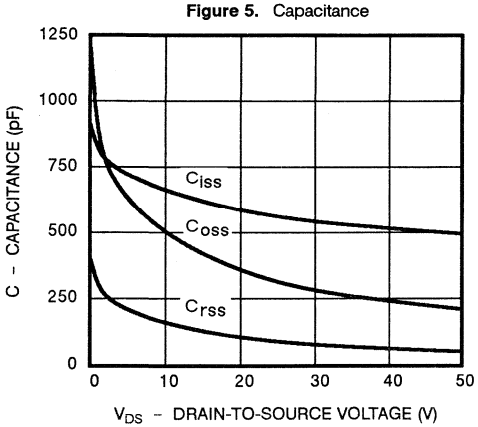
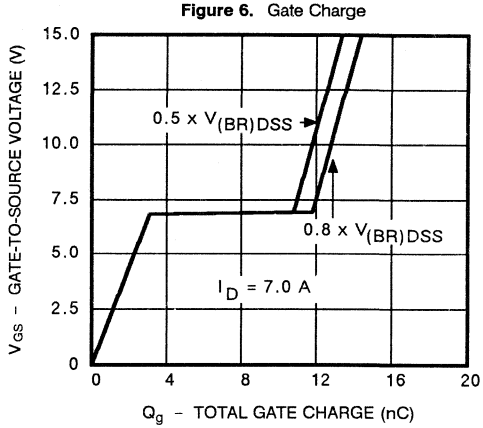


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

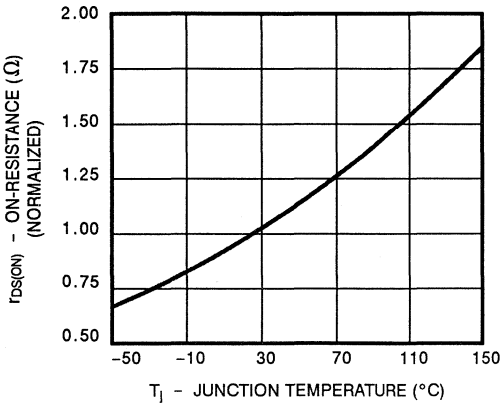
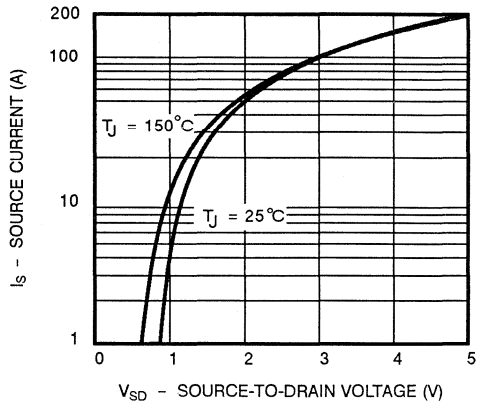


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

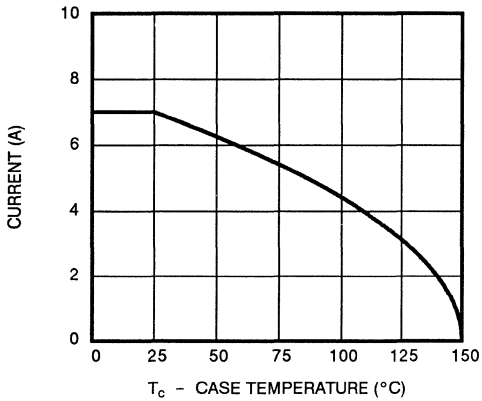
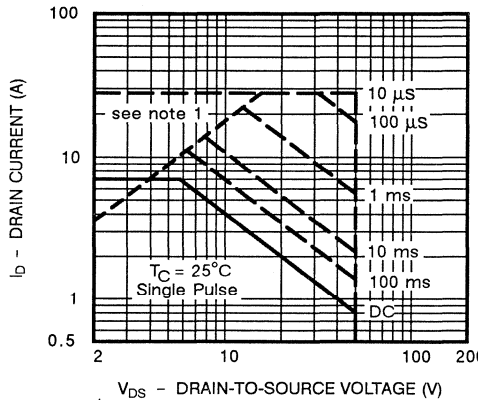
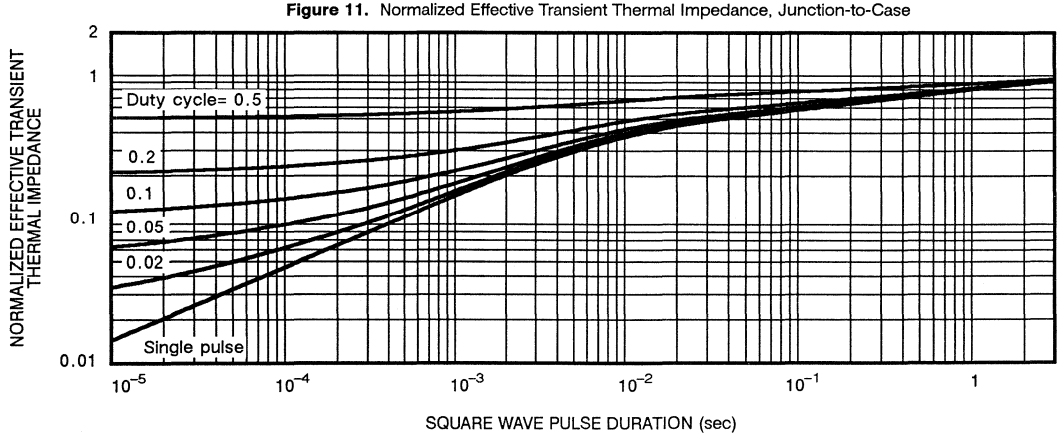


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

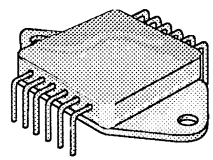
Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



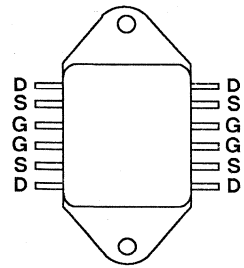
MOD100A/100B/100C

4 N-Channel Enhancement Mode Transistors

HERMETIC MODULE



TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	LEADFORM OPTION
MOD100A	100	0.08	21	Straight
MOD100B	100	0.08	21	Bent Down
MOD100C	100	0.08	21	Bent Up

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SINGLE DIE	ALL DIE	
Drain-Source Voltage		V_{DS}	100	100	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		21	70	
Pulsed Drain Current[1]		I_{DM}	125	440	
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYP	MAXIMUM		UNITS
			SINGLE	ALL	
Junction-to-Case	R_{thJC}		0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}		30	30	
Case-to-Sink	R_{thCS}	0.1			

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		21		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 20 A	0.070		0.080	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125°C	0.100		0.120	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	11.0	9.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2800		3200	pF
Output Capacitance	C_{oss}		1100		1500	
Reverse Transfer Capacitance	C_{rss}		400		500	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A	62		120	nC
Gate-Source Charge[2]	Q_{gs}		13			
Gate-Drain Charge[2]	Q_{gd}		29			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 24 V, R_L = 1.2 Ω, $I_D \simeq$ 20 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		35	ns
Rise Time[2]	t_r		30		100	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		125	
Fall Time[2]	t_f		20		100	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				21	A
Pulsed Current[3]	I_{SM}				125	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

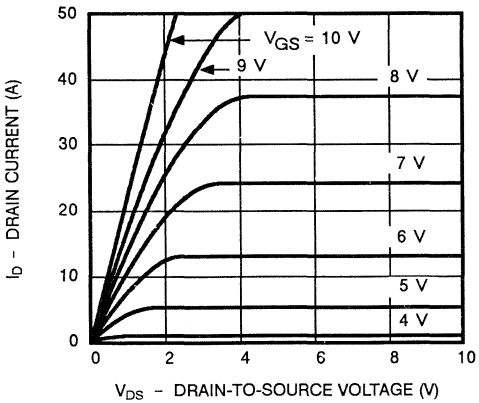


Figure 2. Transfer Characteristics

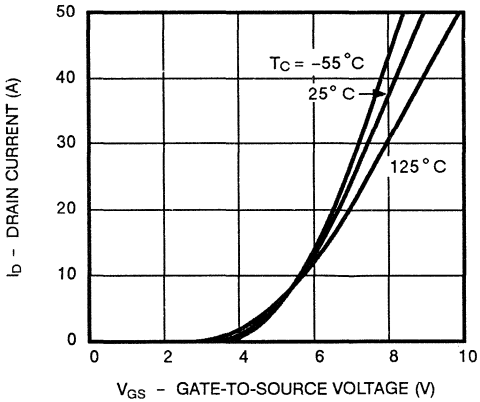


Figure 3. Transconductance

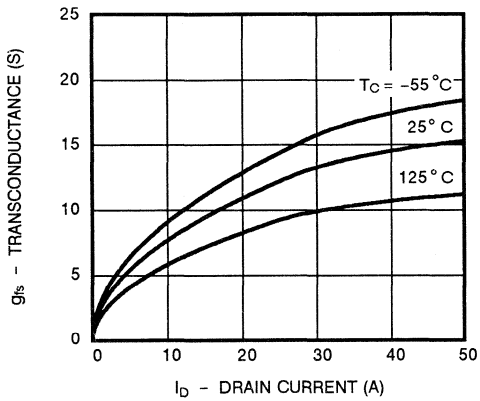


Figure 4. On-Resistance

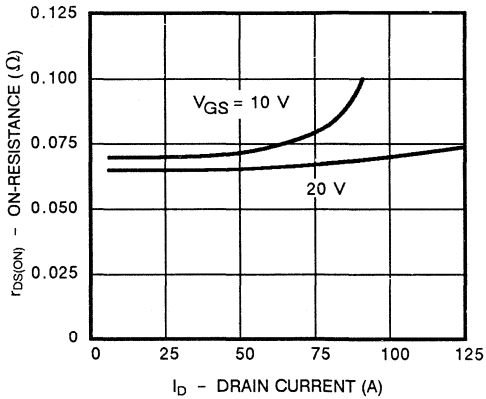


Figure 5. Capacitance

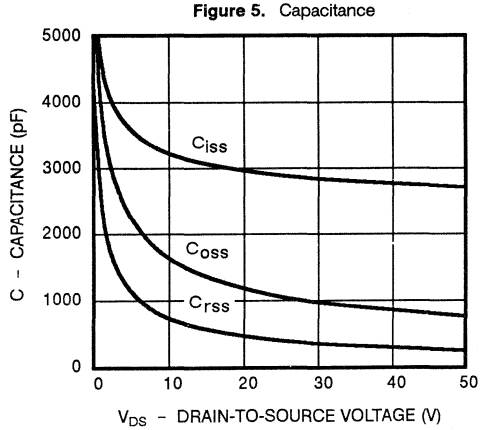
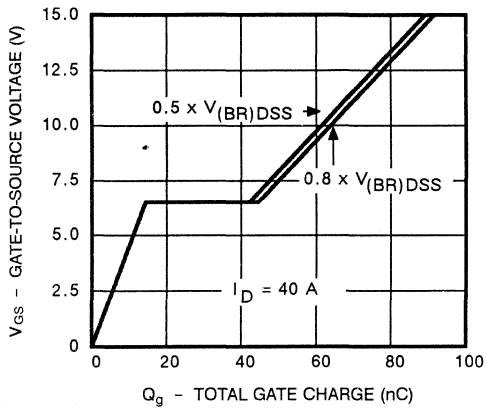


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

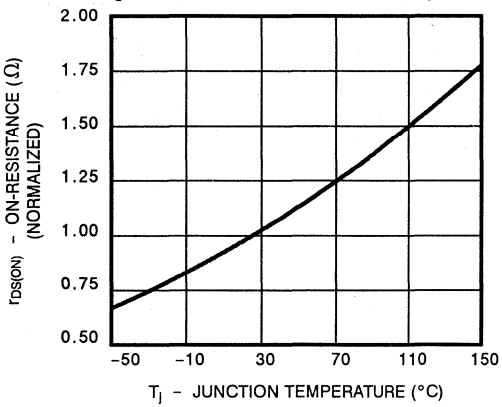
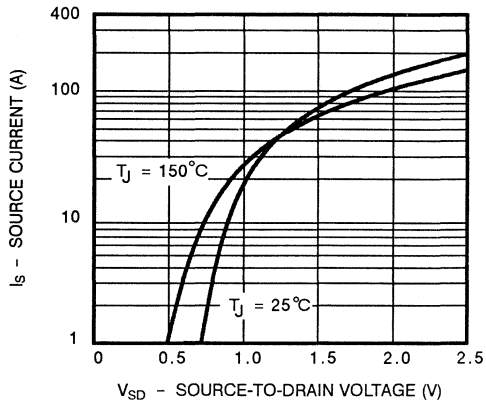


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

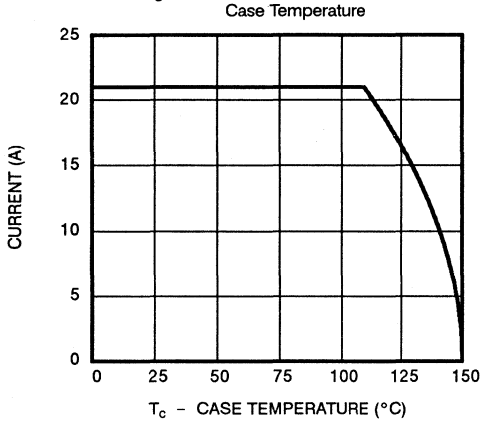
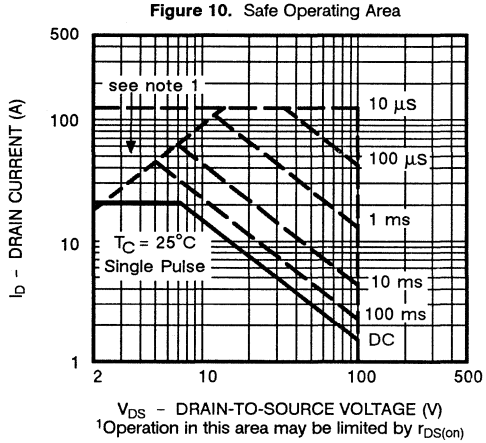
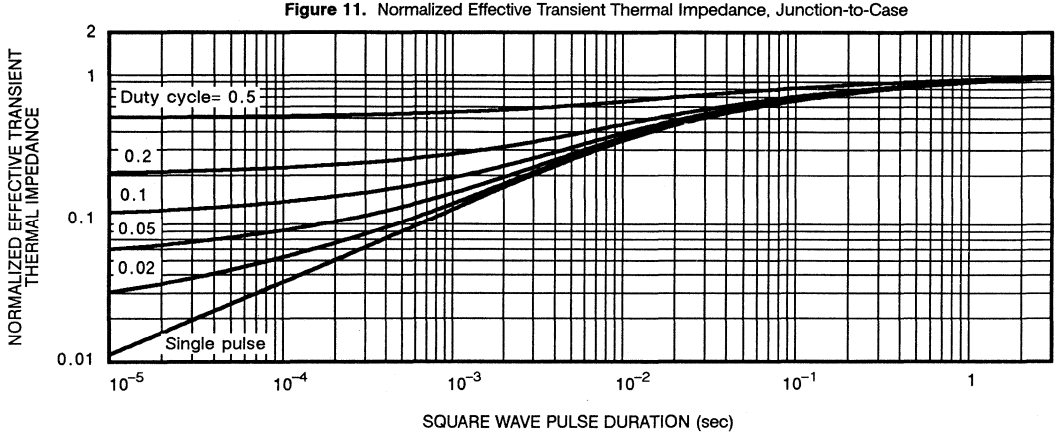


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

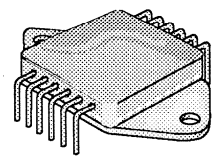


Siliconix incorporated

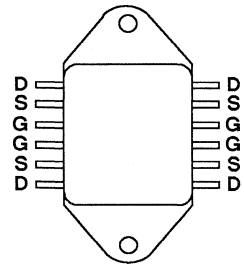
MOD200A/200B/200C

4 N-Channel Enhancement Mode Transistors

HERMETIC MODULE



TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	LEADFORM OPTION
MOD200A	200	0.11	21	Straight
MOD200B	200	0.11	21	Bent Down
MOD200C	200	0.11	21	Bent Up

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SINGLE DIE	ALL DIE	
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		17	56	
Pulsed Drain Current[1]		I_{DM}	100	360	
Avalanche Current (See Figure 9)		I_A	21	–	
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYP	MAXIMUM		UNITS
			SINGLE	ALL	
Junction-to-Case	R_{thJC}		0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}		30	30	
Case-to-Sink	R_{thCS}	0.1			

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		21		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 16 A	0.090		0.11	Ω
		V_{GS} = 10 V, I_D = 16 A, T_J = 125°C	0.150		0.175	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 16 A	13	8.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700		3200	pF
Output Capacitance	C_{oss}		850		1200	
Reverse Transfer Capacitance	C_{rss}		300		500	
Total Gate Charge[2]	Q_g	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 21 A	63		120	nC
Gate-Source Charge[2]	Q_{gs}		14			
Gate-Drain Charge[2]	Q_{gd}		32			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 95 V, R_L = 6.2 Ω, $I_D \simeq$ 16 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		35	ns
Rise Time[2]	t_r		30		100	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		125	
Fall Time[2]	t_f		20		100	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				21	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

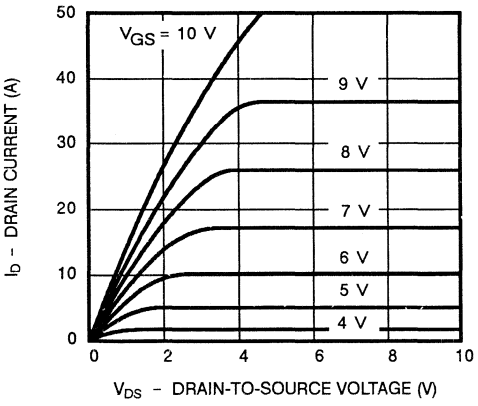


Figure 2. Transfer Characteristics

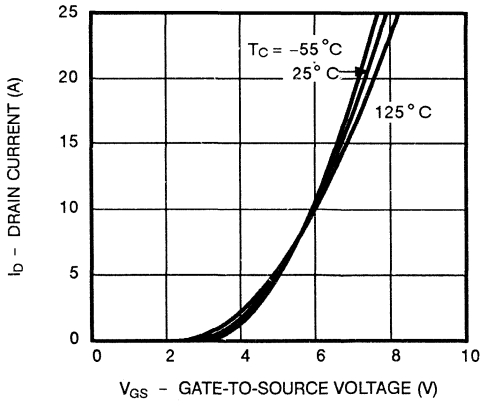


Figure 3. Transconductance

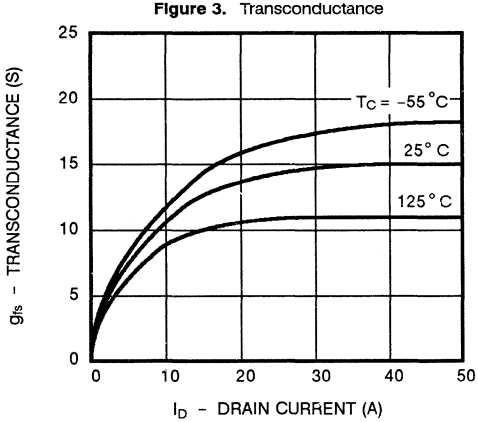


Figure 4. On-Resistance

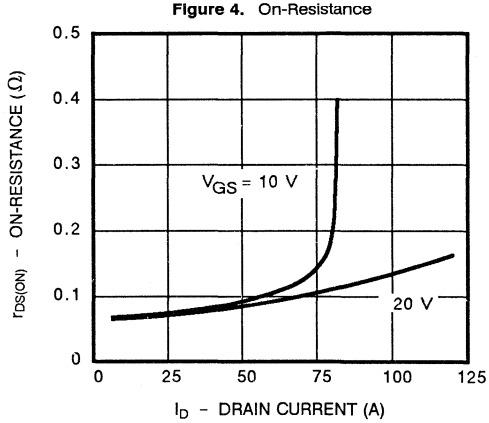


Figure 5. Capacitance

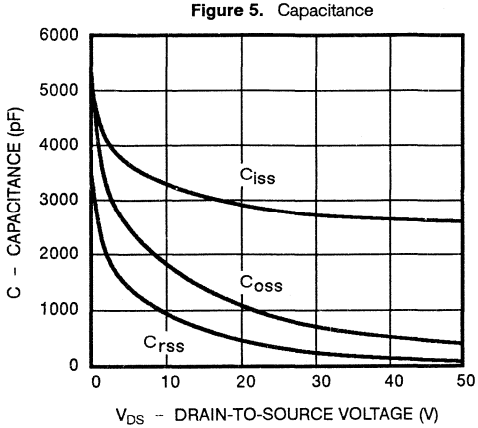
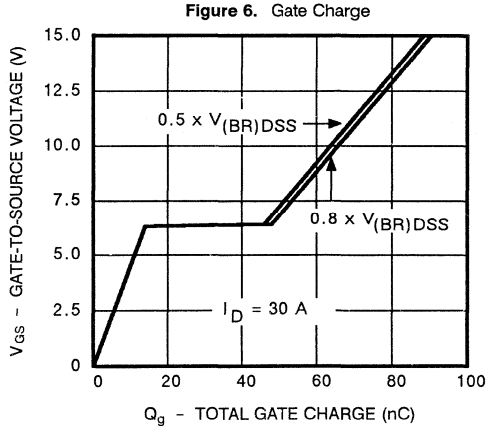


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

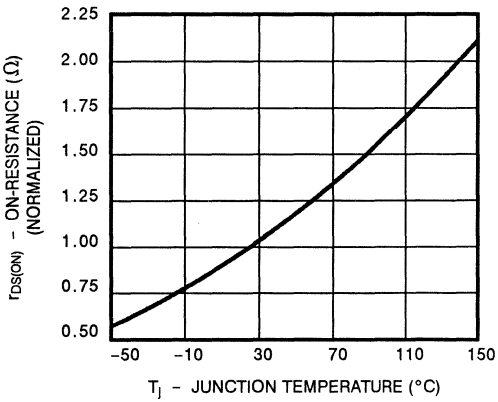
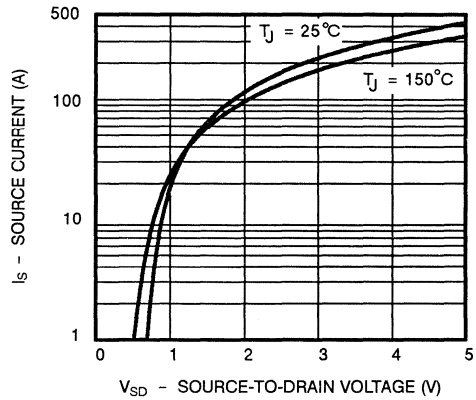


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

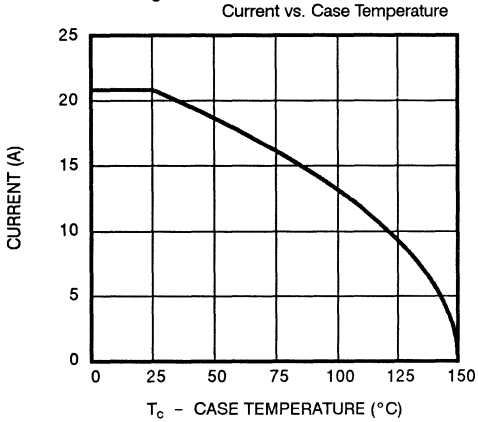
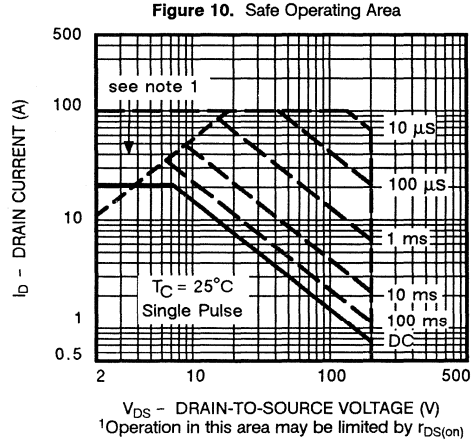
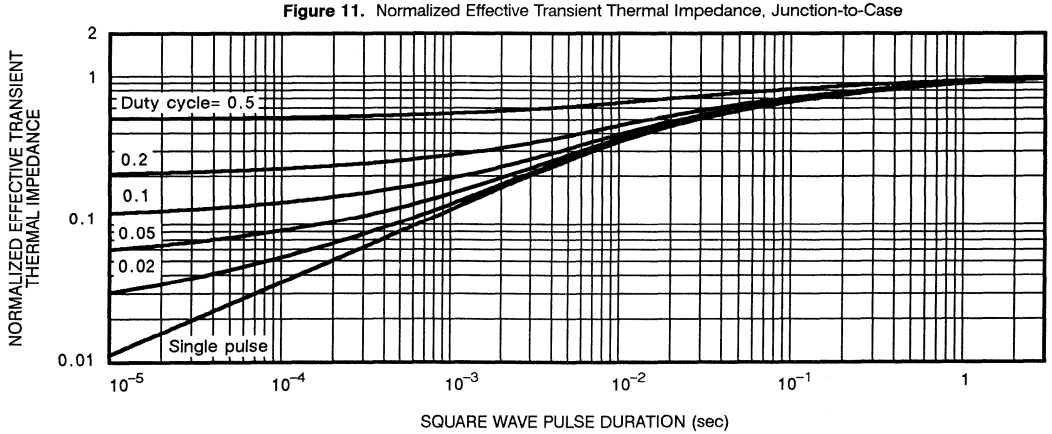


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

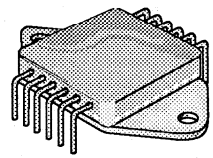
Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



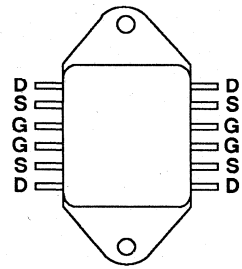
MOD400A/400B/400C

4 N-Channel Enhancement Mode Transistors

HERMETIC MODULE



TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	LEADFORM OPTION
MOD400A	400	0.35	15	Straight
MOD400B	400	0.35	15	Bent Down
MOD400C	400	0.35	15	Bent Up

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SINGLE DIE	ALL DIE	
Drain-Source Voltage		V_{DS}	400	400	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	15	47	A
	T_C = 100°C		9	30	
Pulsed Drain Current[1]		I_{DM}	60	190	
Avalanche Current (See Figure 9)		I_A	15	–	
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYP	MAXIMUM		UNITS
			SINGLE	ALL	
Junction-to-Case	R_{thJC}		0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}		30	30	
Case-to-Sink	R_{thCS}	0.1			

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		400		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		15		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 8 A	0.22		0.35	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C	0.40		0.62	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	8.5	8.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700		3200	pF
Output Capacitance	C_{oss}		450		600	
Reverse Transfer Capacitance	C_{rss}		160		200	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A	77		120	nC
Gate-Source Charge[2]	Q_{gs}		14			
Gate-Drain Charge[2]	Q_{gd}		39			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 180 V, R_L = 25 Ω, $I_D \simeq$ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω	14		35	ns
Rise Time[2]	t_r		30		65	
Turn-Off Delay Time[2]	$t_{d(off)}$		54		150	
Fall Time[2]	t_f		15		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				15	A
Pulsed Current[3]	I_{SM}				60	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	300			ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

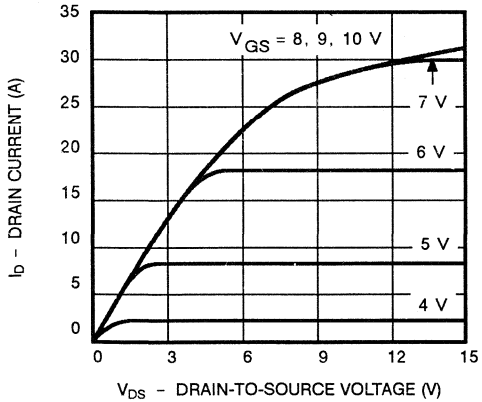


Figure 2. Transfer Characteristics

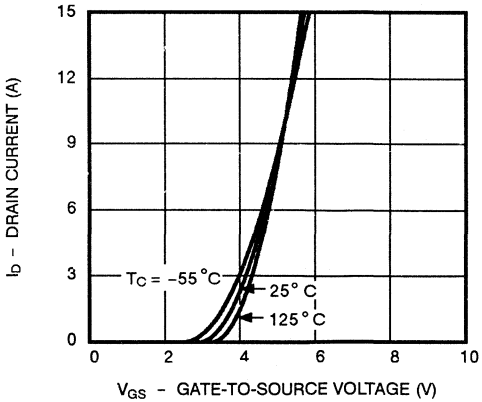


Figure 3. Transconductance

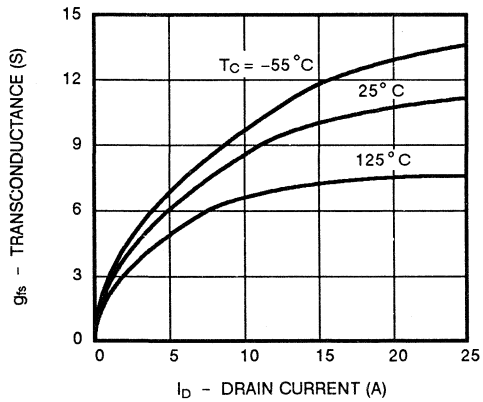


Figure 4. On-Resistance

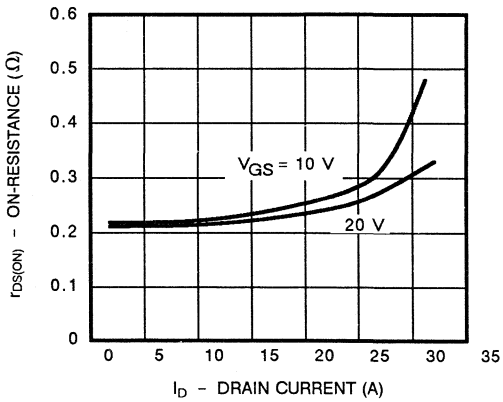


Figure 5. Capacitance

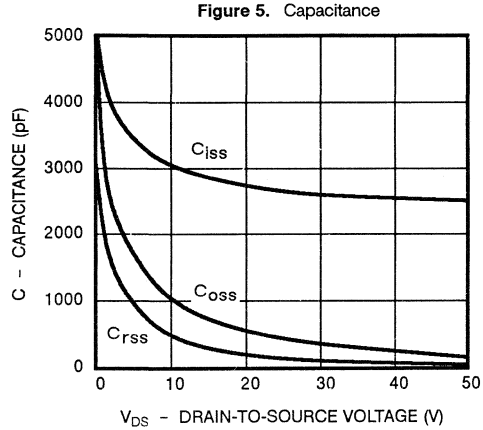
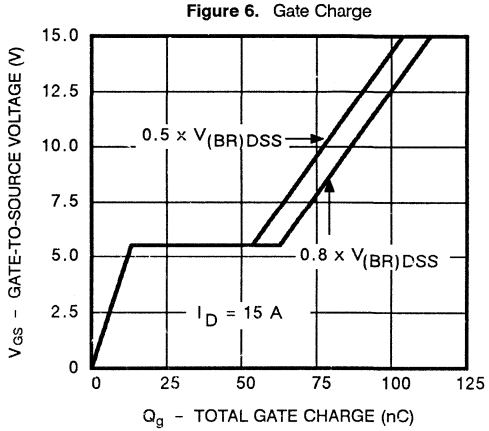


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

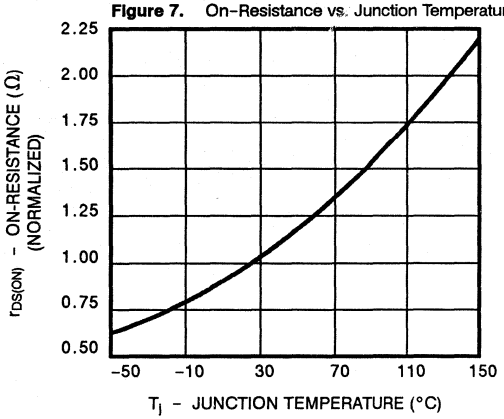
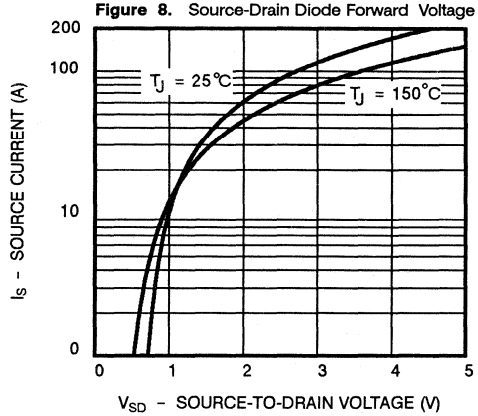


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

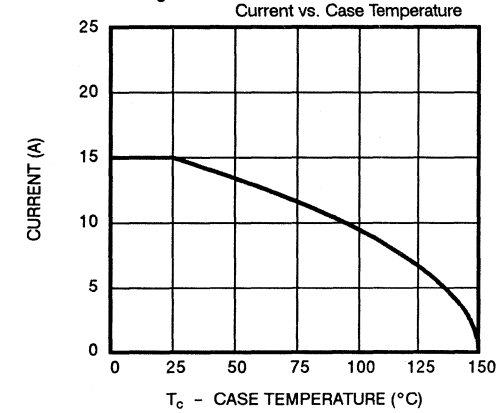
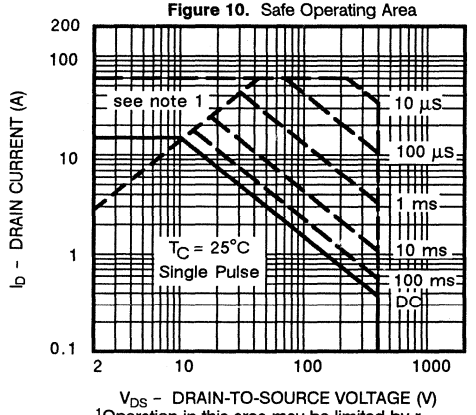
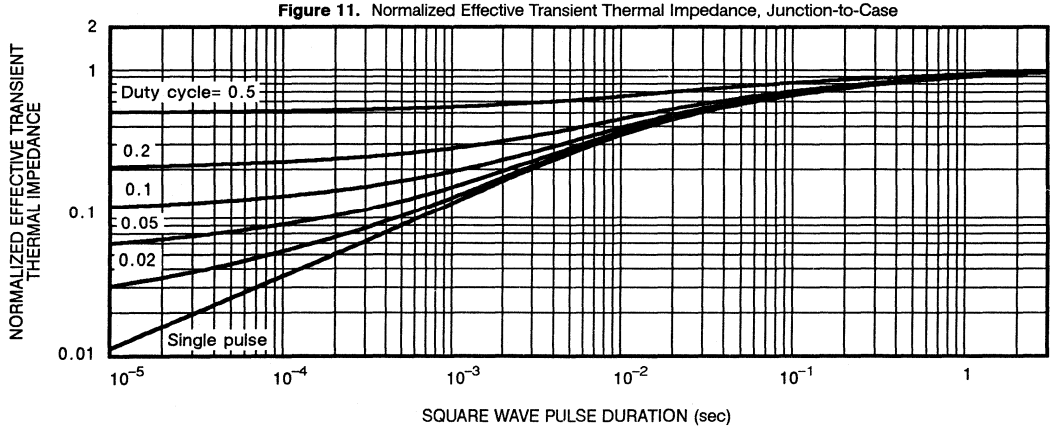


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

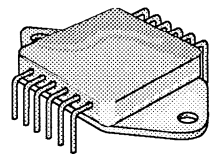
Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



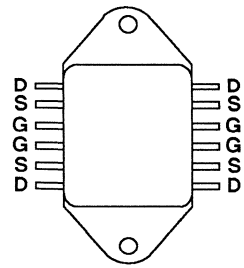
MOD500A/500B/500C

4 N-Channel Enhancement Mode Transistors

HERMETIC MODULE



TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	LEADFORM OPTION
MOD500A	500	0.43	13	Straight
MOD500B	500	0.43	13	Bent Down
MOD500C	500	0.43	13	Bent Up

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SINGLE DIE	ALL DIE	
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	13	41	A
	T_C = 100°C		8	26	
Pulsed Drain Current[1]		I_{DM}	52	164	
Avalanche Current (See Figure 9)		I_A	13	–	
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYP	MAXIMUM		UNITS
			SINGLE	ALL	
Junction-to-Case	R_{thJC}		0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}		30	30	
Case-to-Sink	R_{thCS}	0.1			

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		13		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7 A	0.33		0.43	Ω
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	0.66		0.88	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7 A	9.0	6.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700		3200	pF
Output Capacitance	C_{oss}		410		600	
Reverse Transfer Capacitance	C_{rss}		140		200	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A	75		120	nC
Gate-Source Charge[2]	Q_{gs}		12			
Gate-Drain Charge[2]	Q_{gd}		35			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 210 V, R_L = 30 Ω, $I_D \simeq$ 7 A, V_{GEN} = 10 V, R_G = 4.7 Ω	13		35	ns
Rise Time[2]	t_r		26		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		55		150	
Fall Time[2]	t_f		17		70	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				13	A
Pulsed Current[3]	I_{SM}				52	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	300			ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

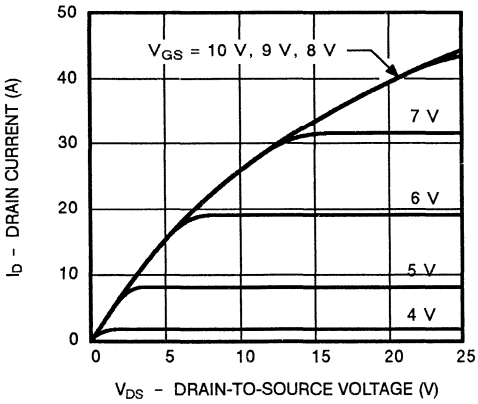


Figure 2. Transfer Characteristics

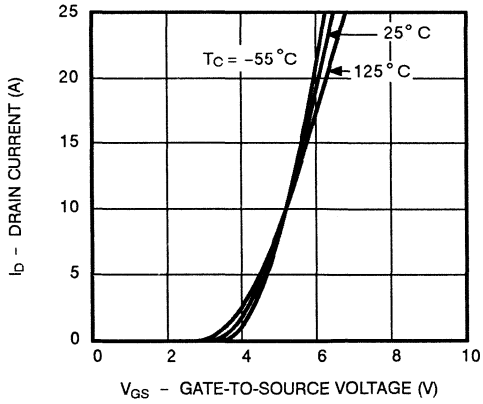


Figure 3. Transconductance

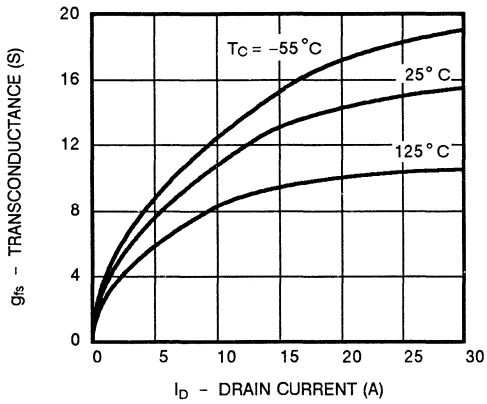


Figure 4. On-Resistance

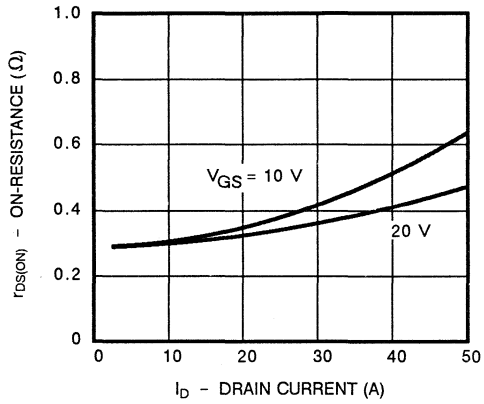


Figure 5. Capacitance

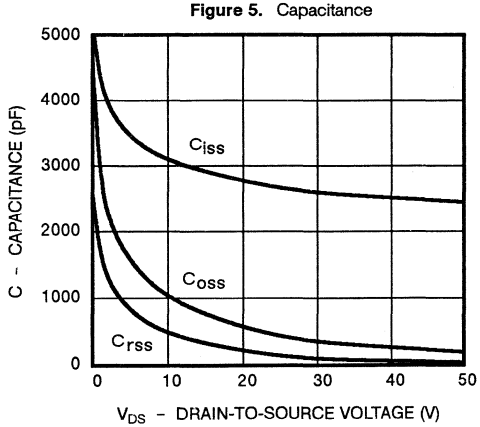
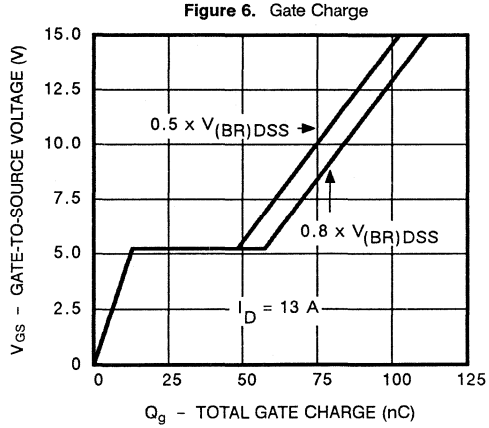


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

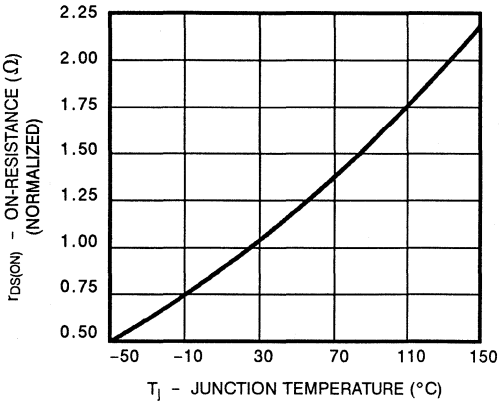
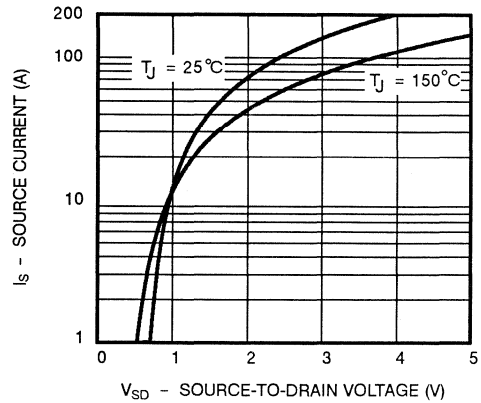


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

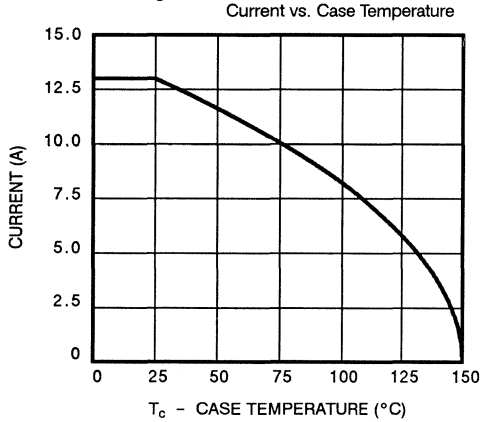
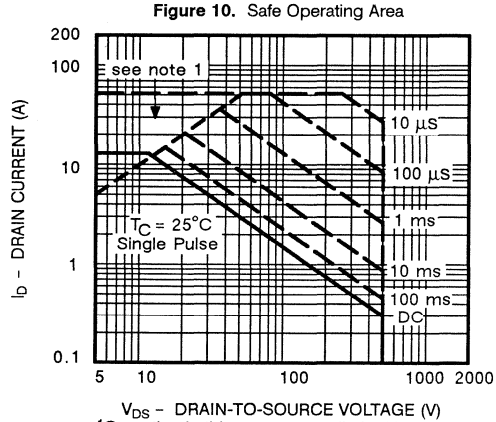
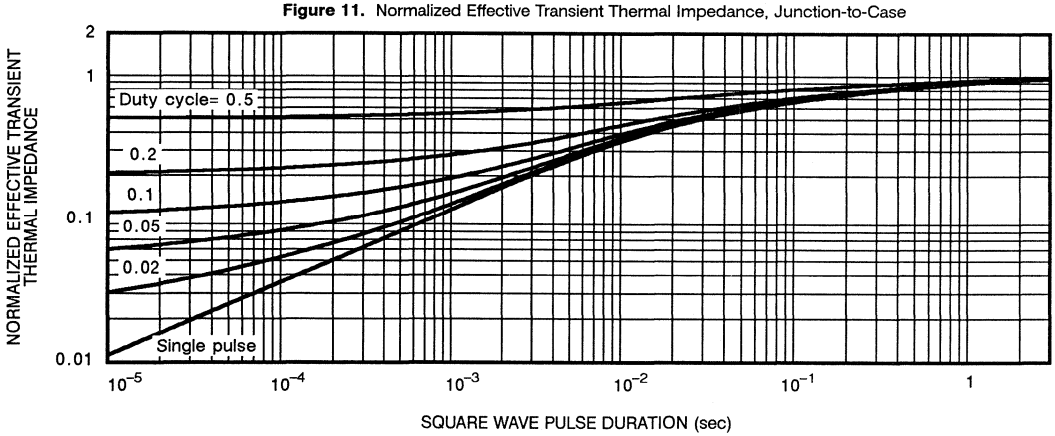


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



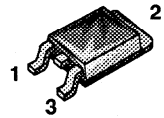
SMD10P05, SMU10P05

P-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

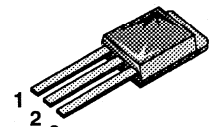
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)[1]
SMD10P05	-50	0.28	-10
SMU10P05	-50	0.28	-10

D-PAK (TO-252)



SMD10P05

THROUGH HOLE D-PAK (TO-251)



SMU10P05

1 GATE
2 DRAIN (TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SMD10P05 SMU10P05	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[3]	T_A = 25°C	I_D	2.0[3]	A
	T_A = 100°C		1.3[3]	
Pulsed Drain Current[4]		I_{DM}	16	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[3]	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}	2.3	3.0	K/W
Junction-to-Ambient Free Air, PC Board Mount[3]	R_{thJA}	50	60	
Junction-to-Ambient Free Air, Vertical Mount		50	60	

[1]Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see absolute maximum ratings and Figures 9, 10 and 11).
[2]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[3]Surface mounted on PC board or mounted vertically in free air.
[4]Maximum current limited by package.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)
P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x BV_{DSS}			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		10		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5 A	0.25		0.28	Ω
		V_{GS} = 10 V, I_D = 5 A, T_J = 125°C	0.4		0.50	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	1.4	1.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	530			pF
Output Capacitance	C_{oss}		325			
Reverse Transfer Capacitance	C_{rss}		85			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A	13		20	nC
Gate-Source Charge[2]	Q_{gs}		3.6		5.0	
Gate-Drain Charge[2]	Q_{gd}		9		12.0	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 3 Ω, I_D ≃ 10 A, V_{GEN} = 10 V, R_G = 25 Ω	10		30	ns
Rise Time[2]	t_r		50		95	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		90	
Fall Time[2]	t_f		50		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				2.0	A
Pulsed Current[3]	I_{SM}				24	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.3	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	70			ns
Reverse Recovery Charge	Q_{rr}		0.07			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

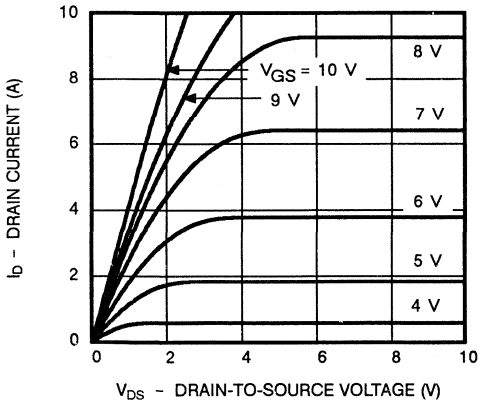


Figure 2. Transfer Characteristics

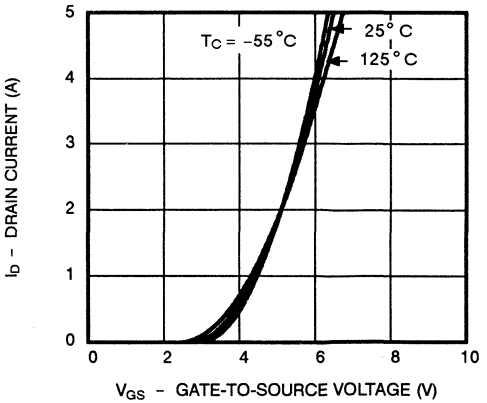


Figure 3. Transconductance

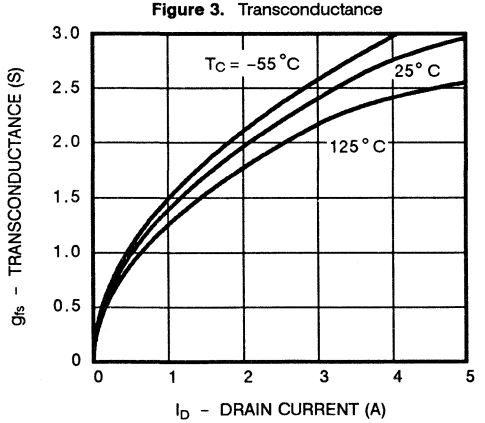


Figure 4. On-Resistance

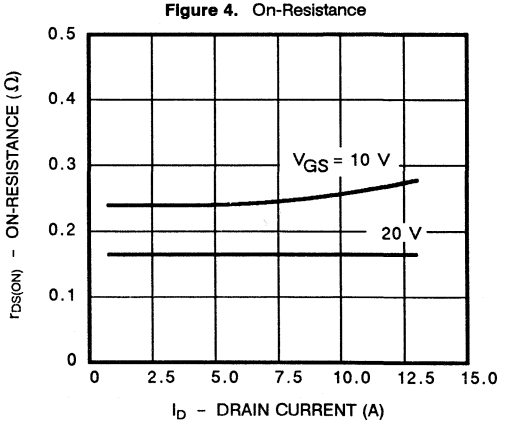


Figure 5. Capacitance

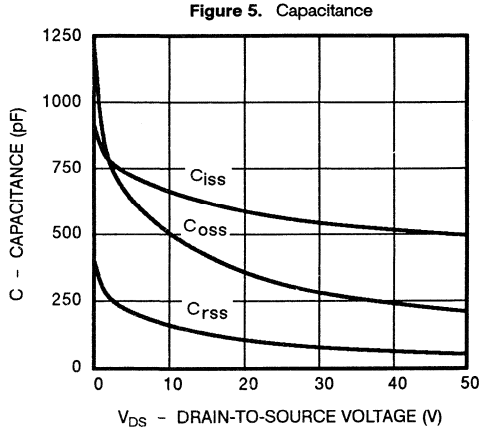
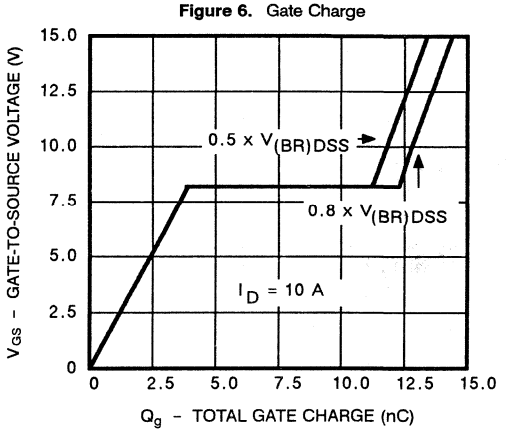


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

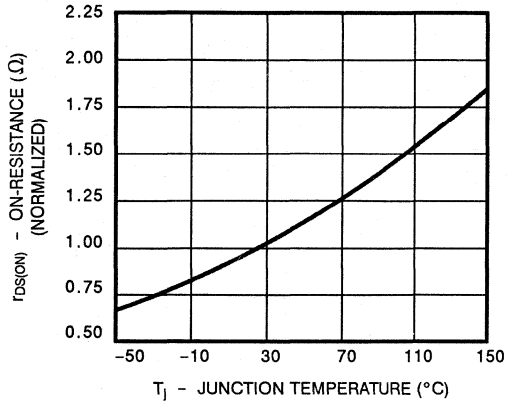
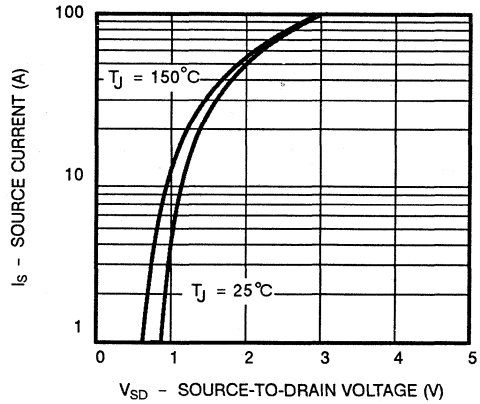


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Ambient Temperature

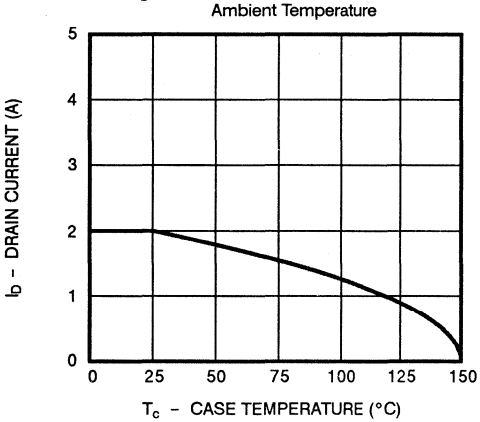
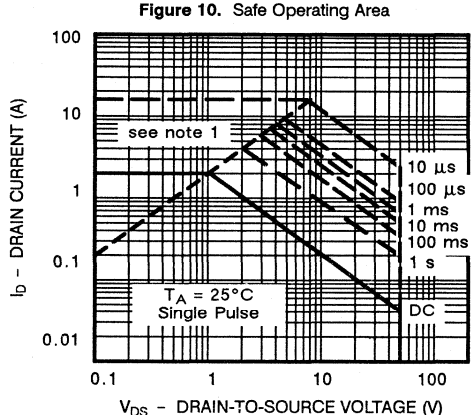
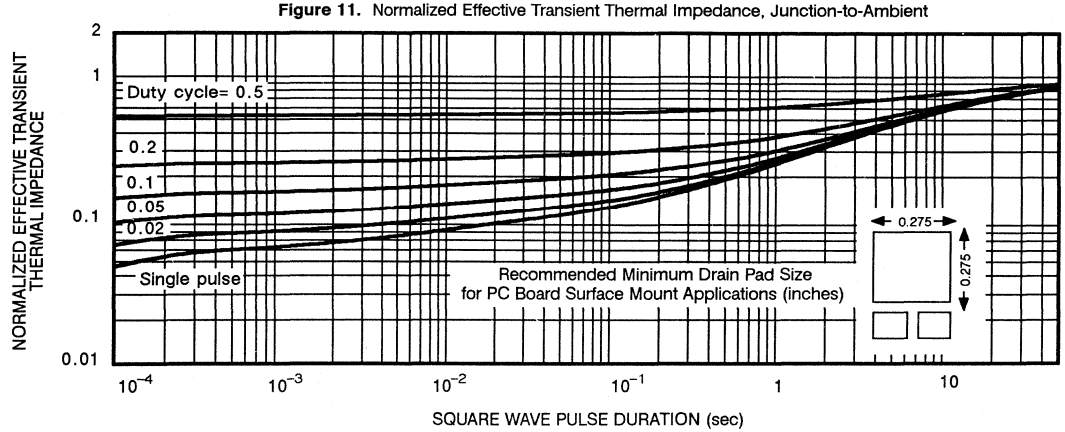


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Ambient



Siliconix incorporated

SMD10P05L

P-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)[1]
-50	0.28	-10

D-PAK
(TO-252)

1 GATE
2 DRAIN (TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[3]	T_A = 25°C	I_D	2.0[3]	A
	T_A = 100°C		1.3[3]	
Pulsed Drain Current[4]		I_{DM}	16	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[3]	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}	2.3	3.0	K/W
Junction-to-Ambient Free Air, PC Board Mount[3]	R_{thJA}	50	60	
Junction-to-Ambient Free Air, Vertical Mount		50	60	

[1]Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating.
[2]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[3]Surface mounted on PC board or mounted vertically in free air.
[4]Maximum current limited by package.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		0.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x BV_{DSS}, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		10		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5 A	0.25		0.28	Ω
		V_{GS} = 5 V, I_D = 1 A	0.25		0.30	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2 A	2	1.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	600			pF
Output Capacitance	C_{oss}		325			
Reverse Transfer Capacitance	C_{rss}		100			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2 A	26			nC
Gate-Source Charge[2]	Q_{gs}		2.2			
Gate-Drain Charge[2]	Q_{gd}		10			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	13		30	ns
Rise Time[2]	t_r		14		25	
Turn-Off Delay Time[2]	$t_{d(off)}$		180		250	
Fall Time[2]	t_f		140		200	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				2.0	A
Pulsed Current[3]	I_{SM}				24	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.3	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	70			ns
Reverse Recovery Charge	Q_{rr}		0.07			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

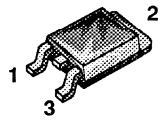
SMD15N05, SMU15N05

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

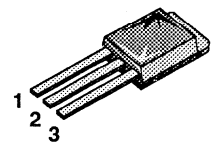
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)[1]
SMD15N05	50	0.10	15
SMU15N05	50	0.10	15

D-PAK
(TO-252)



SMD15N05

THROUGH HOLE
D-PAK
(TO-251)



SMU15N05

1 GATE
2 DRAIN (TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SMD15N05 SMU15P05	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[2]	T_A = 25°C	I_D	3.3[2]	A
	T_A = 100°C		1.9[2]	
Pulsed Drain Current[3]		I_{DM}	16	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[2]	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}	2.3	3.0	K/W
Junction-to-Ambient Free Air, PC Board Mount[2]	R_{thJA}	50	60	
Junction-to-Ambient Free Air, Vertical Mount		50	60	

[1]Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see absolute maximum ratings and Figures 9, 10 and 11).
[2]Surface mounted on PC board or mounted vertically in free air.
[3]Maximum current limited by package.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		15		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7.5 A	0.08		0.10	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C	0.13		0.18	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A	5.0	3.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	480			pF
Output Capacitance	C_{oss}		140			
Reverse Transfer Capacitance	C_{rss}		120			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A	13		24	nC
Gate-Source Charge[2]	Q_{gs}		2.5		4.0	
Gate-Drain Charge[2]	Q_{gd}		6		8.0	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1.67 Ω, I_D ≃ 15 A, V_{GEN} = 10 V, R_G = 25 Ω	15		30	ns
Rise Time[2]	t_r		50		85	
Turn-Off Delay Time[2]	$t_{d(off)}$		80		90	
Fall Time[2]	t_f		80		110	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				3.3	A
Pulsed Current[3]	I_{SM}				16	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1		2.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	65			ns
Reverse Recovery Charge	Q_{rr}		0.11			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

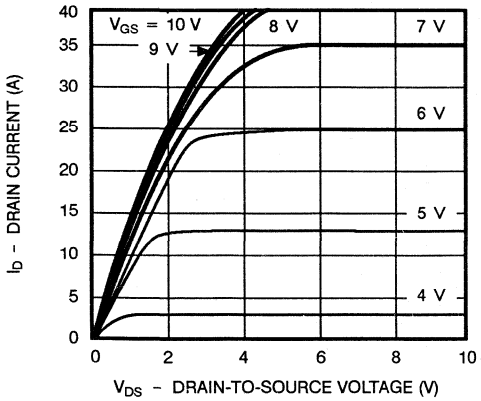


Figure 2. Transfer Characteristics

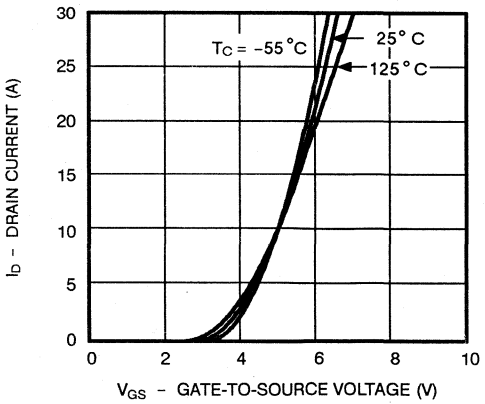


Figure 3. Transconductance

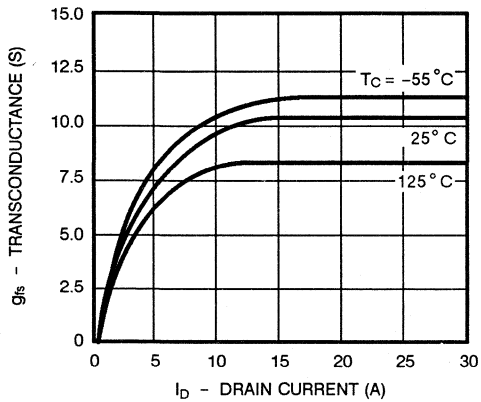


Figure 4. On-Resistance

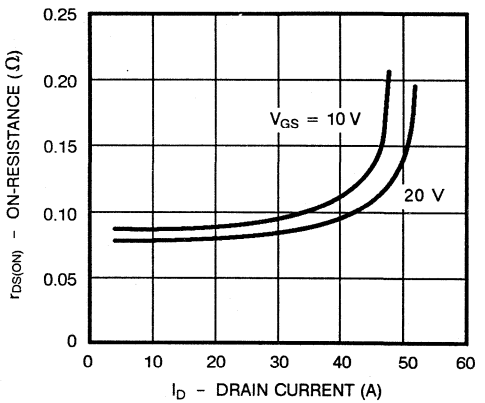


Figure 5. Capacitance

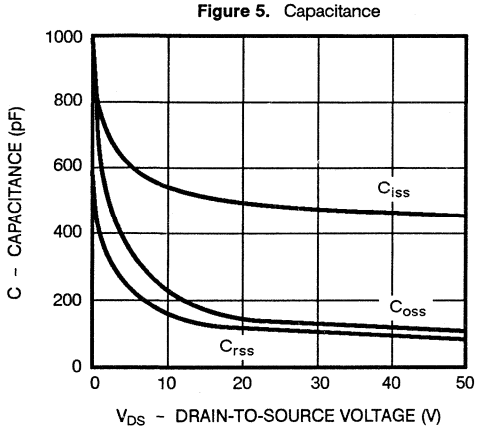
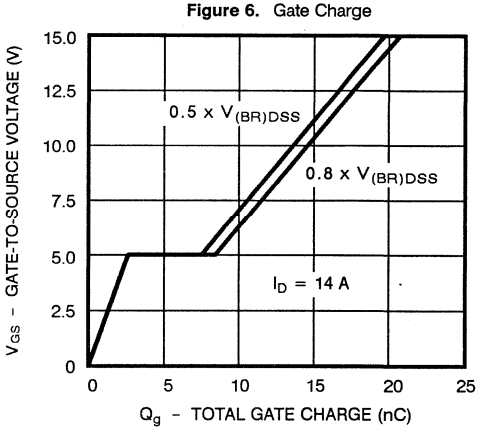


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

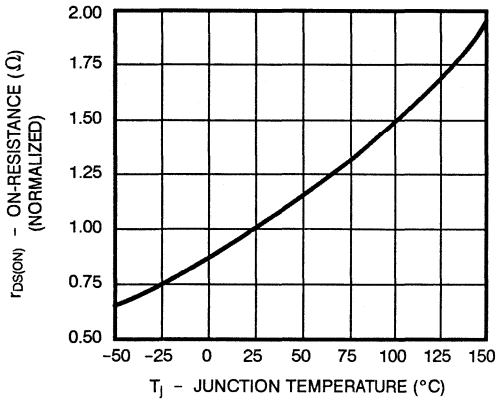
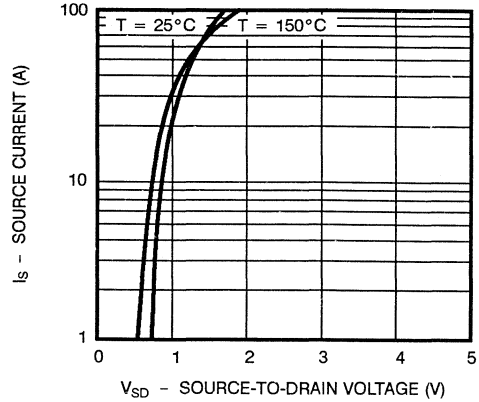


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Ambient Temperature

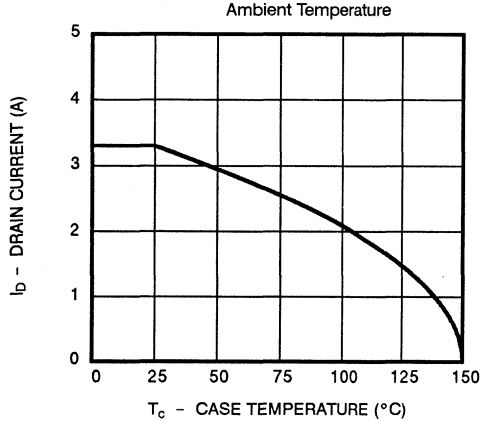
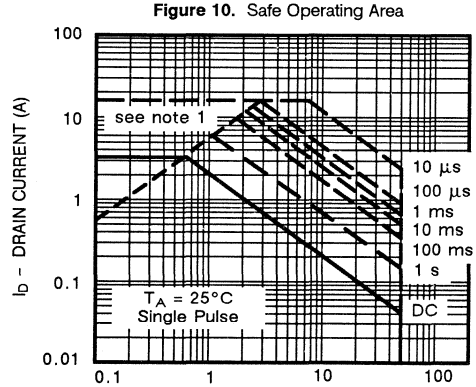
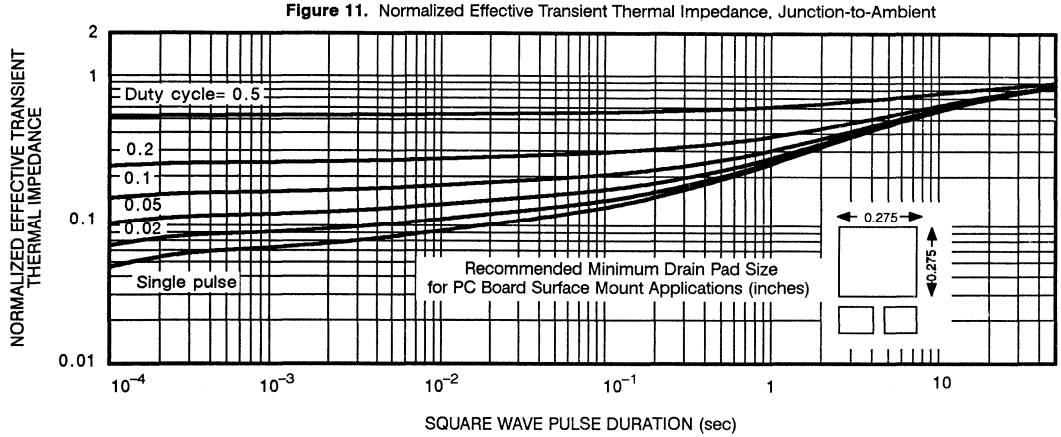


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Ambient

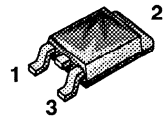


Siliconix incorporated

SMD25N05-45L

N-Channel Enhancement Mode Transistor
Logic Level

D-PAK
(TO-252)



1 GATE
2 DRAIN (TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
50	0.045	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		16	
Pulsed Drain Current[1]		I_{DM}	100	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy[2]	L = 0.1 mH	E_{AR}	31	mJ
Power Dissipation	T_C = 25°C	P_D	50	W
	T_A = 25°C		2	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.5	K/W
Junction-to-Ambient	R_{thJA}		60	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%.

Advance Information

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.8	1.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		25		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.035		0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.60		0.080	
		V_{GS} = 5 V, I_D = 12.5 A	0.045		0.070	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	16			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	800			pF
Output Capacitance	C_{oss}		320			
Reverse Transfer Capacitance	C_{rss}		90			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	27			nC
Gate-Source Charge[2]	Q_{gs}		6			
Gate-Drain Charge[2]	Q_{gd}		8			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω I_D ≃ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		20	ns
Rise Time[2]	t_r		20		40	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				25	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	90			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

Siliconix incorporated

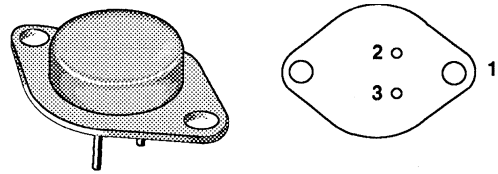
SMM11P20

P-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-11

TO-204AA (TO-3) BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	11	A
	T_C = 100°C		7.0	
Pulsed Drain Current[2]		I_{DM}	44	
Avalanche Current (See Figure 9)		I_A	11	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		30	
Case-to-Sink	R_{thCS}	0.1		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		11.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 6 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 6 A, T_J = 125°C	0.50		1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 6 A	4.3	4.0	1.4	S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11 A	55	40	75	nC
Gate-Source Charge[2]	Q_{gs}		9	6	18	
Gate-Drain Charge[2]	Q_{gd}		30	20	45	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 15.4 Ω, $I_D \simeq$ 6 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		30		40	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		100	
Fall Time[2]	t_f		16		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				11.0	A
Pulsed Current[3]	I_{SM}				44	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

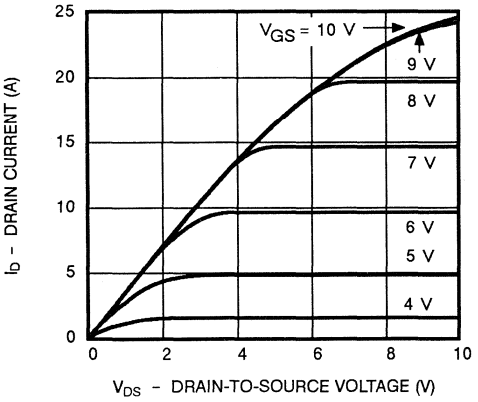


Figure 2. Transfer Characteristics

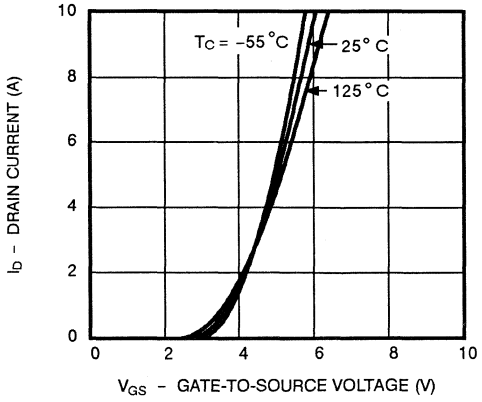


Figure 3. Transconductance

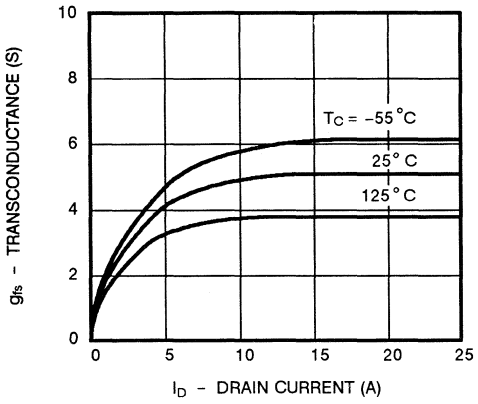


Figure 4. On-Resistance

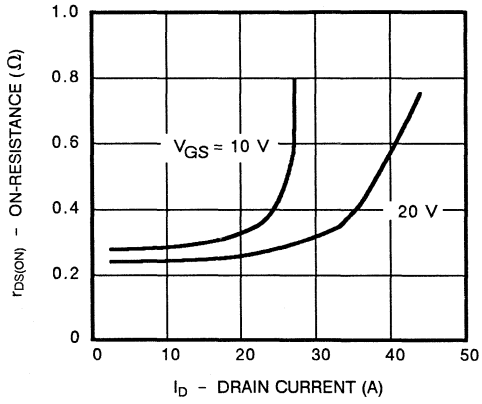


Figure 5. Capacitance

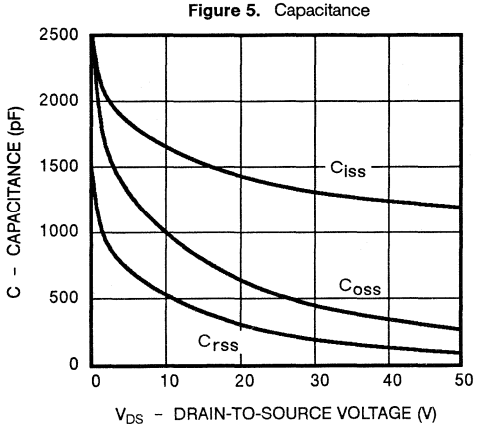
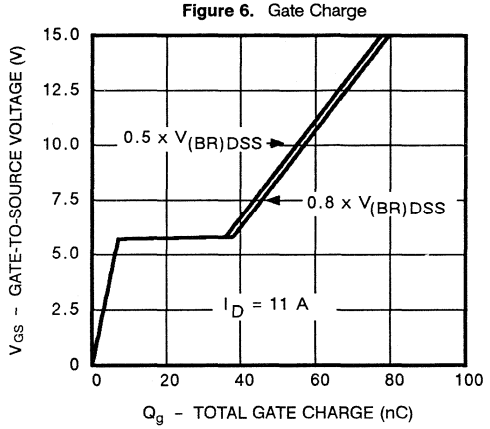


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

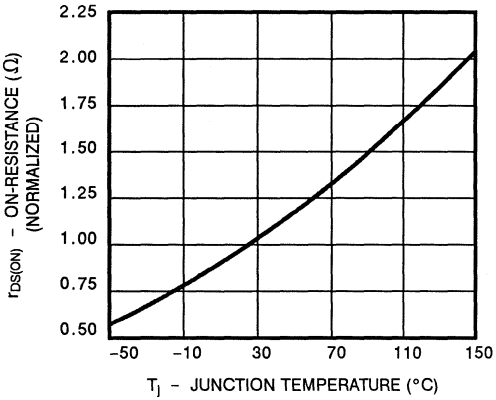
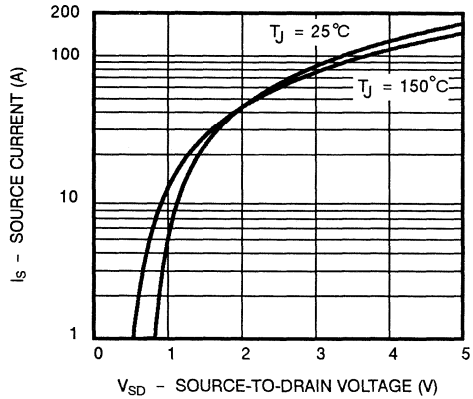


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

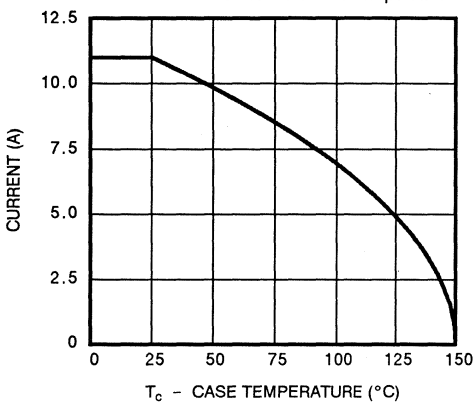
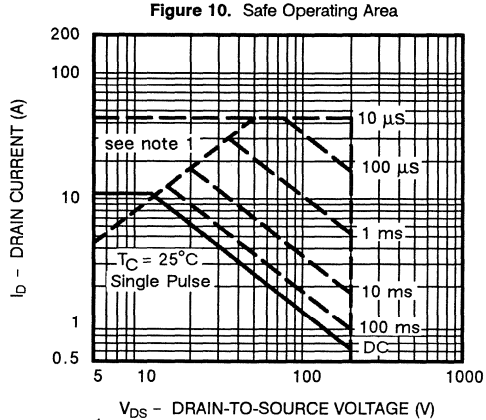
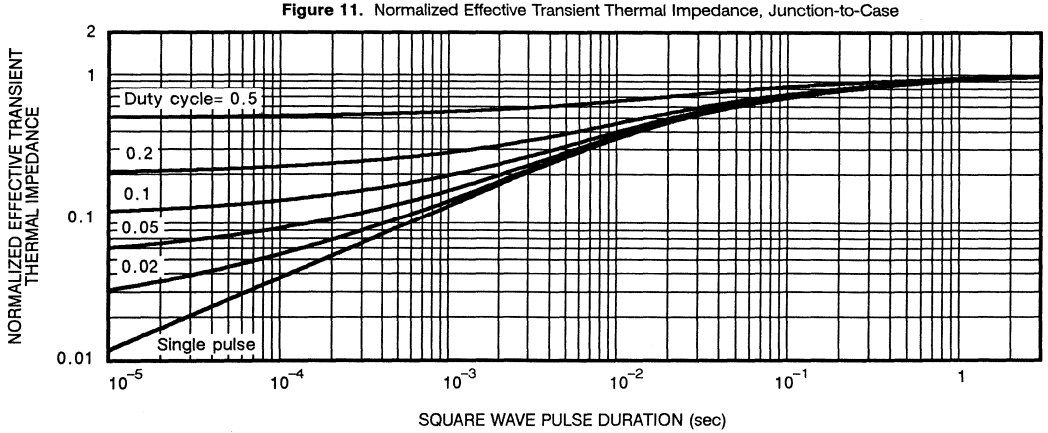


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

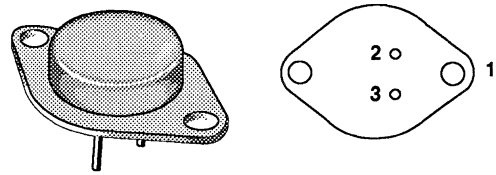


Siliconix incorporated

SMM20P10

P-Channel Enhancement Mode Transistor

TO-204AA (TO-3) BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	0.20	-20

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		13	
Pulsed Drain Current[2]		I_{DM}	80	
Avalanche Current (See Figure 9)		I_A	20	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		30	
Case-to-Sink	R_{thCS}	0.1		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 A	0.15		0.20	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	0.24		0.36	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	6.7	4.8		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		310			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	47	38	60	nC
Gate-Source Charge[2]	Q_{gs}		10	6.0	18	
Gate-Drain Charge[2]	Q_{gd}		27	18	36	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω, I_D ≃ 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		80	
Fall Time[2]	t_f		15		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				80	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.7	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

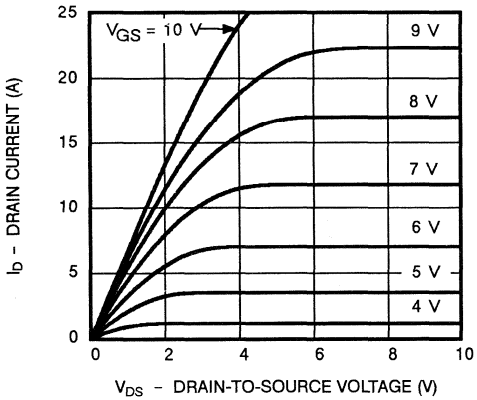


Figure 2. Transfer Characteristics

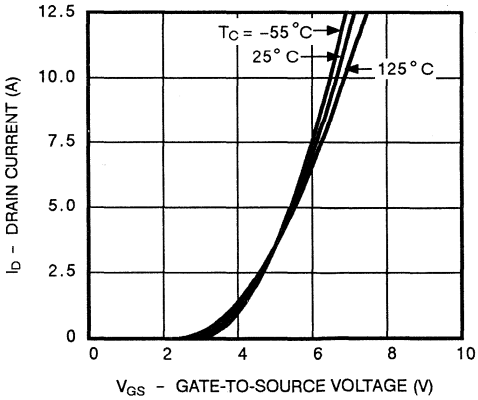


Figure 3. Transconductance

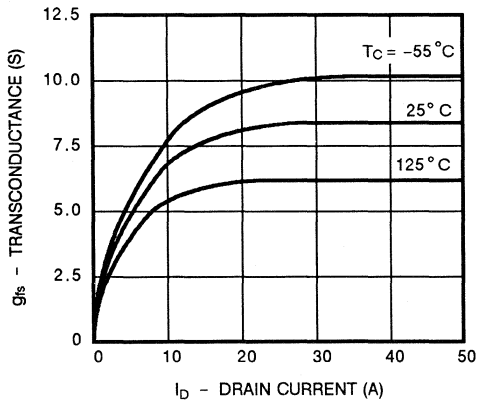


Figure 4. On-Resistance

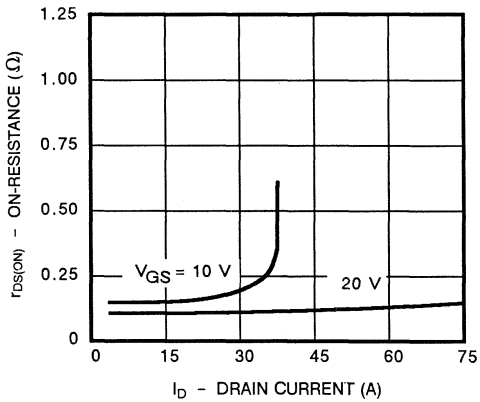


Figure 5. Capacitance

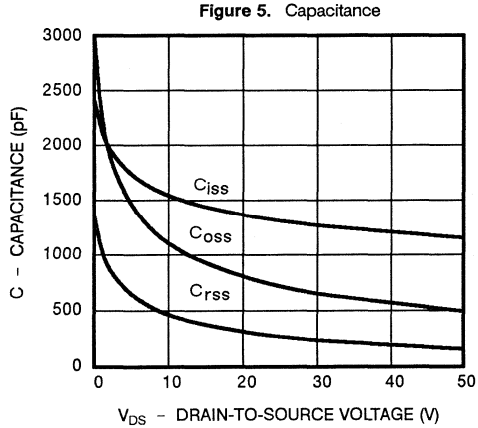
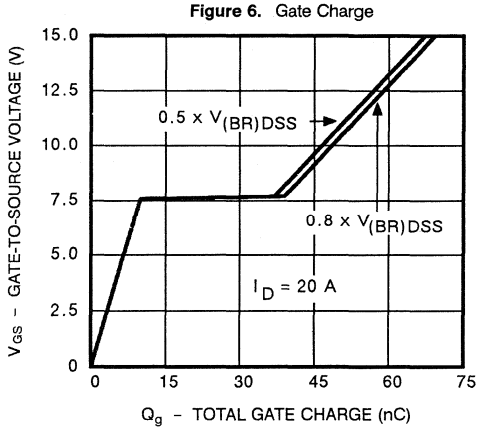


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

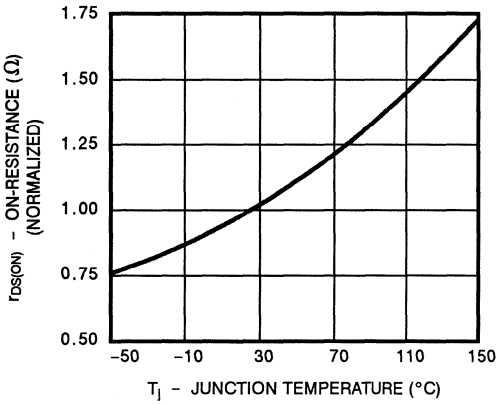
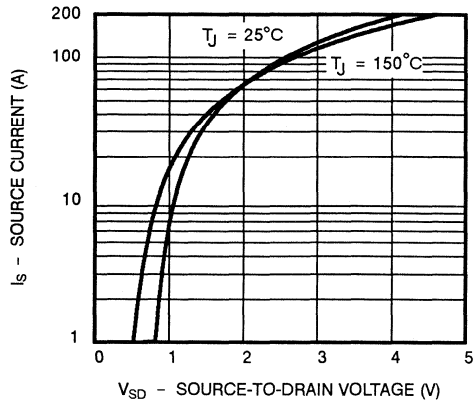


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

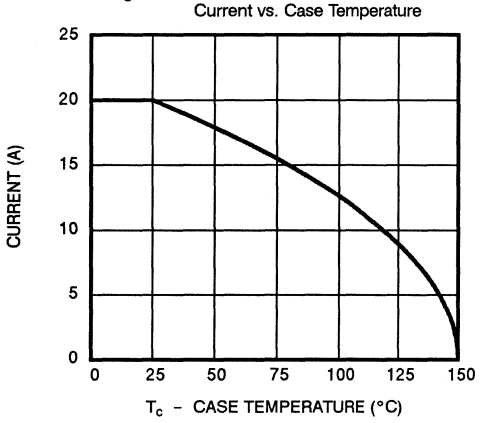
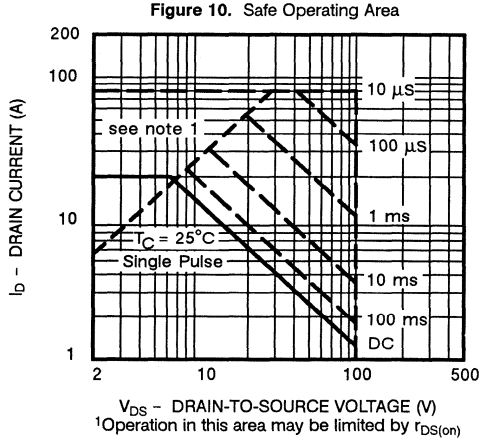
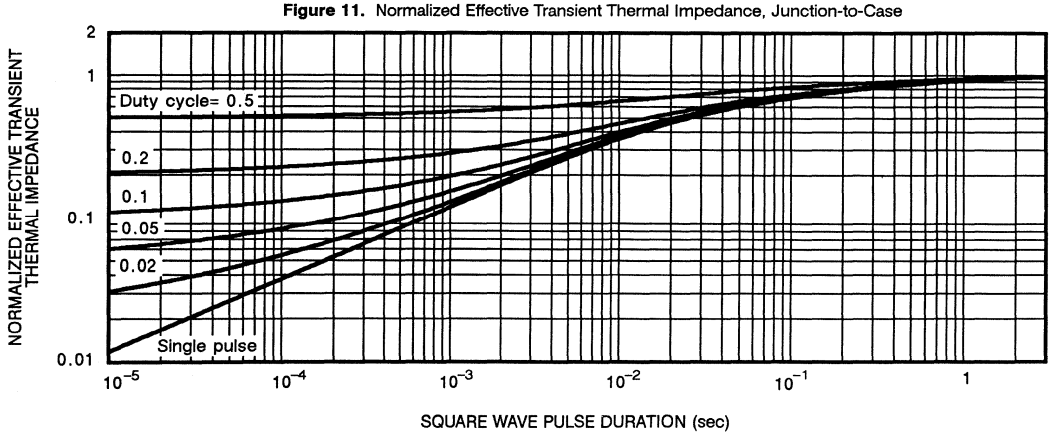


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

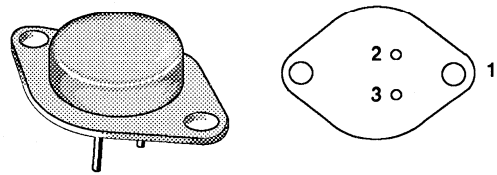


Siliconix incorporated

SMM70N06

N-Channel Enhancement Mode Transistor

TO-204AE (TO-3) BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.018	70

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	70	A
	T_C = 100°C		43	
Pulsed Drain Current[1]		I_{DM}	280	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.50	K/W
Junction-to-Ambient	R_{thJA}		30	
Case-to-Sink	R_{thCS}	0.1		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		70		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 35 A	0.013		0.018	Ω
		V_{GS} = 10 V, I_D = 35 A, T_J = 125°C	0.020		0.027	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 35 A	25	20		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	4800			pF
Output Capacitance	C_{oss}		2000			
Reverse Transfer Capacitance	C_{rss}		600			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V	120	100	160	nC
Gate-Source Charge[2]	Q_{gs}	I_D = 70 A	30	20	40	
Gate-Drain Charge[2]	Q_{gd}		50	40	80	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.86 Ω, $I_D \simeq$ 35 A, V_{GEN} = 10 V, R_G = 2.5 Ω	20		40	ns
Rise Time[2]	t_r		30		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		45		90	
Fall Time[2]	t_f		22		45	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				70	A
Pulsed Current[3]	I_{SM}				280	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	80			ns
Reverse Recovery Charge	Q_{rr}		0.2			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

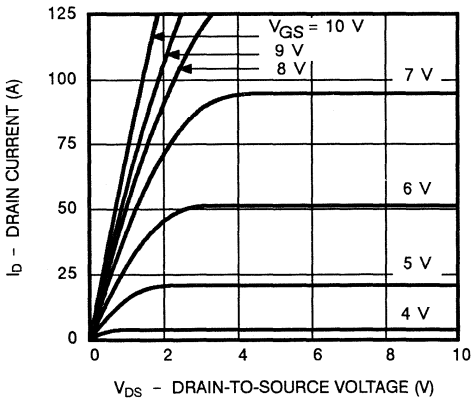


Figure 2. Transfer Characteristics

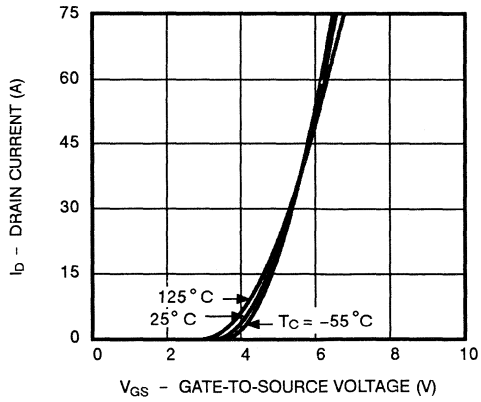


Figure 3. Transconductance

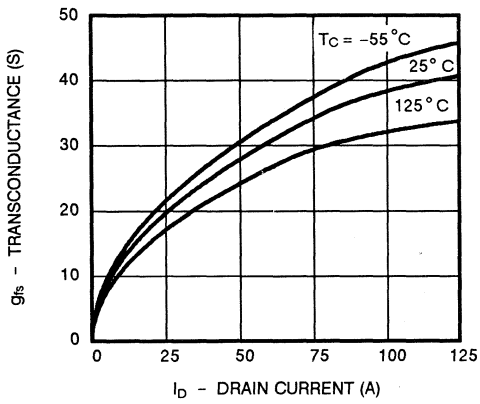


Figure 4. On-Resistance

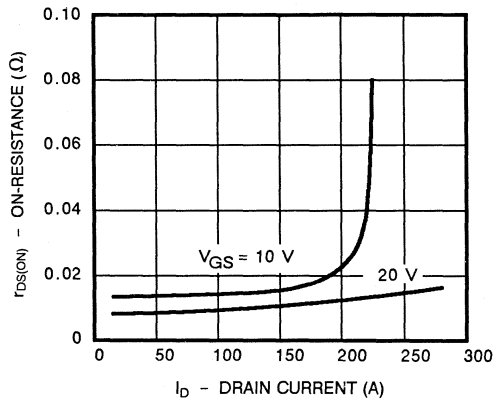


Figure 5. Capacitance

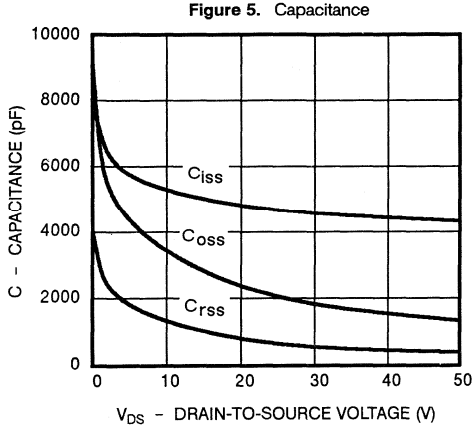
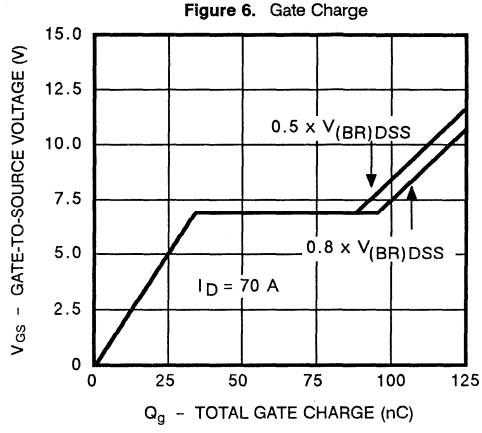


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

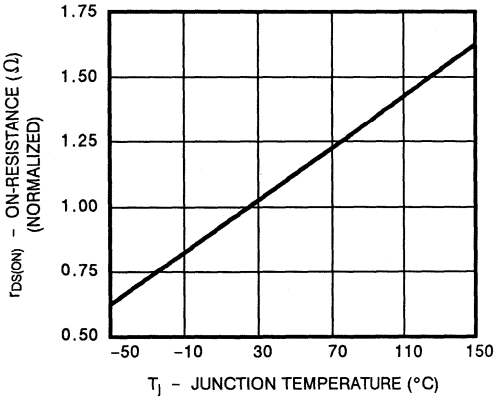
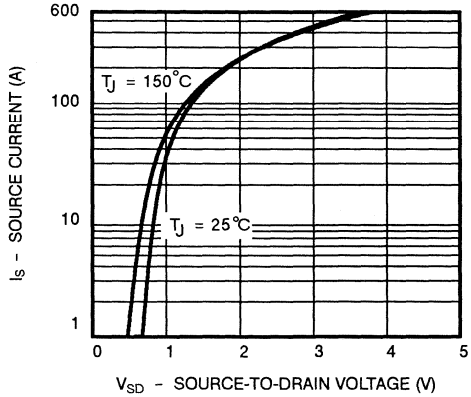


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

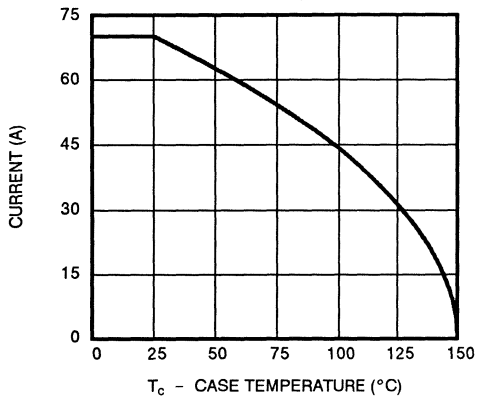
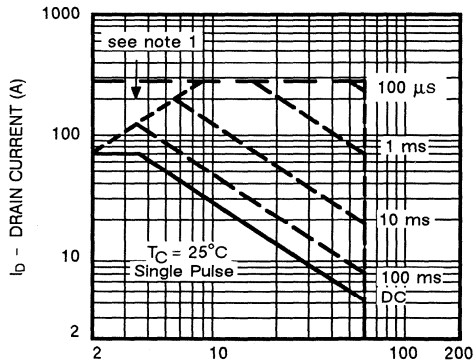
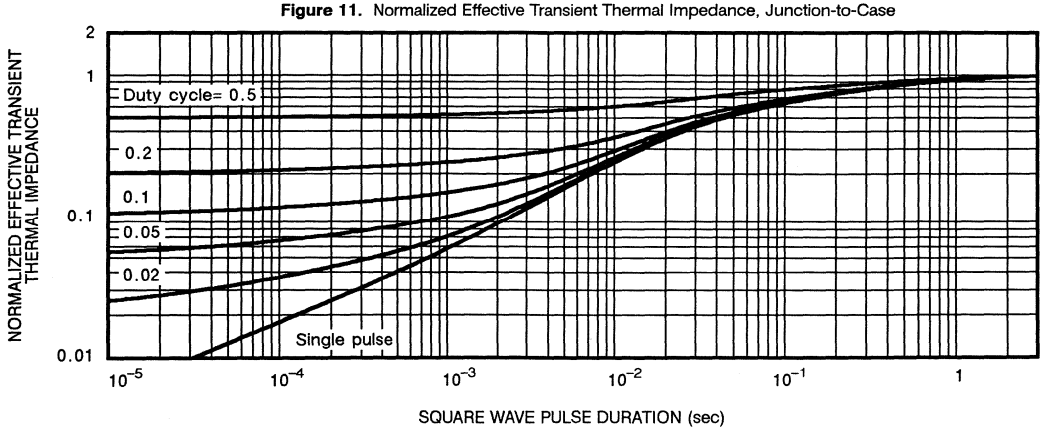


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

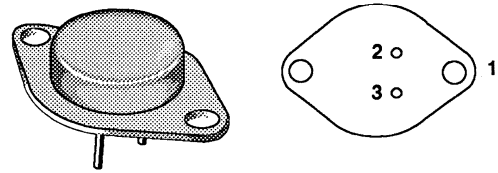


Siliconix incorporated

SMM70N10

N-Channel Enhancement Mode Transistor

TO-204AE (TO-3) BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.025	70

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	70	A
	T_C = 100°C		45	
Pulsed Drain Current[1]		I_{DM}	280	
Avalanche Current (See Figure 9)		I_A	70	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.50	K/W
Junction-to-Ambient	R_{thJA}		30	
Case-to-Sink	R_{thCS}	0.1		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		70		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 45 A	0.020		0.025	Ω
		V_{GS} = 10 V, I_D = 45 A, T_J = 125°C	0.034		0.045	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 45 A	30	20		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	4100			pF
Output Capacitance	C_{oss}		1200			
Reverse Transfer Capacitance	C_{rss}		310			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 70 A	110	90	140	nC
Gate-Source Charge[2]	Q_{gs}		30	20	40	
Gate-Drain Charge[2]	Q_{gd}		52	40	80	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 0.71 Ω, I_D ≃ 70 A, V_{GEN} = 10 V, R_G = 2.5 Ω	20		40	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				70	A
Pulsed Current[3]	I_{SM}				280	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	125			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

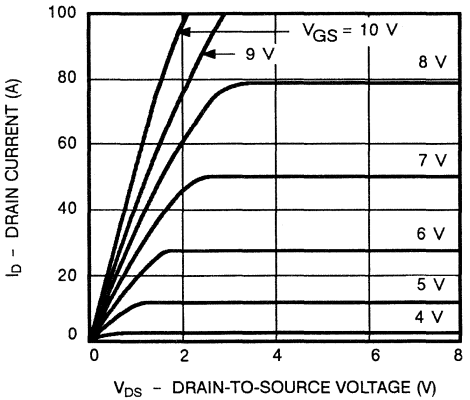


Figure 2. Transfer Characteristics

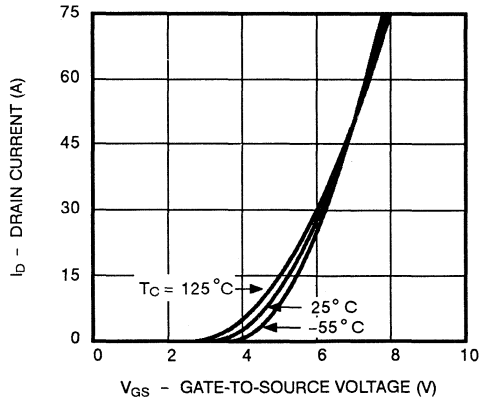


Figure 3. Transconductance

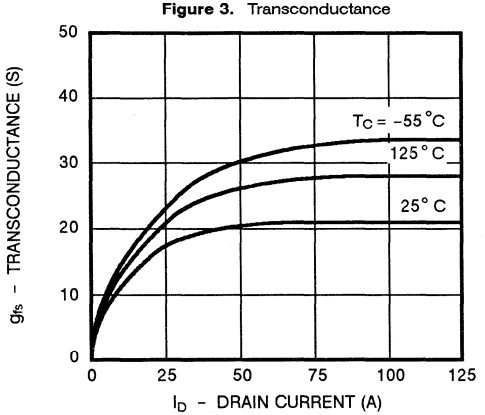


Figure 4. On-Resistance

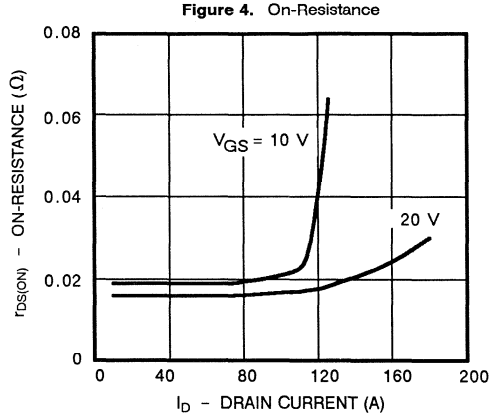


Figure 5. Capacitance

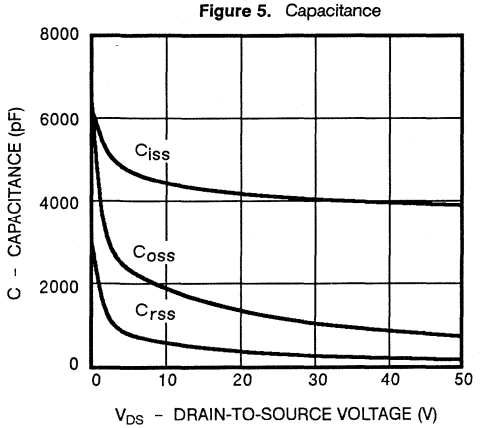
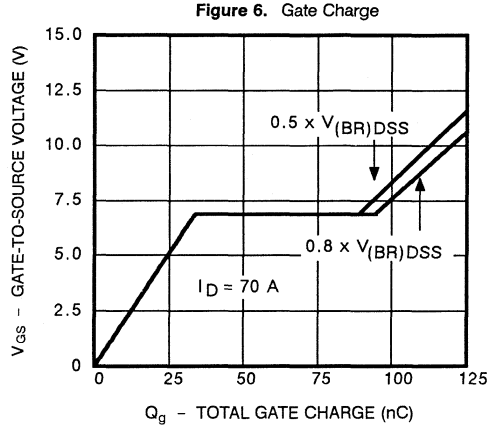


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

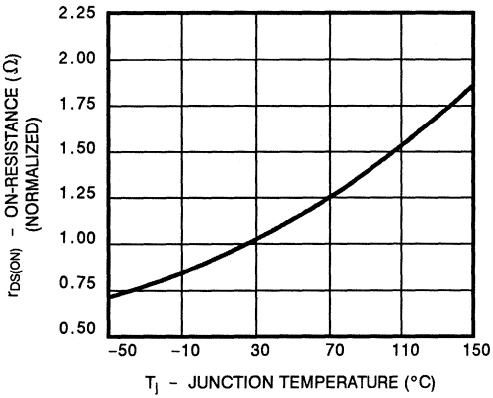
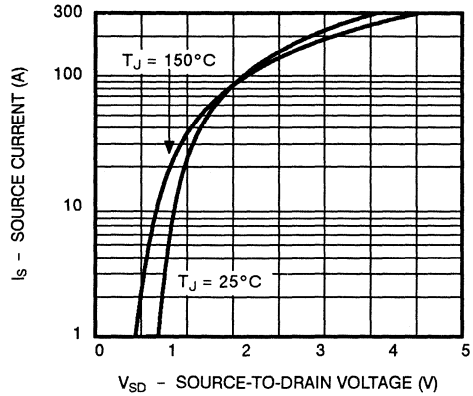


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

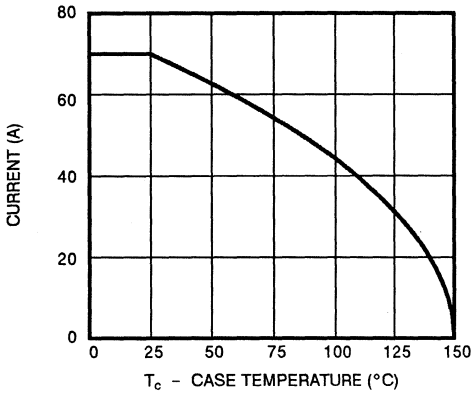
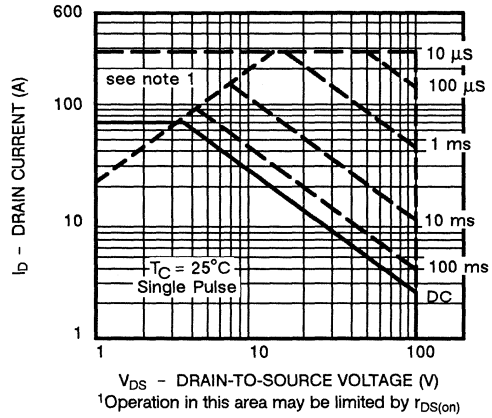
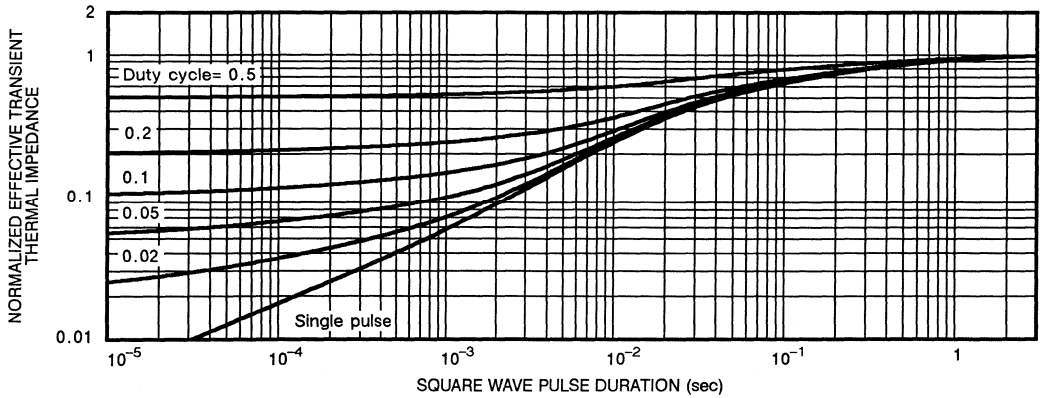


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

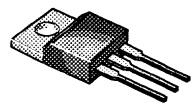
SMP2P20

P-Channel Enhancement Mode Transistor

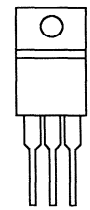
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	3.0	-1.75

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	1.75	A
	T_C = 100°C		1.1	
Pulsed Drain Current[2]		I_{DM}	7.0	
Avalanche Current (See Figure 9)		I_{AR}	1.75	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	0.15	mJ
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		6.4	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		1.75		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 0.9 A	2.2		3.0	Ω
		V_{GS} = 10 V, I_D = 0.9 A, T_J = 125°C	4.0		5.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 0.9 A	0.8	0.5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	170			pF
Output Capacitance	C_{oss}		70			
Reverse Transfer Capacitance	C_{rss}		25			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.75 A	5.8		11	nC
Gate-Source Charge[2]	Q_{gs}		0.9		3.0	
Gate-Drain Charge[2]	Q_{gd}		3.2		6.0	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 110 Ω, I_D ≃ 0.9 A, V_{GEN} = 10 V, R_G = 25 Ω	7.5		15	ns
Rise Time[2]	t_r		13		25	
Turn-Off Delay Time[2]	$t_{d(off)}$		45		60	
Fall Time[2]	t_f		28		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				1.75	A
Pulsed Current[3]	I_{SM}				7.0	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			5.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	100			ns
Reverse Recovery Charge	Q_{rr}		36			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

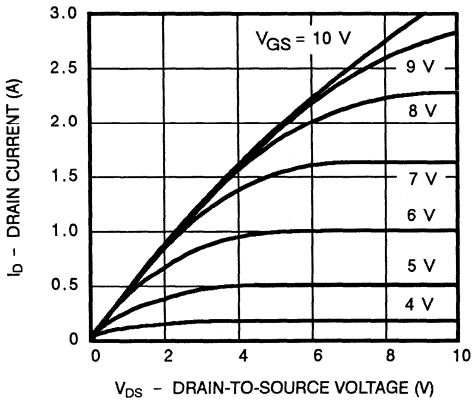


Figure 2. Transfer Characteristics

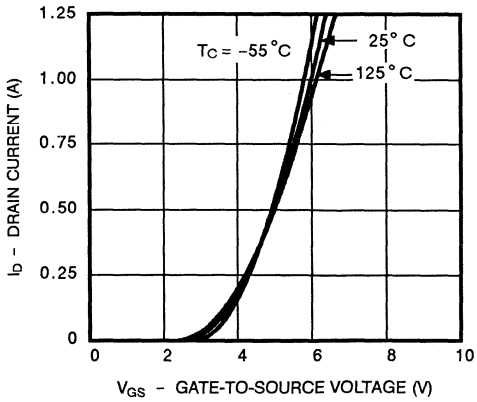


Figure 3. Transconductance

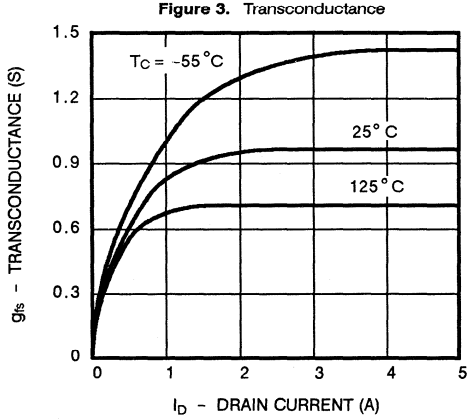


Figure 4. On-Resistance

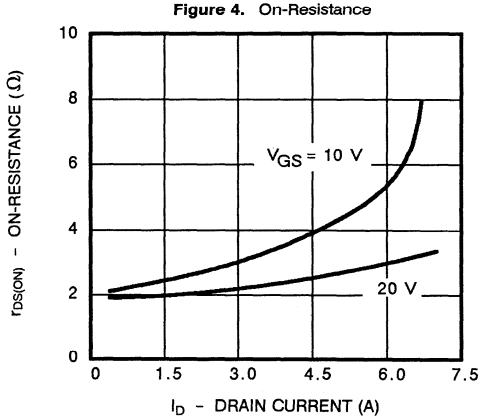


Figure 5. Capacitance

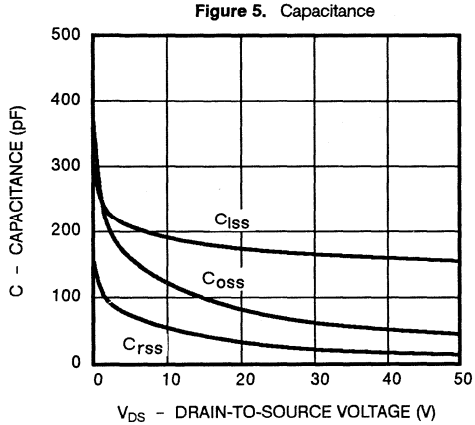
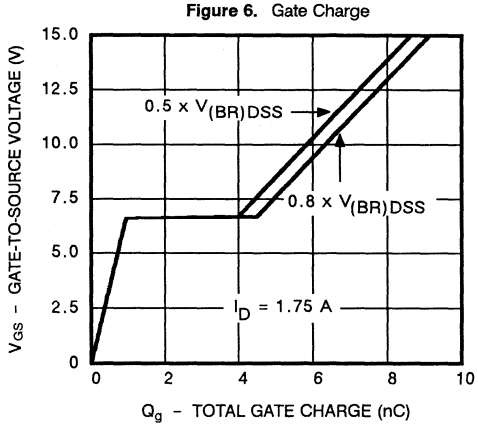


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

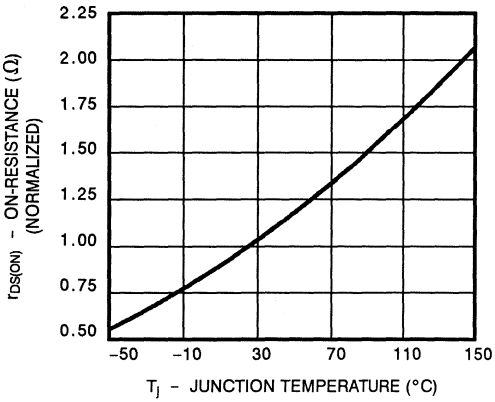
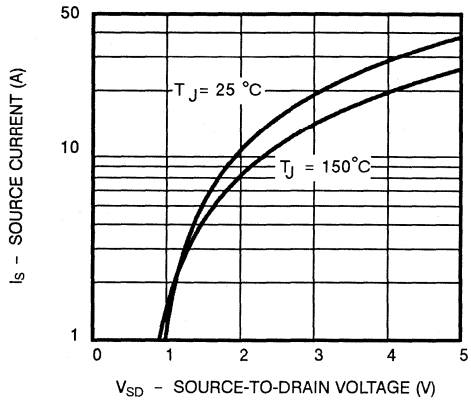


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

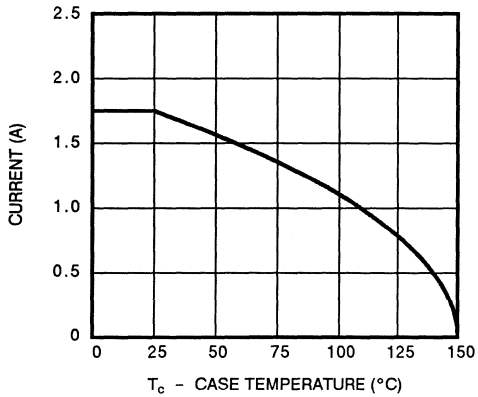
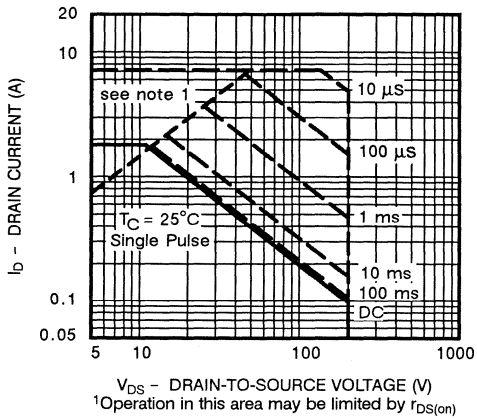
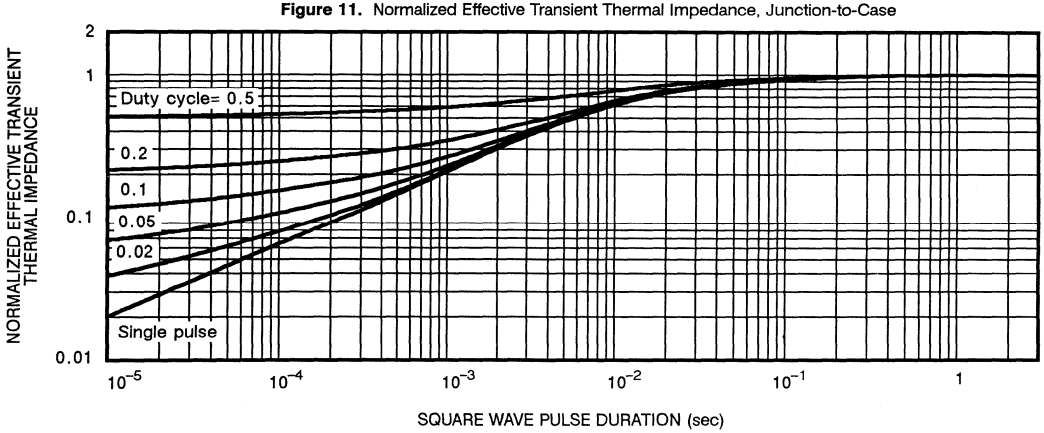


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

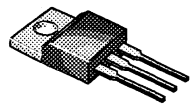


Siliconix incorporated

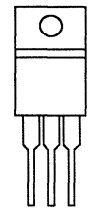
SMP3N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	3.0	2.5	250

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	A
	T_C = 100°C		1.6	
Pulsed Drain Current[1]		I_{DM}	12	
Avalanche Current (See Figure 9)		I_{AR}	2.5	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	3	mJ
Power Dissipation	T_C = 25°C	P_D	48	W
	T_C = 100°C		19	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.6	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			2.5		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1.5 A		2.2		3.0	Ω
		V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C		4.4		6.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1.5 A		1.5	1.0		S
DYNAMIC							
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		350			pF
Output Capacitance	C_{oss}			75			
Reverse Transfer Capacitance	C_{rss}			25			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.5 A		11		18	nC
Gate-Source Charge[2]	Q_{gs}			2		5	
Gate-Drain Charge[2]	Q_{gd}			7		11	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 80 Ω, $I_D \simeq$ 2.5 A, V_{GEN} = 10 V, R_G = 25 Ω		7		60	ns
Rise Time[2]	t_r			15		50	
Turn-Off Delay Time[2]	$t_{d(off)}$			42		60	
Fall Time[2]	t_f			16		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					3.0	A
Pulsed Current[3]	I_{SM}					12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.6	V
Reverse Recovery Time	t_{rr}	I_F = 3 A, dI_F/dt = 100 A/µs, V_{DD} = 250 V	T_J = 25°C T_J = 125°C	135 175		250 300	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C T_J = 125°C	5 7			A
Reverse Recovery Charge	Q_{rr}		T_J = 25°C T_J = 125°C	0.34 0.56		1.2 4.0	µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

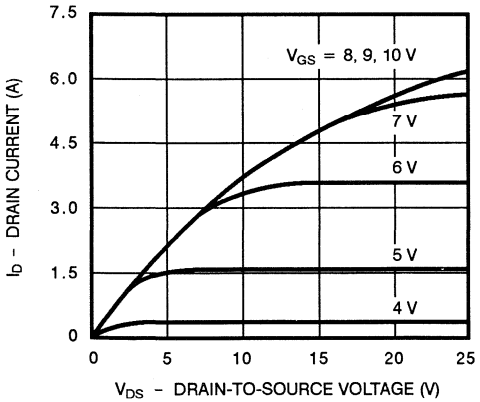


Figure 2. Transfer Characteristics

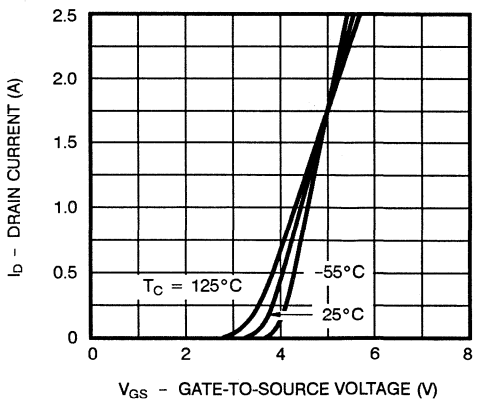


Figure 3. Transconductance

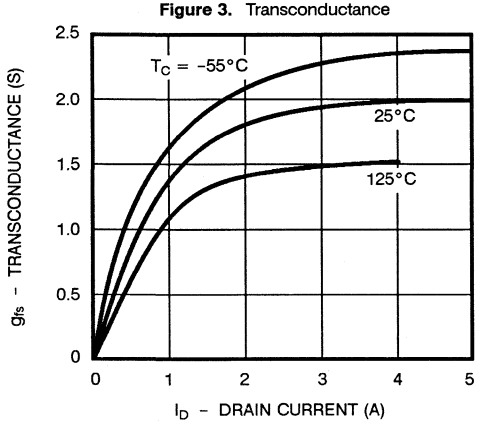


Figure 4. On-Resistance

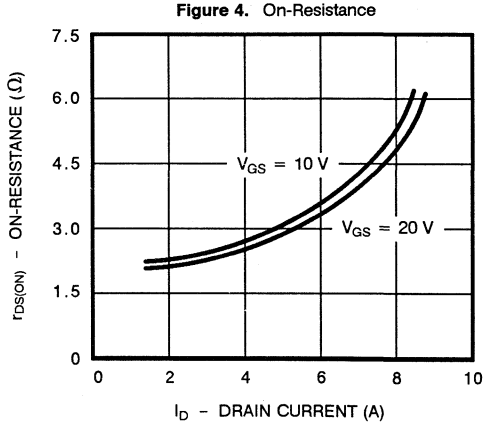


Figure 5. Capacitance

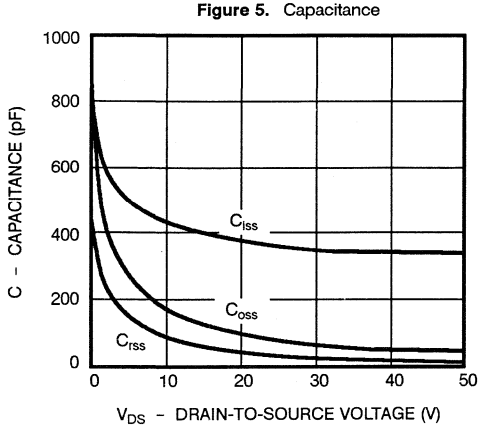
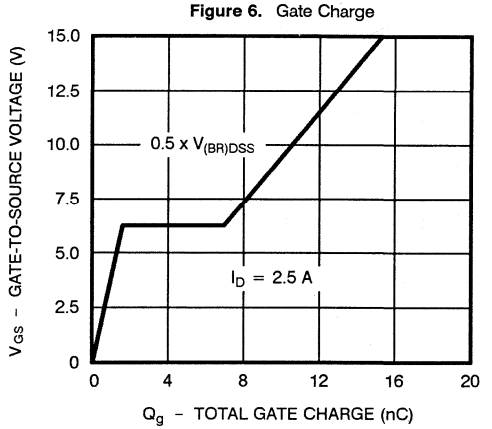


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

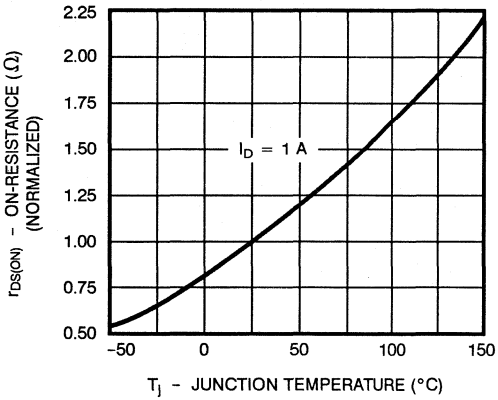
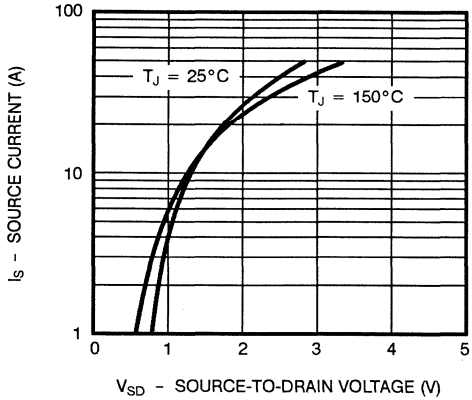


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

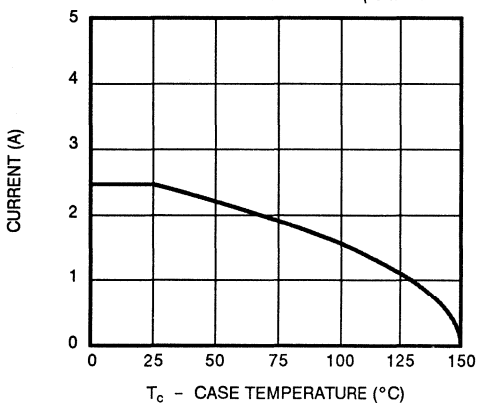
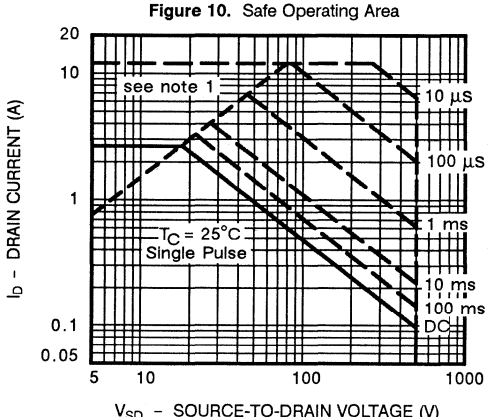
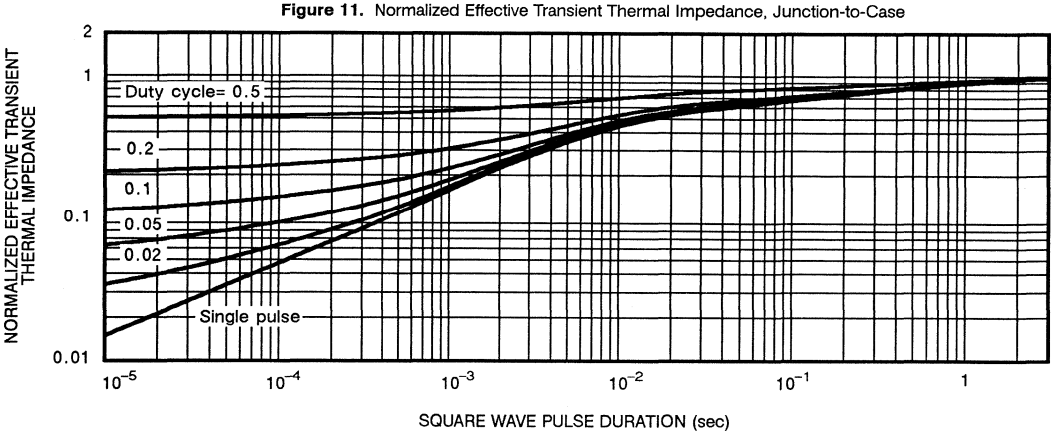


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

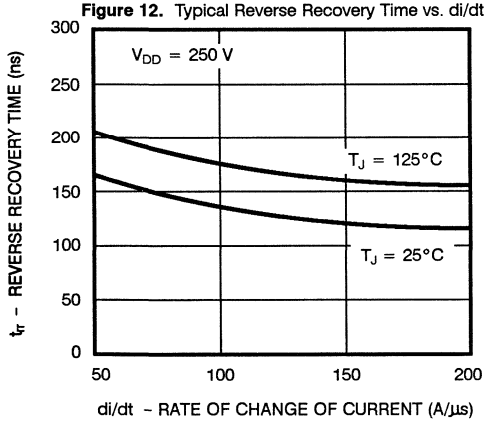


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

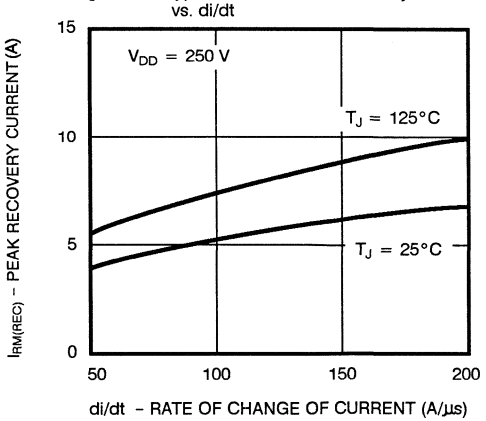


Figure 14. Commutating Safe Operating Area

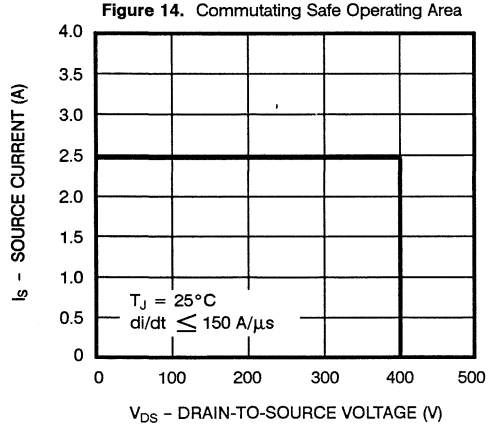


Figure 15. Typical dv/dt vs. di/dt

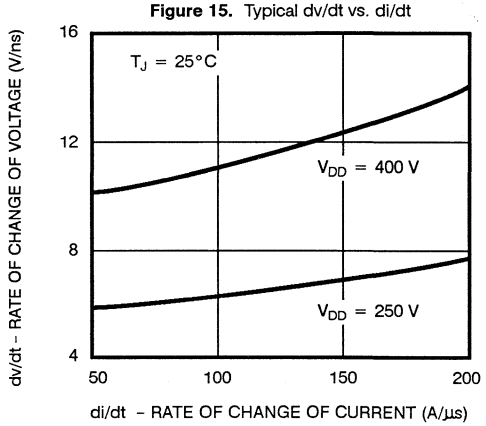
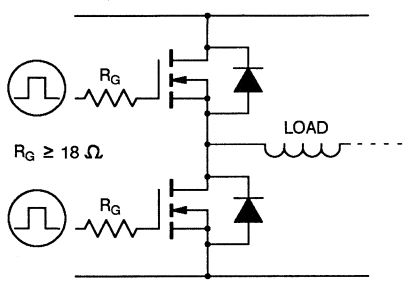
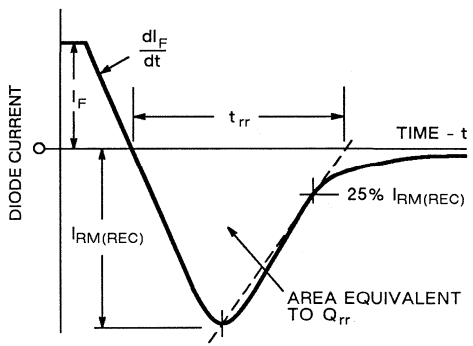


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4

Siliconix incorporated

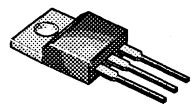
SMP3P10

P-Channel Enhancement Mode Transistor

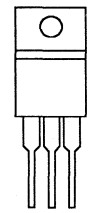
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	1.2	-3.0

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	3.0	A
	T_C = 100°C		2.0	
Pulsed Drain Current[2]		I_{DM}	12	
Avalanche Current (See Figure 9)		I_{AR}	3.0	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	0.45	mJ
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		6.4	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		3.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1.5 A	1.0		1.2	Ω
		V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	1.6		2.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1.5 A	0.9	0.5		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	150			pF
Output Capacitance	C_{oss}		65			
Reverse Transfer Capacitance	C_{rss}		25			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3 A	6.6		11	nC
Gate-Source Charge[2]	Q_{gs}		1.5		3.0	
Gate-Drain Charge[2]	Q_{gd}		3.8		6.0	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 33 Ω, I_D ≃ 1.5 A, V_{GEN} = 10 V, R_G = 25 Ω	7		30	ns
Rise Time[2]	t_r		45		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		38		60	
Fall Time[2]	t_f		55		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				3.0	A
Pulsed Current[3]	I_{SM}				12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			5.5	V
Reverse Recovery Time	t_{rr}		70			ns
Reverse Recovery Charge	Q_{rr}		0.20			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

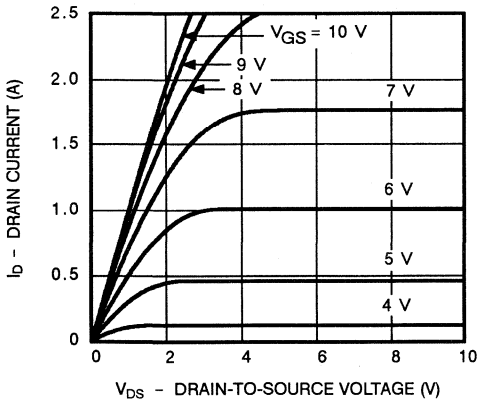


Figure 2. Transfer Characteristics

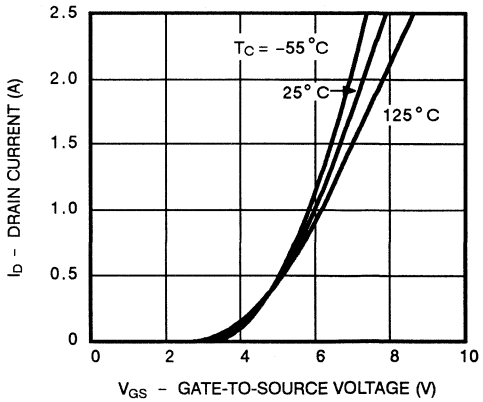


Figure 3. Transconductance

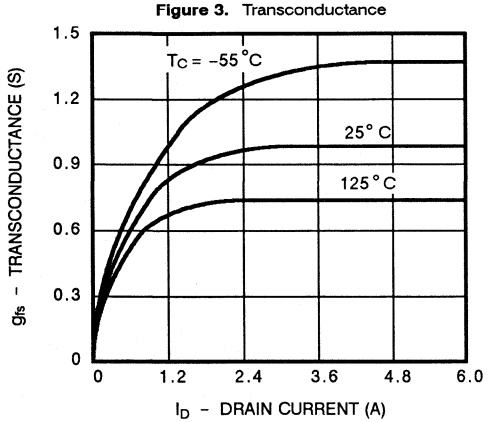


Figure 4. On-Resistance

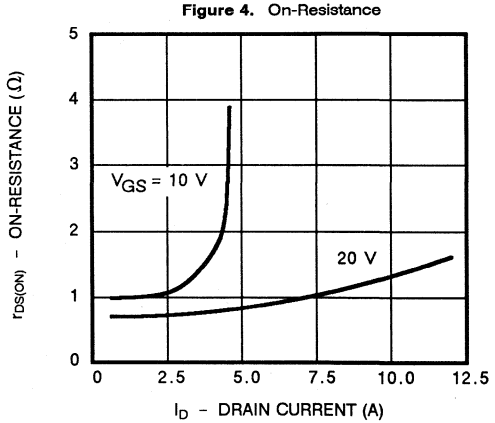


Figure 5. Capacitance

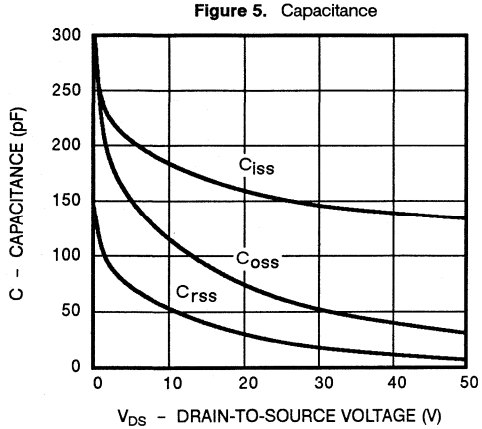
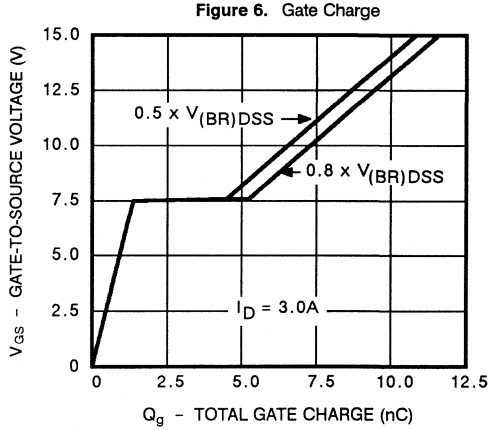


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

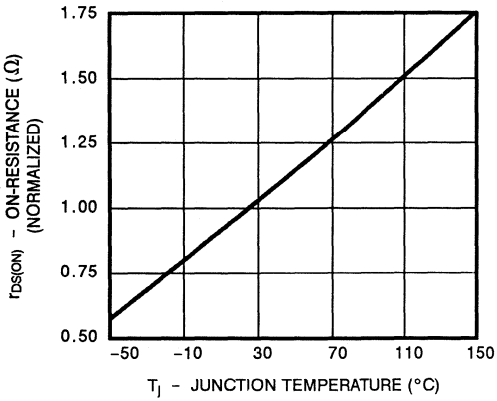
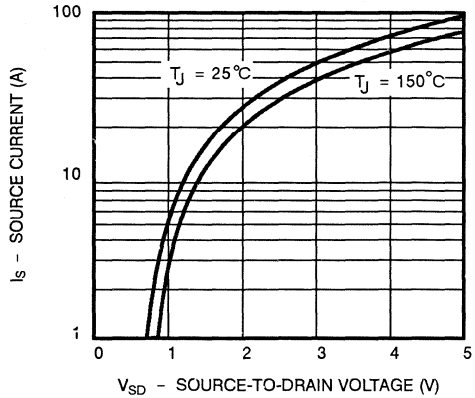


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

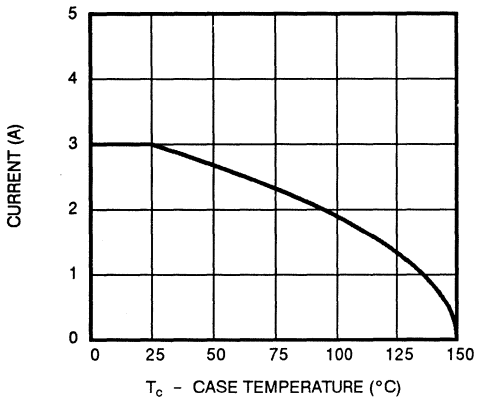
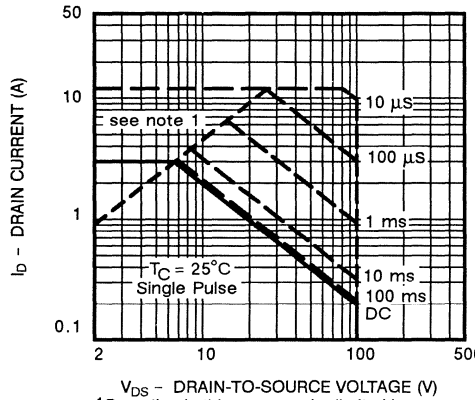
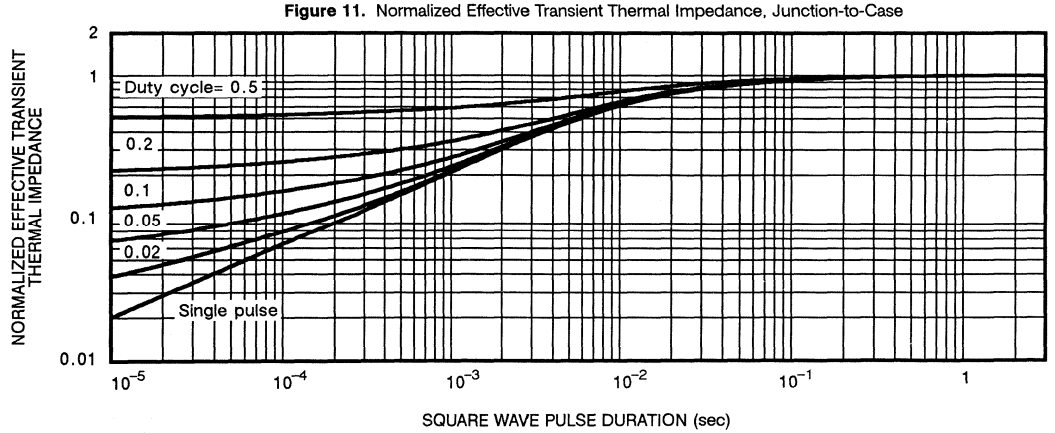


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

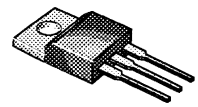
SMP4N60

N-Channel Enhancement Mode Transistor

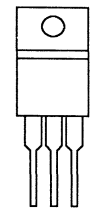
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
600	2.0	4.0

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.5	
Pulsed Drain Current[1]		I_{DM}	16	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		600		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		4.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2 A	1.8		2.0	Ω
		V_{GS} = 10 V, I_D = 2 A, T_J = 125°C	3.9		4.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2 A		1.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	700			pF
Output Capacitance	C_{oss}		120			
Reverse Transfer Capacitance	C_{rss}		50			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4 A	22		45	nC
Gate-Source Charge[2]	Q_{gs}		4		7	
Gate-Drain Charge[2]	Q_{gd}		12		24	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 300 V, R_L = 75 Ω, $I_D \simeq$ 4 A, V_{GEN} = 10 V, R_G = 12 Ω	8		17	ns
Rise Time[2]	t_r		13		20	
Turn-Off Delay Time[2]	$t_{d(off)}$		48		60	
Fall Time[2]	t_f		22		35	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				4.0	A
Pulsed Current[3]	I_{SM}				16.0	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	500			ns
Reverse Recovery Charge	Q_{rr}		2.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

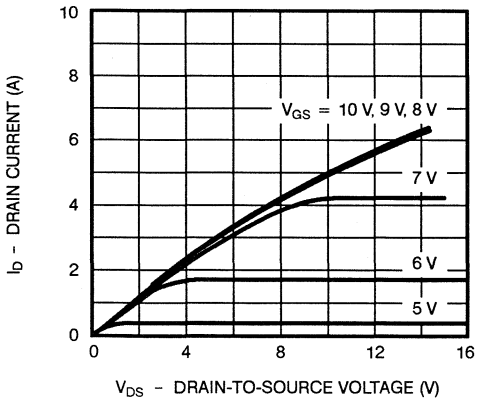


Figure 2. Transfer Characteristics

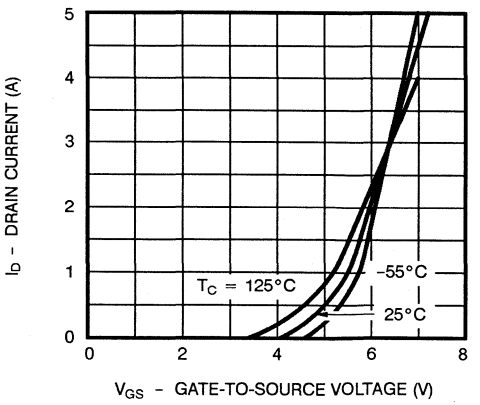


Figure 3. Transconductance

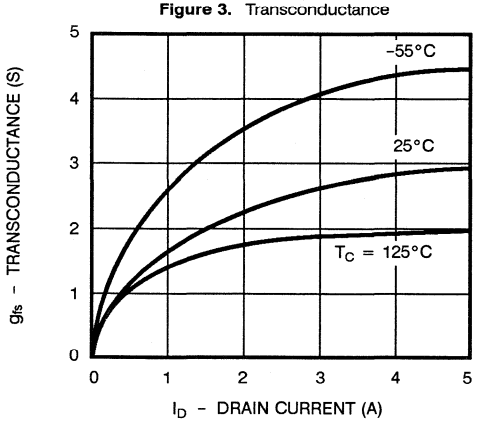


Figure 4. On-Resistance

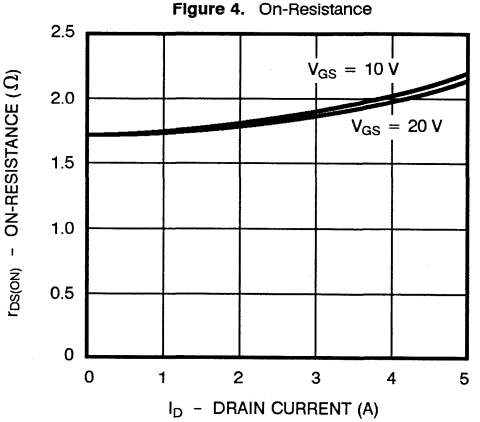


Figure 5. Capacitance

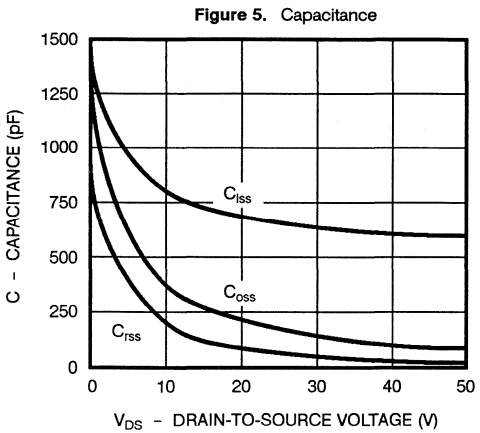
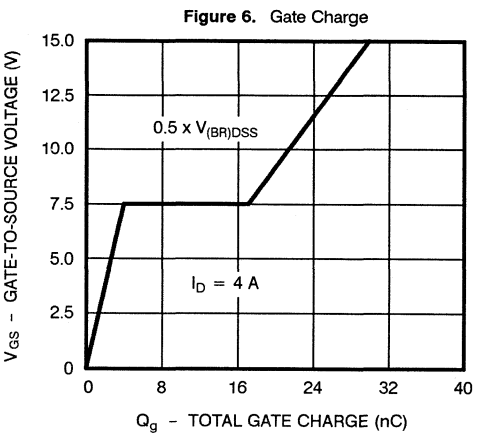


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

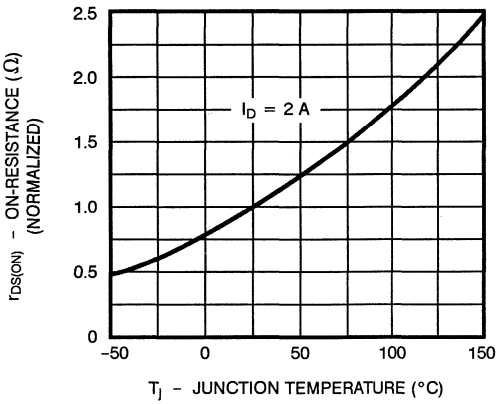
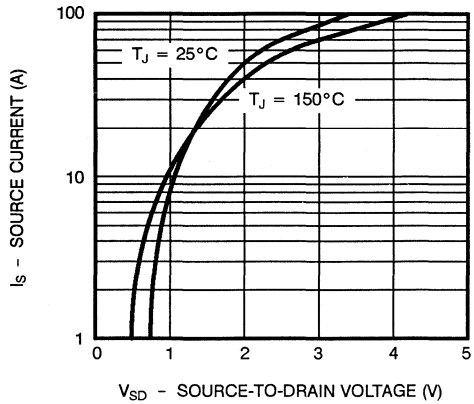


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

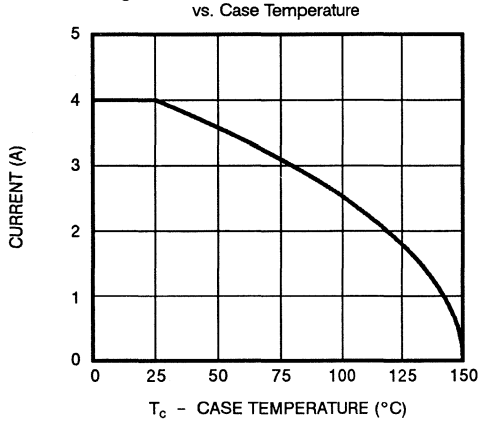
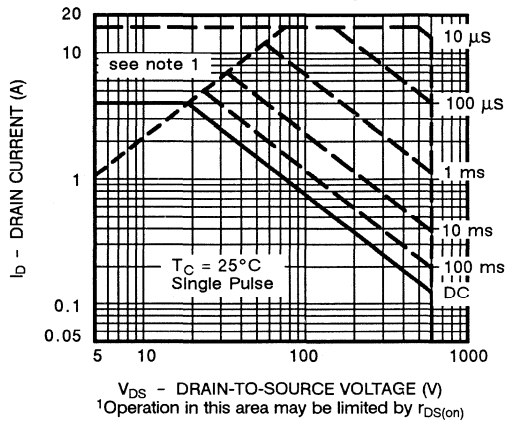
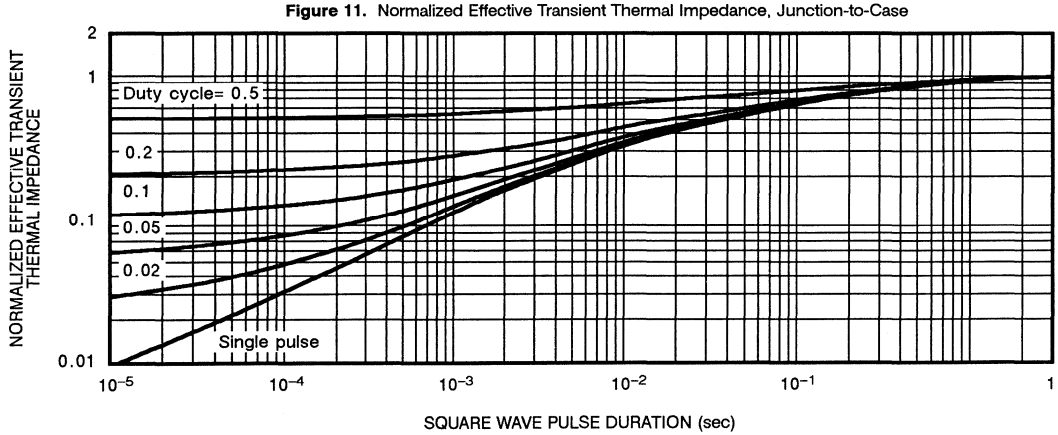


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

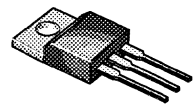
SMP5N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

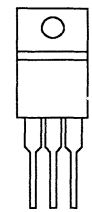
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	1.5	4.5	250

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	4.5	A
	T_C = 100°C		3.0	
Pulsed Drain Current[1]		I_{DM}	20	
Avalanche Current (See Figure 9)		I_{AR}	4.5	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	10	mJ
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.67	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			5.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2.5 A		1.2		1.5	Ω
		V_{GS} = 10 V, I_D = 25. A, T_J = 125°C		2.6		3.3	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2.5 A		3.0	2.5		S
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		720			pF
Output Capacitance	C_{oss}			130			
Reverse Transfer Capacitance	C_{rss}			40			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.5 A		22		30	nC
Gate-Source Charge[2]	Q_{gs}			3.5		7	
Gate-Drain Charge[2]	Q_{gd}			11		20	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 50 Ω $I_D \simeq$ 4.5 A, V_{GEN} = 10 V, R_G = 7.5 Ω		8		30	ns
Rise Time[2]	t_r			13		30	
Turn-Off Delay Time[2]	$t_{d(off)}$			32		55	
Fall Time[2]	t_f			20		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					5.0	A
Pulsed Current[3]	I_{SM}					20	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.6	V
Reverse Recovery Time	t_{rr}	I_F = 5 A, dI_F/dt = 100 A/µs V_{DD} = 250 V	T_J = 25°C T_J = 125°C	160 220		250 300	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C T_J = 125°C	9 11			A
Reverse Recovery Charge	Q_{rr}		T_J = 25°C T_J = 125°C	0.72 1.16		1.2 4.0	µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

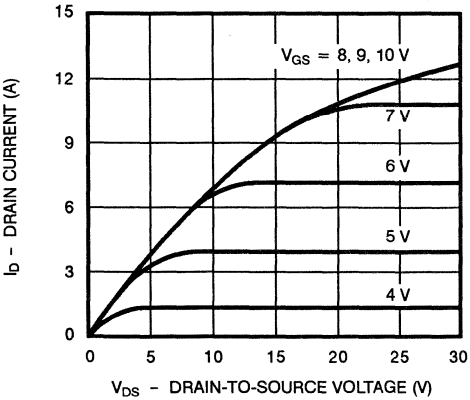


Figure 2. Transfer Characteristics

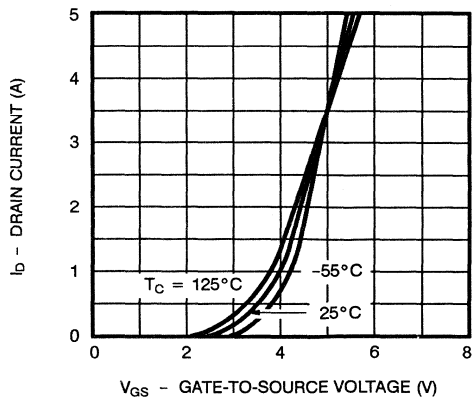


Figure 3. Transconductance

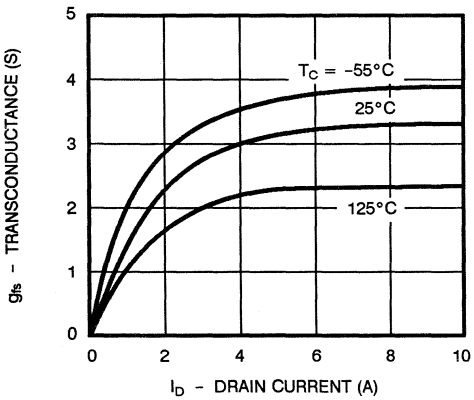


Figure 4. On-Resistance

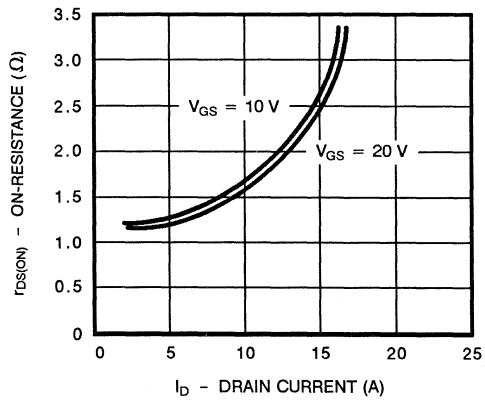


Figure 5. Capacitance

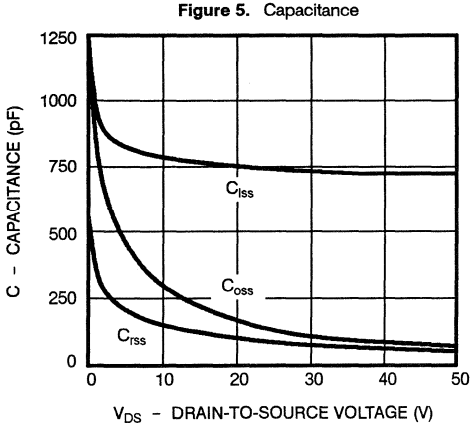
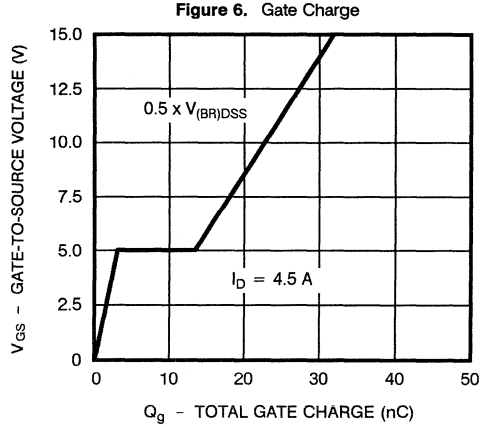


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

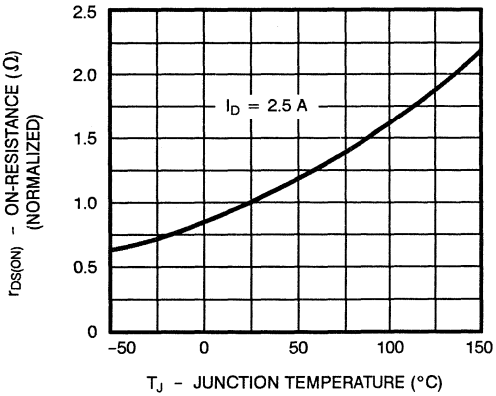
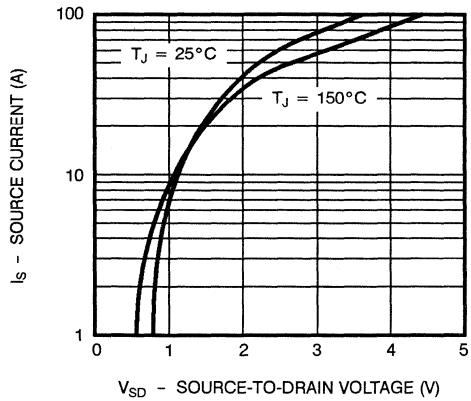


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

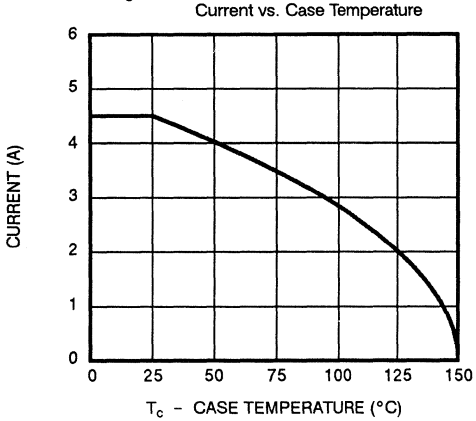
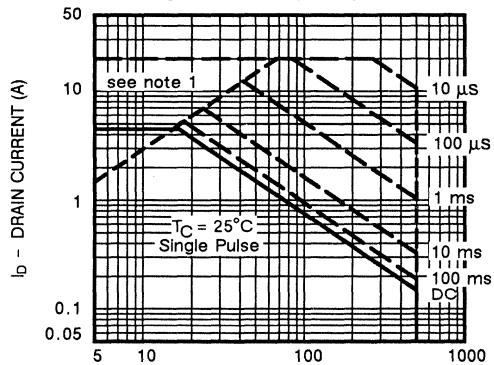
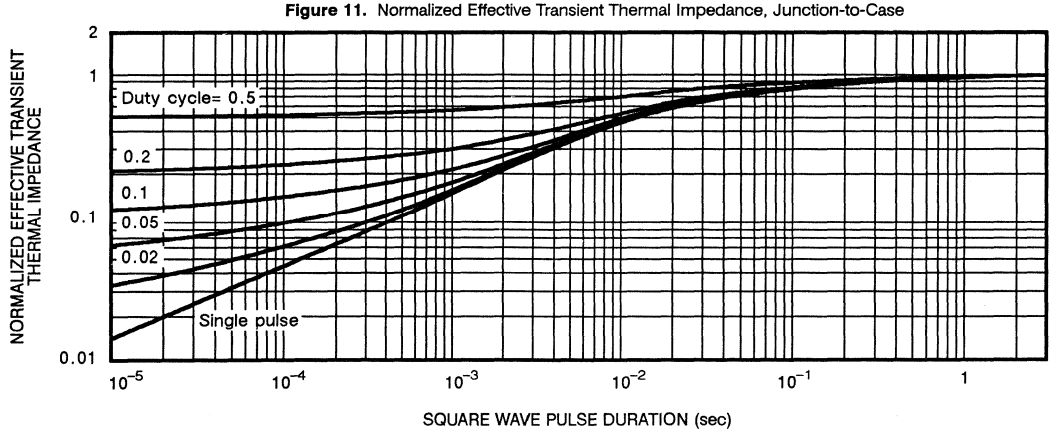


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

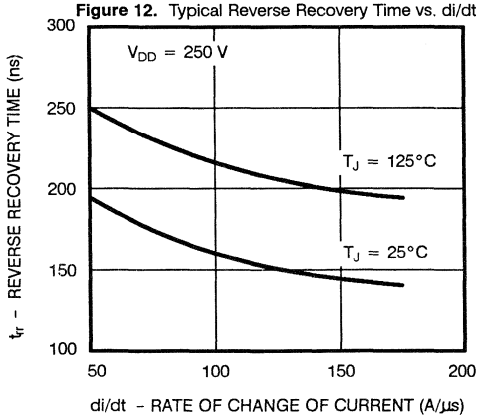


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

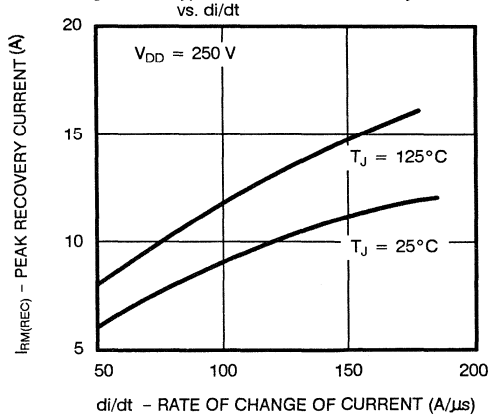


Figure 14. Commutating Safe Operating Area

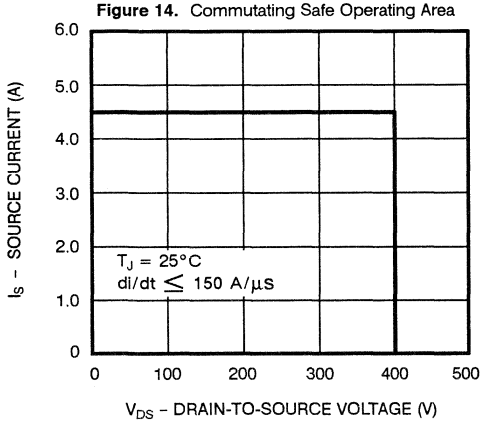


Figure 15. Typical dv/dt vs. di/dt

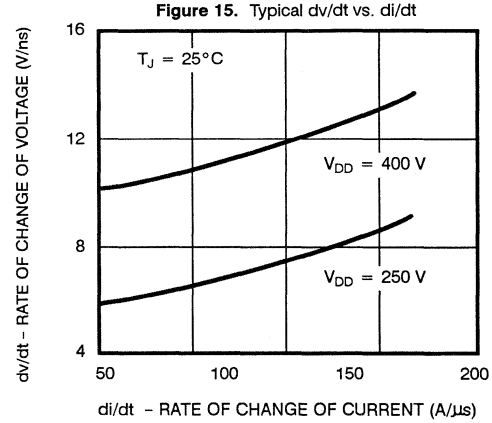
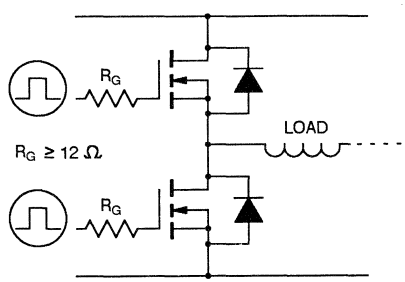
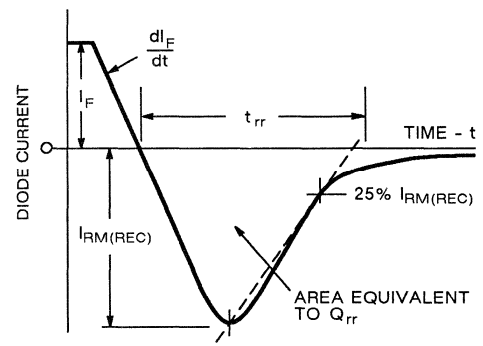


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4

Siliconix incorporated

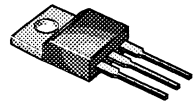
SMP7N60

N-Channel Enhancement Mode Transistor

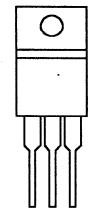
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
600	1.1	7.0

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.5	
Pulsed Drain Current[1]		I_{DM}	28.0	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		600		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V			250	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 9 V, V_{GS} = 10 V		7.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 3.5 A	0.9		1.1	Ω
		V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C			2.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 3.5 A		2.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1200			pF
Output Capacitance	C_{oss}		200			
Reverse Transfer Capacitance	C_{rss}		80			
Total Gate Charge[2]	Q_g	V_{DS} = 300 V, V_{GS} = 10 V, I_D = 7 A	42		60	nC
Gate-Source Charge[2]	Q_{gs}		6.3		10	
Gate-Drain Charge[2]	Q_{gd}		25		39	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 300 V, R_L = 42 Ω, $I_D \simeq$ 7 A, V_{GEN} = 10 V, R_G = 9 Ω	11		20	ns
Rise Time[2]	t_r		27		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		64		83	
Fall Time[2]	t_f		29		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				7	A
Pulsed Current[3]	I_{SM}				28	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	500			ns
Reverse Recovery Charge	Q_{rr}		3.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

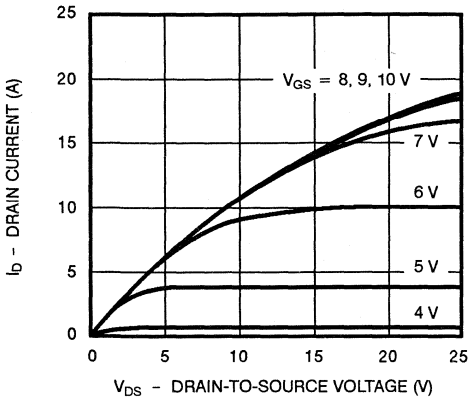


Figure 2. Transfer Characteristics

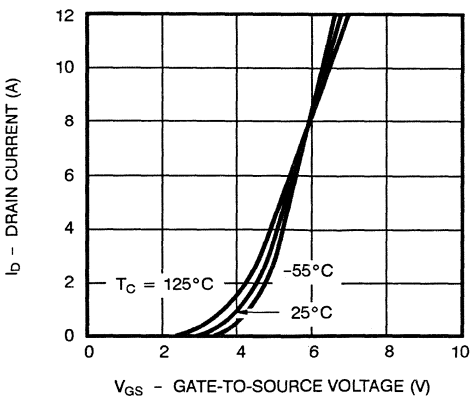


Figure 3. Transconductance

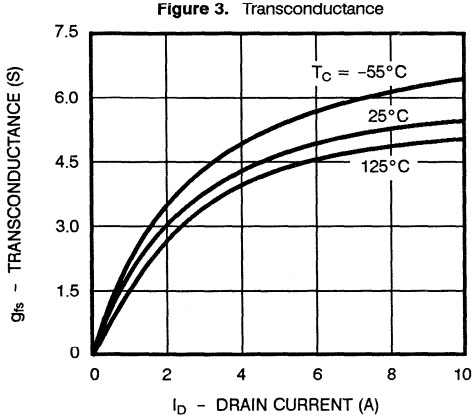


Figure 4. On-Resistance

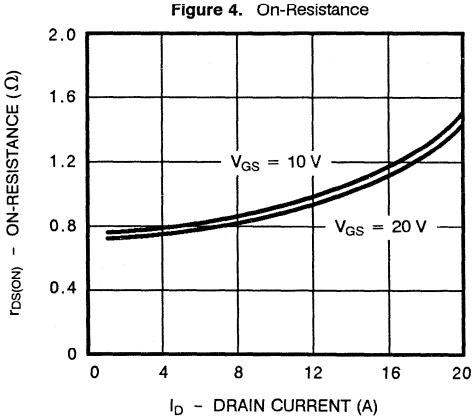


Figure 5. Capacitance

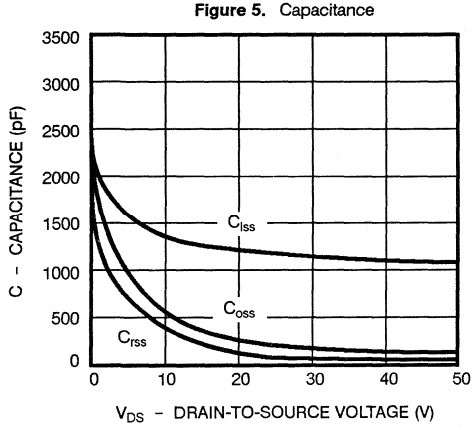
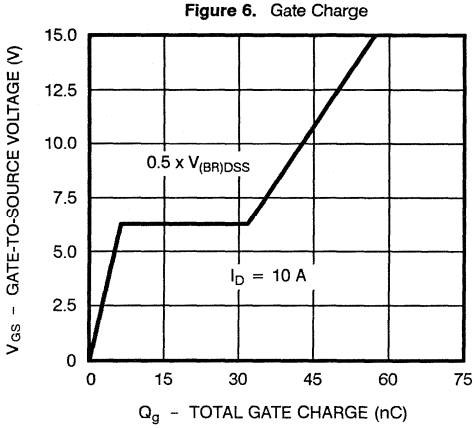


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

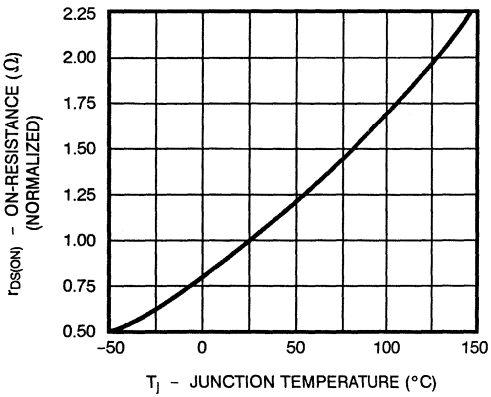
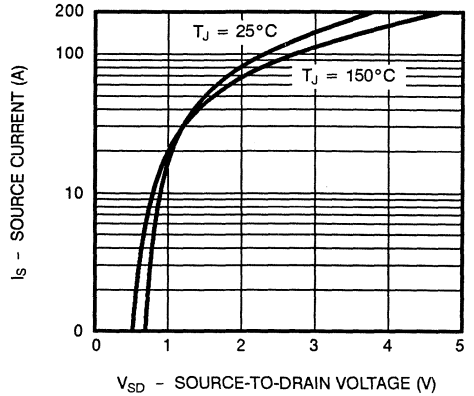


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

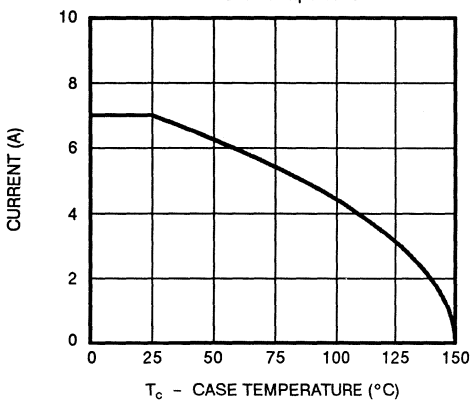
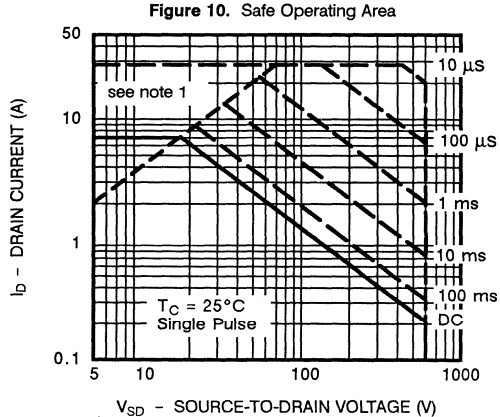
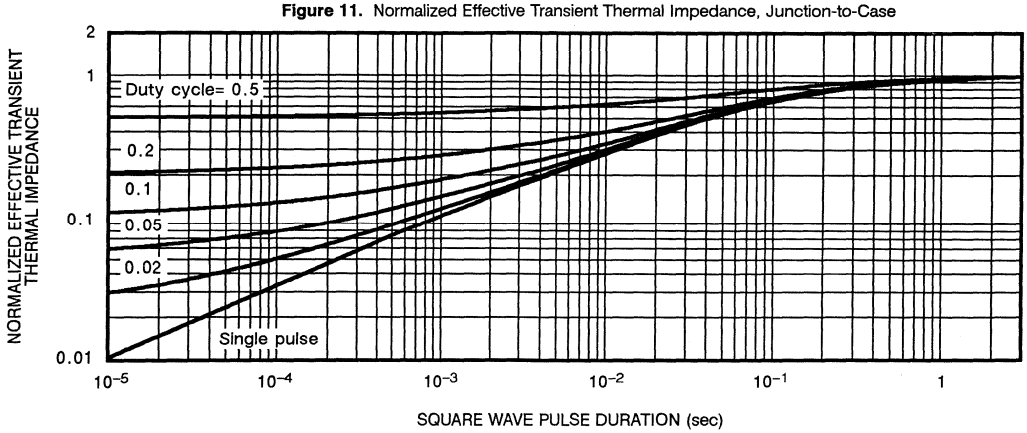


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

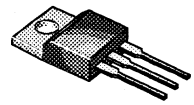
SMP8N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

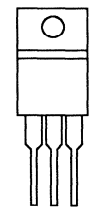
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	0.85	8.0	250

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.0	
Pulsed Drain Current[1]		I_{DM}	32	
Avalanche Current (See Figure 9)		I_{AR}	8.0	
Repetitive Avalanche Energy[2]	L = 1 mH	E_{AR}	32	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			8.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 4 A		0.60		0.85	Ω
		V_{GS} = 10 V, I_D = 4 A, T_J = 125°C		1.20		1.65	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 4 A		4.3	4.0		S
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1360			pF
Output Capacitance	C_{oss}			300			
Reverse Transfer Capacitance	C_{rss}			80			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8 A		45		60	nC
Gate-Source Charge[2]	Q_{gs}			7.5		15	
Gate-Drain Charge[2]	Q_{gd}			25		35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 31 Ω $I_D \simeq$ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω		10		35	ns
Rise Time[2]	t_r			20		25	
Turn-Off Delay Time[2]	$t_{d(off)}$			40		90	
Fall Time[2]	t_f			20		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					8.0	A
Pulsed Current[3]	I_{SM}					32	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				2.0	V
Reverse Recovery Time	t_{rr}	I_F = 8 A, dI_F/dt = 100 A/µs V_{DD} = 250 V	T_J = 25°C	170		250	ns
			T_J = 125°C	240		300	
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C	11			A
			T_J = 125°C	16			
Reverse Recovery Charge	Q_{rr}		T_J = 25°C	0.95		1.6	µC
			T_J = 125°C	2.0		4.0	

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

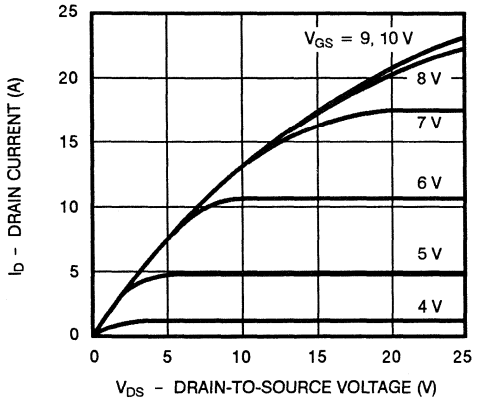


Figure 2. Transfer Characteristics

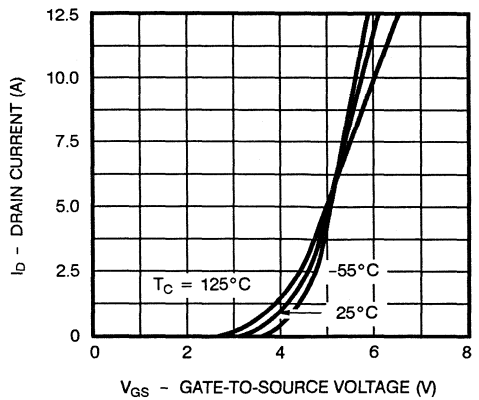


Figure 3. Transconductance

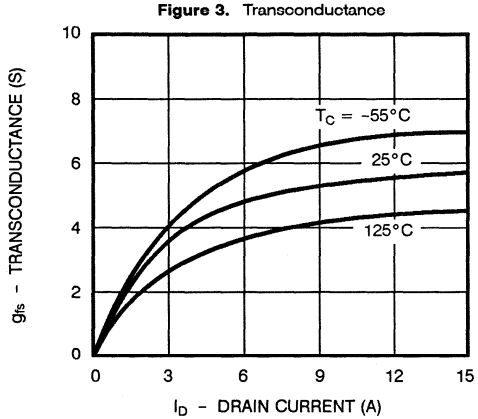


Figure 4. On-Resistance

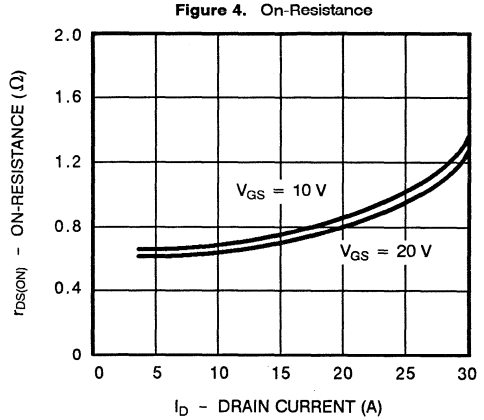


Figure 5. Capacitance

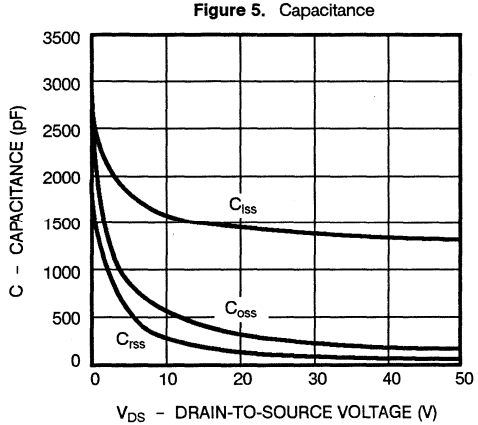
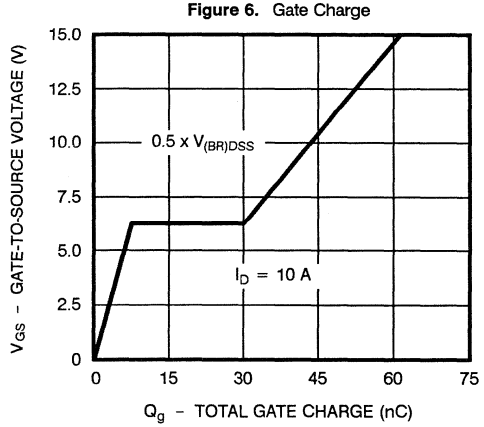


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

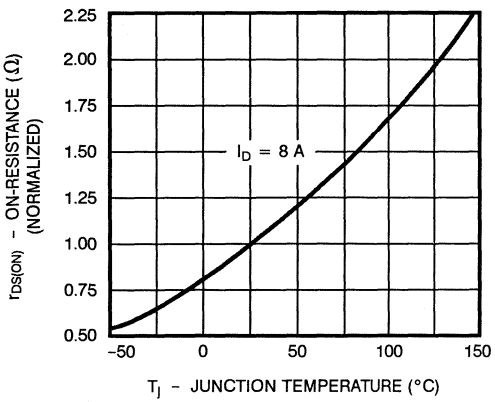
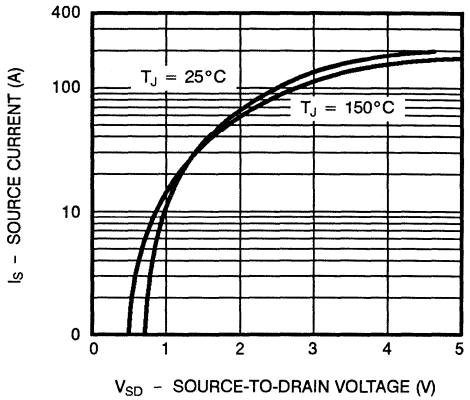


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

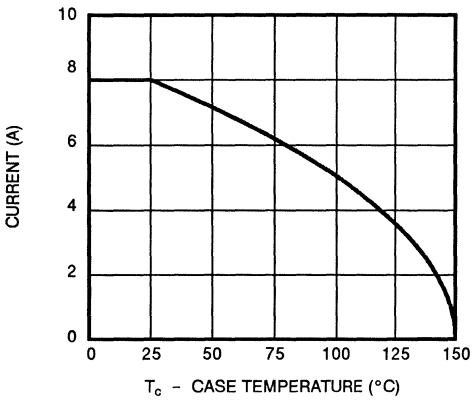
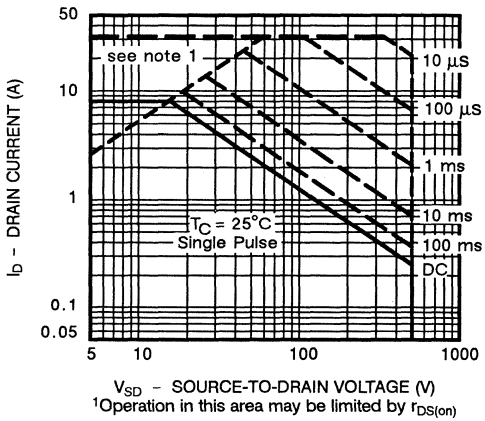
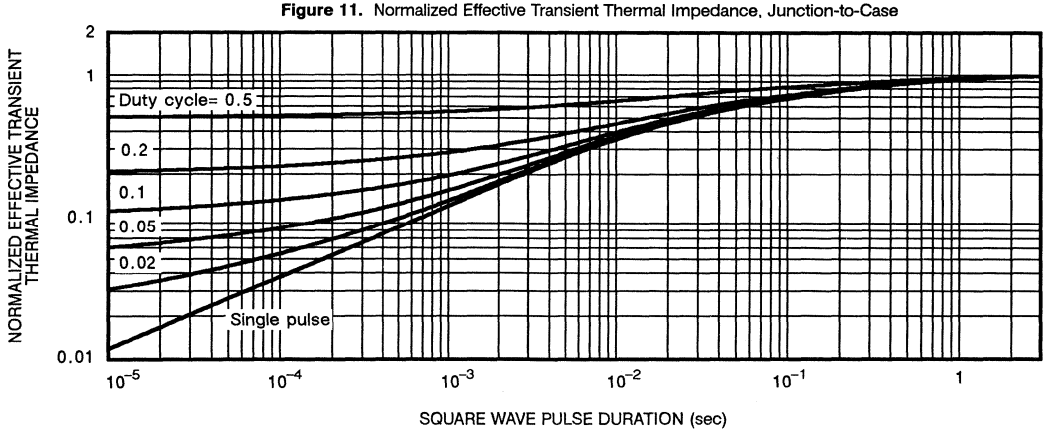


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

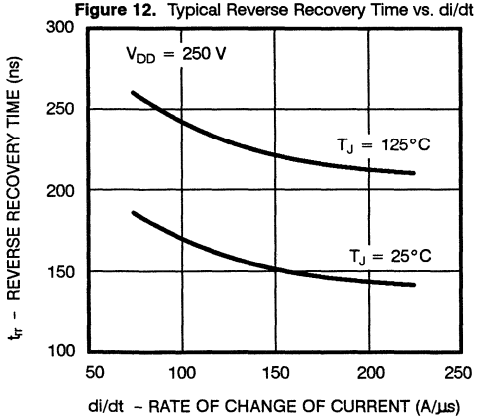


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

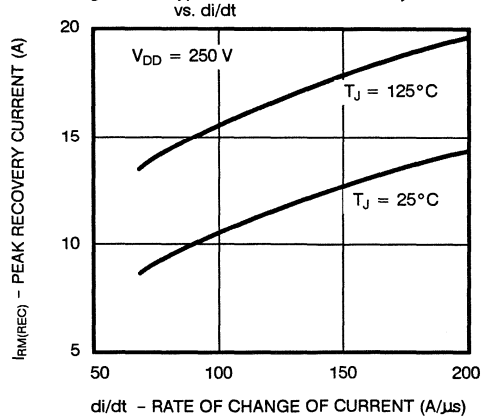


Figure 14. Commutating Safe Operating Area

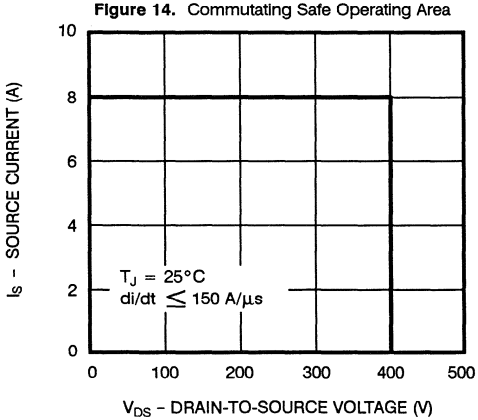


Figure 15. Typical dv/dt vs. di/dt

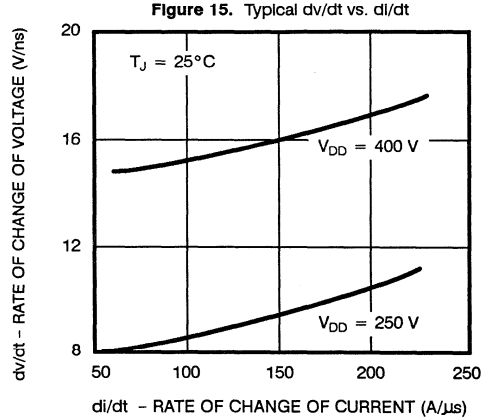
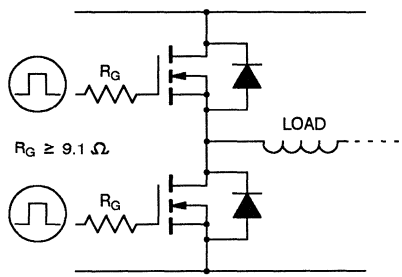
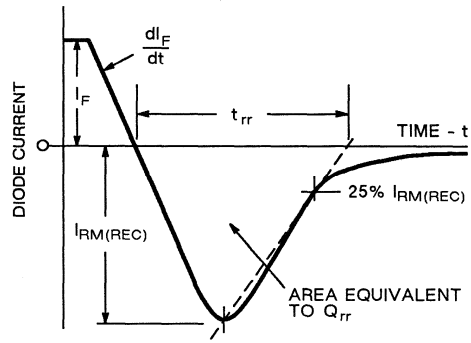


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



4

Siliconix incorporated

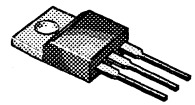
SMP11P20

P-Channel Enhancement Mode Transistor

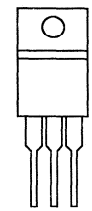
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-11

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	11	A
	T_C = 100°C		7.0	
Pulsed Drain Current[2]		I_{DM}	44	
Avalanche Current (See Figure 9)		I_{AR}	11	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	6.0	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		11.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 6 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 6 A T_J = 125°C	0.50		1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 6 A	4.3	4.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11 A	55		75	nC
Gate-Source Charge[2]	Q_{gs}		9		18	
Gate-Drain Charge[2]	Q_{gd}		30		45	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 15.5 Ω I_D ≃ 6 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		30		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		80	
Fall Time[2]	t_f		16		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				11.0	A
Pulsed Current[3]	I_{SM}				44	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}		200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

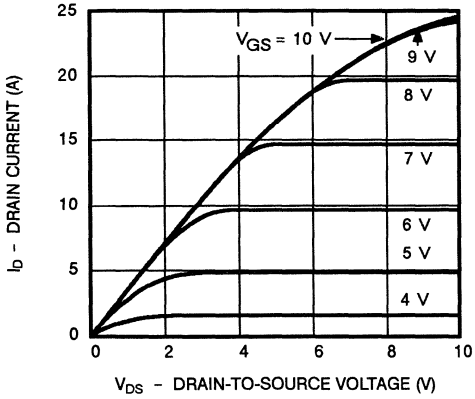


Figure 2. Transfer Characteristics

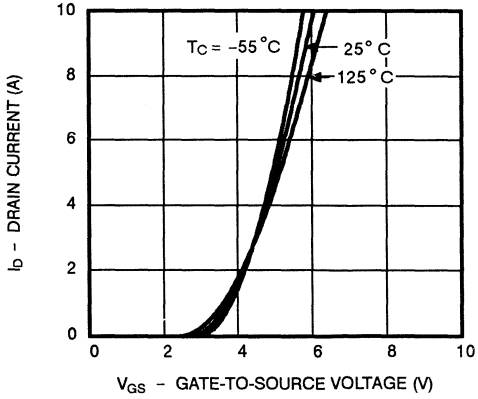


Figure 3. Transconductance

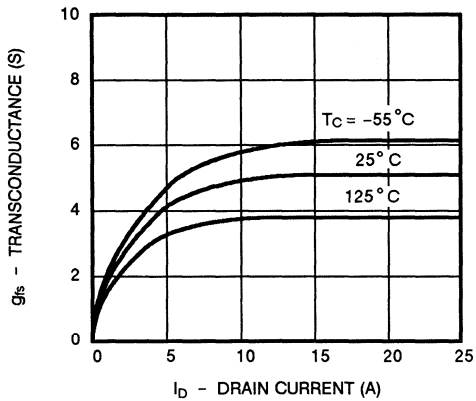


Figure 4. On-Resistance

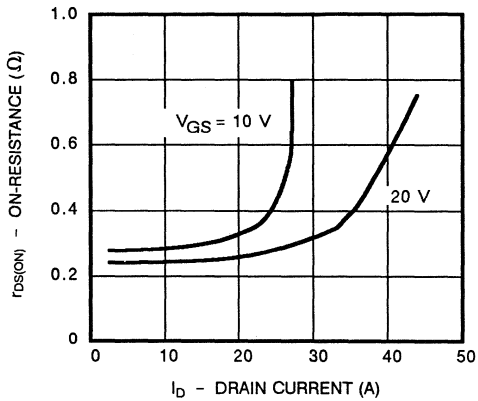


Figure 5. Capacitance

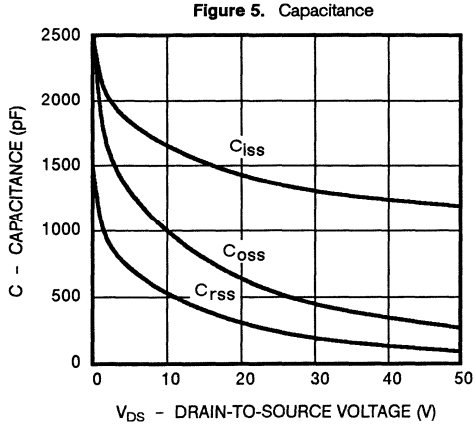
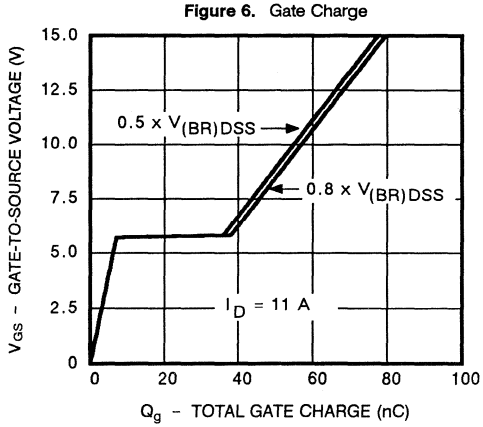


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

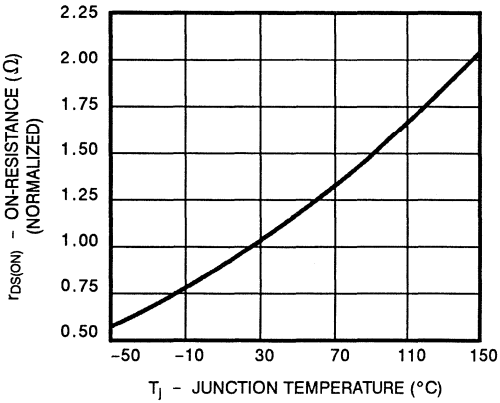
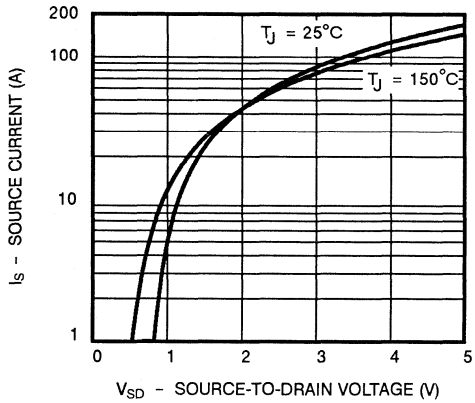


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

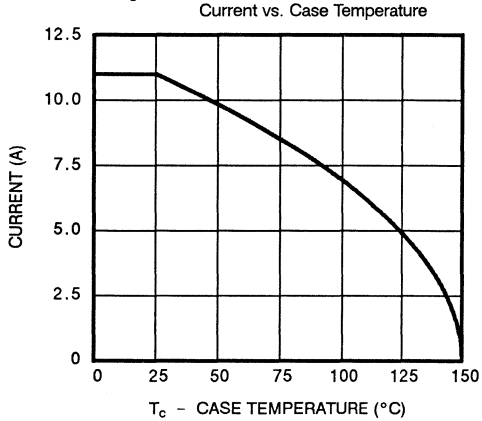
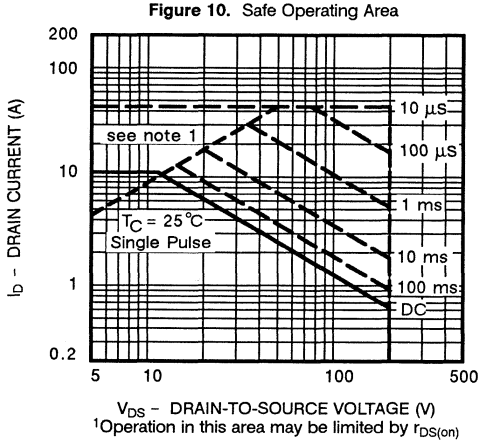
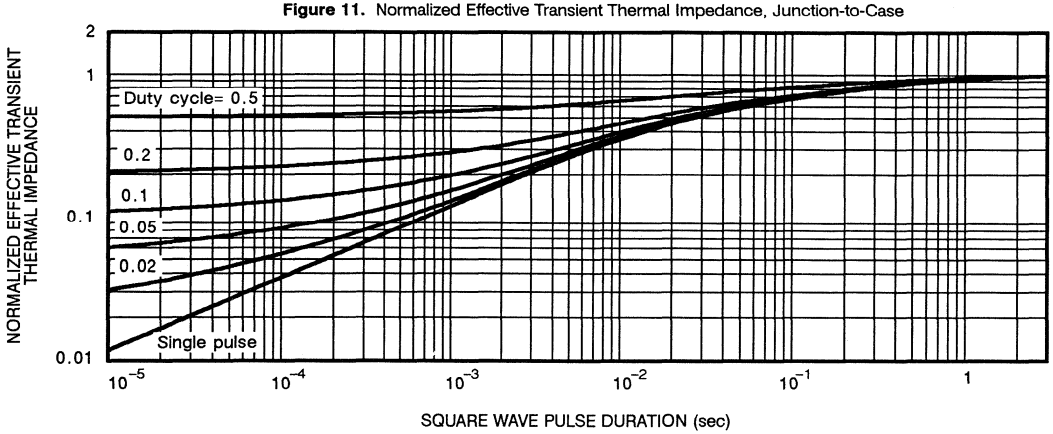


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

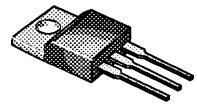
SMP20N20

N-Channel Enhancement Mode Transistor

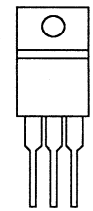
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	0.16	20

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		13	
Pulsed Drain Current[1]		I_{DM}	80	
Avalanche Current (See Figure 9)		I_{AR}	20	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	20	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 A	0.12		0.16	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	0.25		0.32	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	9	6.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		290			
Reverse Transfer Capacitance	C_{rss}		110			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	57		70	nC
Gate-Source Charge[2]	Q_{gs}		9		16	
Gate-Drain Charge[2]	Q_{gd}		35		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 75 V, R_L = 7.5 Ω, I_D ≃ 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		30	ns
Rise Time[2]	t_r		32		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		55		80	
Fall Time[2]	t_f		20		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				80	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	0.9		2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	280			ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 100 V	2.8			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

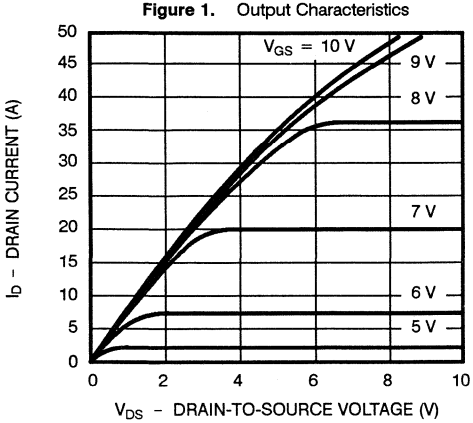


Figure 2. Transfer Characteristics

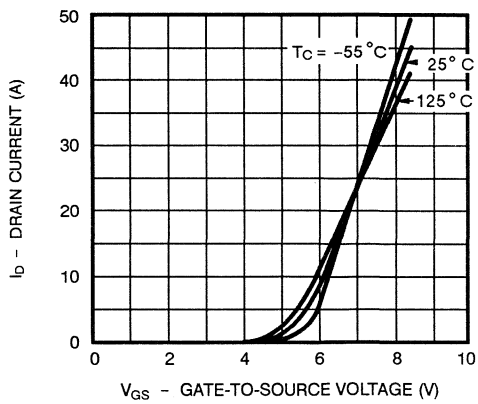


Figure 3. Transconductance

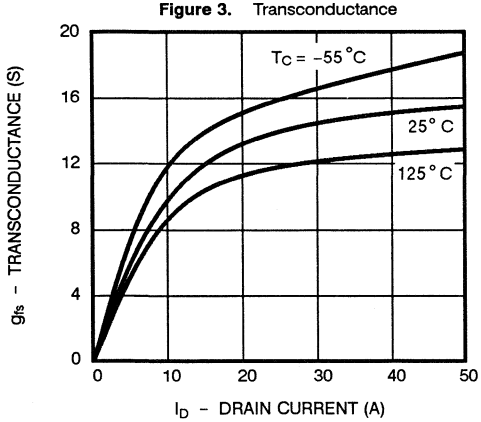


Figure 4. On-Resistance

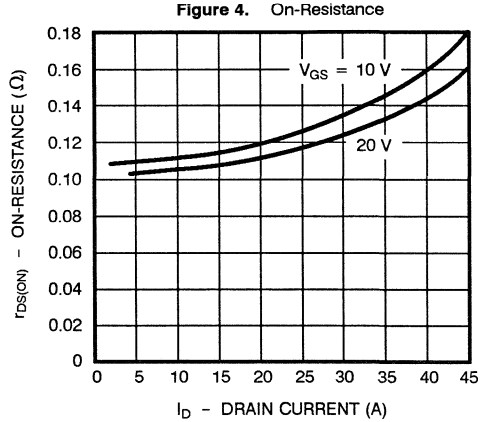


Figure 5. Capacitance

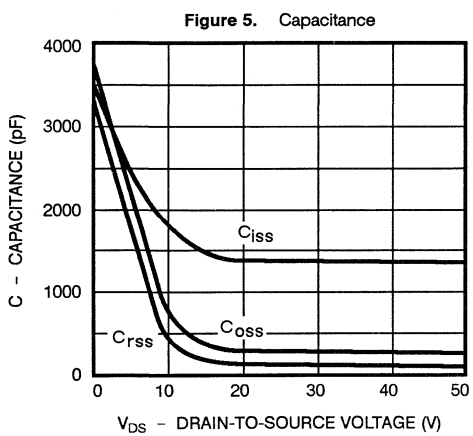
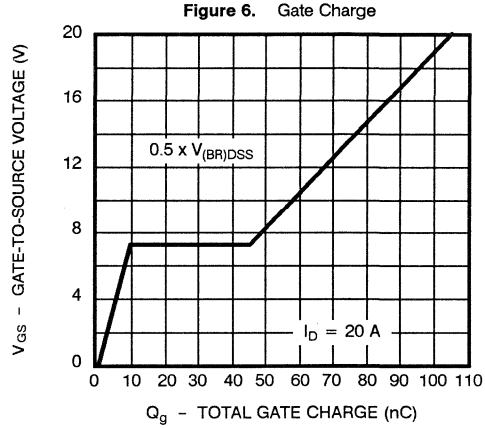


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

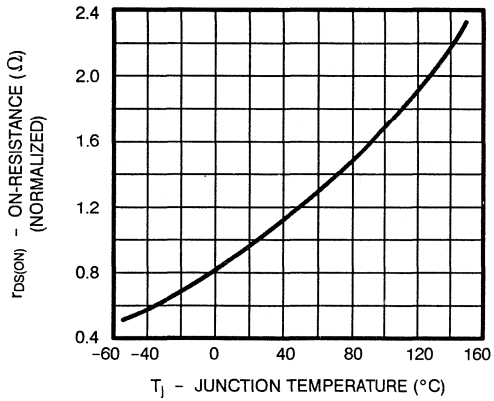
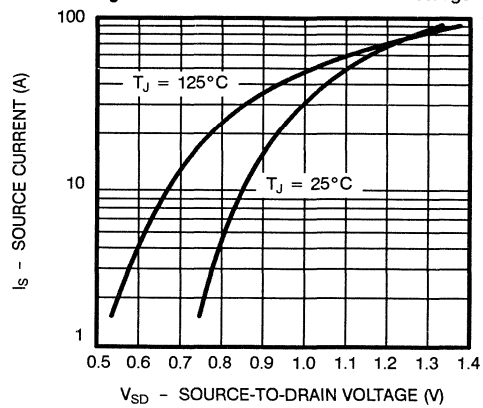


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

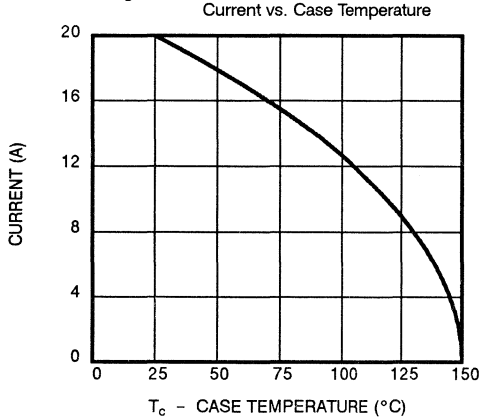
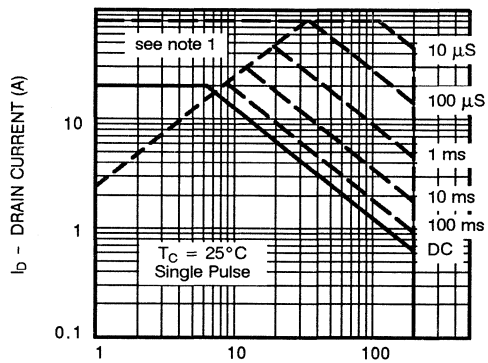
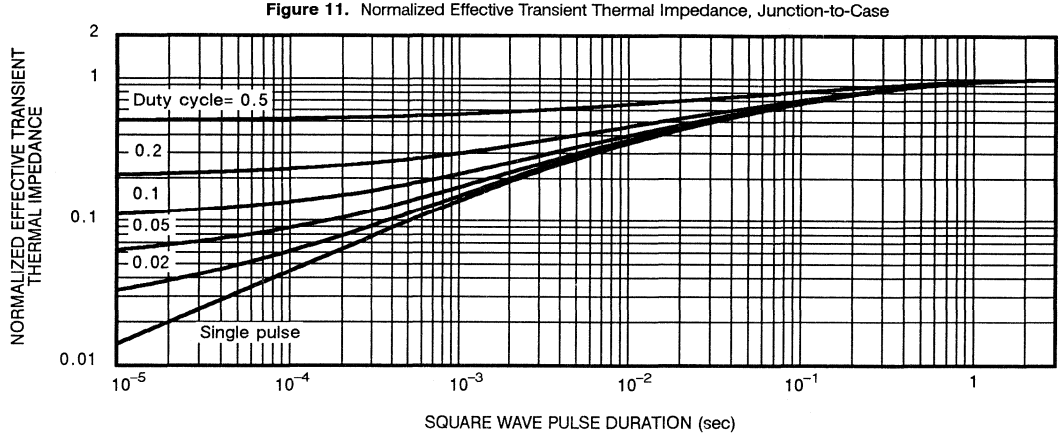


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

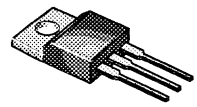
SMP20P10

P-Channel Enhancement Mode Transistor

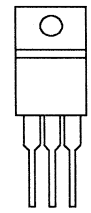
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	0.20	-20

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		13	
Pulsed Drain Current[2]		I_{DM}	80	
Avalanche Current (See Figure 9)		I_{AR}	20	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	20	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 A	0.15		0.20	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	0.24		0.30	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	6.7	4.8		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		310			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	47		60	nC
Gate-Source Charge[2]	Q_{gs}		10		18	
Gate-Drain Charge[2]	Q_{gd}		27		36	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω, I_D ≃ 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		80	
Fall Time[2]	t_f		15		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				80	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.70	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

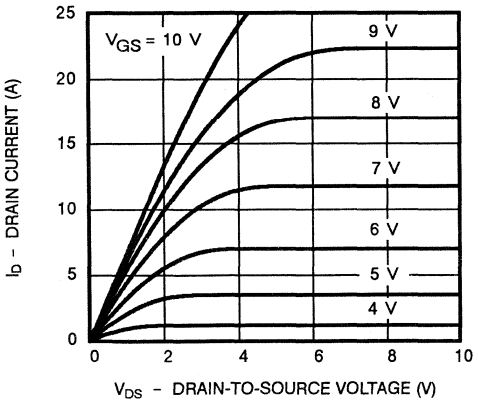


Figure 2. Transfer Characteristics

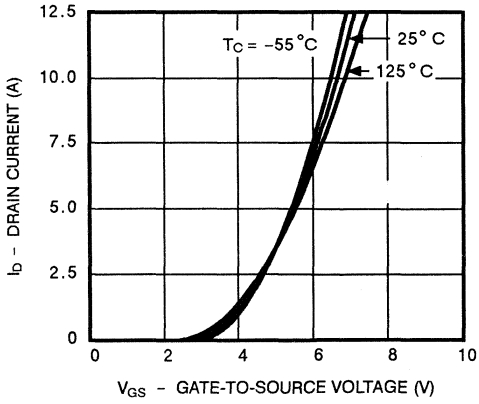


Figure 3. Transconductance

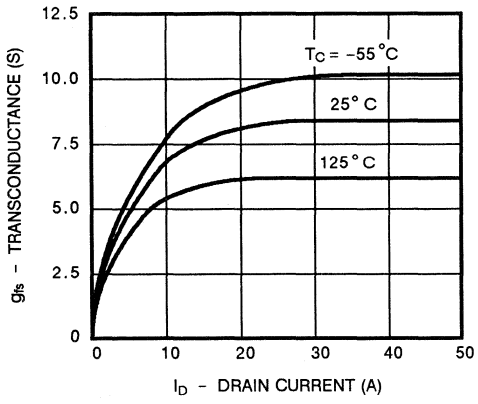


Figure 4. On-Resistance

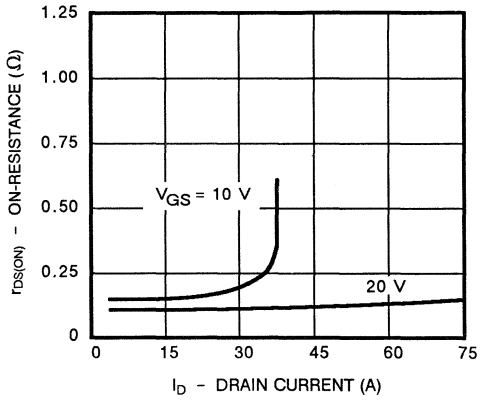


Figure 5. Capacitance

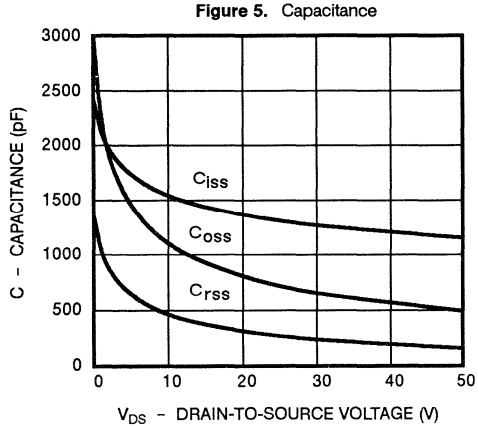
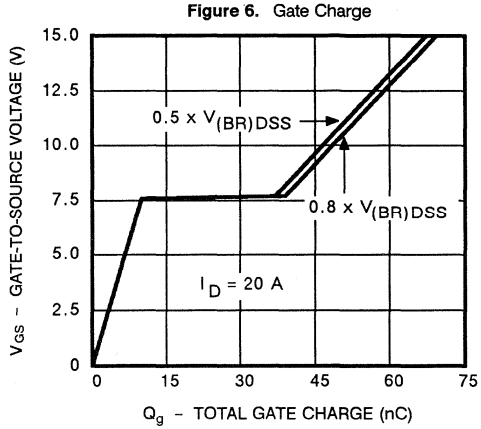


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

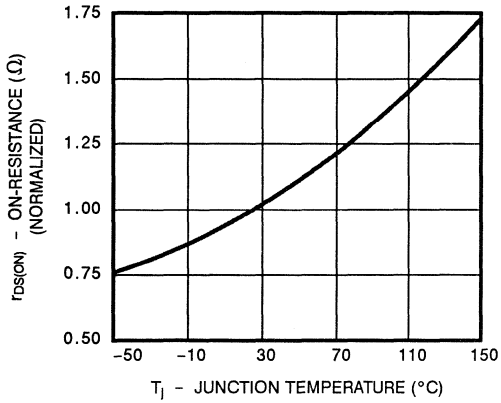
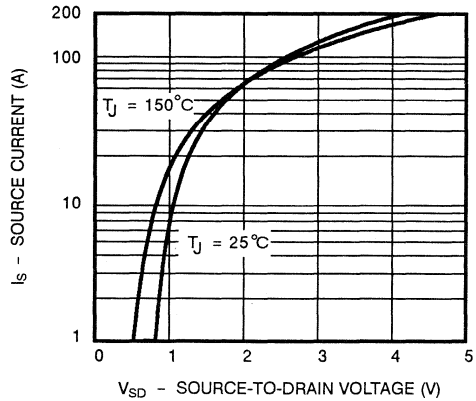


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

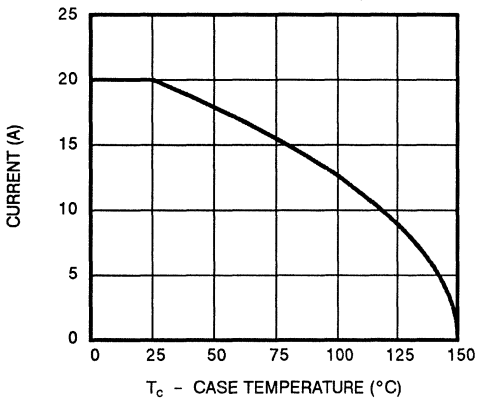
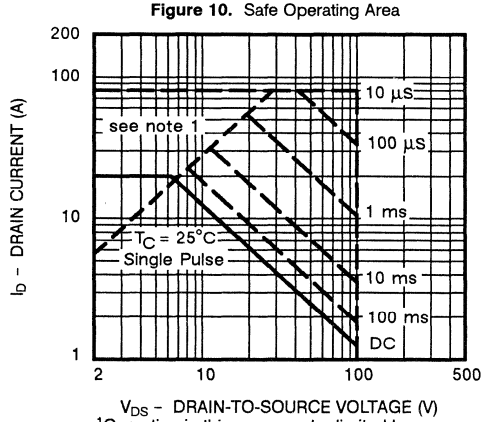
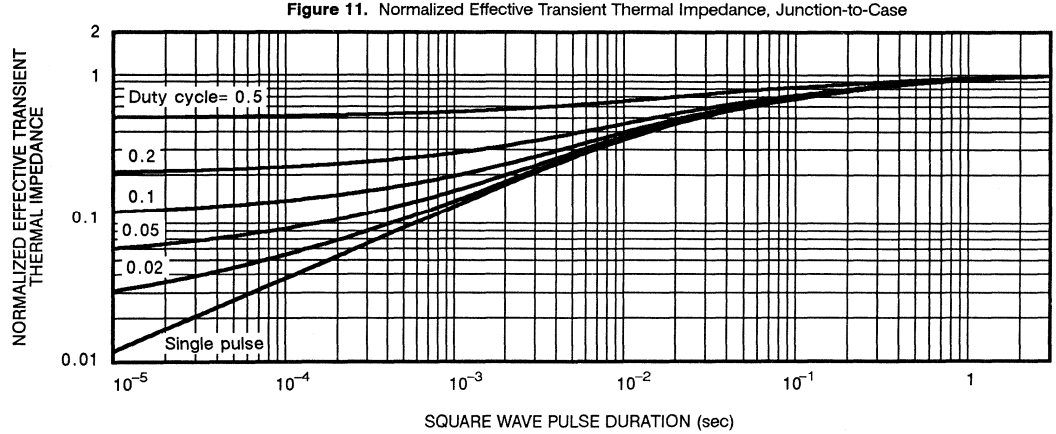


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

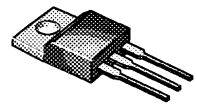


Siliconix incorporated

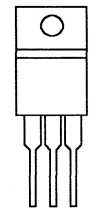
SMP25N05-45L

N-Channel Enhancement Mode Transistor
Logic Level

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
50	0.045	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		16	
Pulsed Drain Current[1]		I_{DM}	100	
Avalanche Current (See Figure 9)		I_{AR}	25	
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	31	mJ
Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		24	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.08	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%.

4

Advance Information

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.8	1.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		25		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.035		0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.060		0.080	
		V_{GS} = 5 V, I_D = 12.5 A	0.045		0.070	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	16			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	800			pF
Output Capacitance	C_{oss}		320			
Reverse Transfer Capacitance	C_{rss}		90			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	27			nC
Gate-Source Charge[2]	Q_{gs}		6			
Gate-Drain Charge[2]	Q_{gd}		8			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω, I_D ≃ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		20	ns
Rise Time[2]	t_r		20		40	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				25	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	90			ns
Peak Reverse Recovery Time	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

Siliconix incorporated

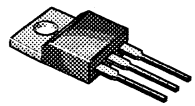
SMP25N06, SMP25N05

N-Channel Enhancement Mode Transistors

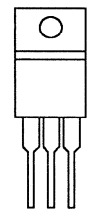
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
SMP25N06	60	0.060	25
SMP25N05	50	0.060	25

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SMP25N06	LIMITS SMP25N05	UNITS
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	25	25	A
	T_C = 100°C		16	16	
Pulsed Drain Current[1]		I_{DM}	100	100	
Avalanche Current (See Figure 9)		I_{AR}	25	25	
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	15	15	mJ
Power Dissipation	T_C = 25°C	P_D	85	85	W
	T_C = 100°C		34	34	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.47	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	SMP25N06	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	65	60		V
	SMP25N05			60	50		
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA	3.3	2.0	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]		$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V	35	25		A
Drain-Source On-State Resistance[1]		$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.05		0.060	Ω
			V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.08		0.11	
Forward Transconductance[1]		g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	9.0	5.0		S
DYNAMIC							
Input Capacitance		C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1020			pF
Output Capacitance		C_{oss}		500			
Reverse Transfer Capacitance		C_{rss}		120			
Total Gate Charge[2]		Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	28		40	nC
Gate-Source Charge[2]		Q_{gs}		8		15	
Gate-Drain Charge[2]		Q_{gd}		15		22	
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 30 V, R_L = 2.4 Ω, I_D ≃ 12.5 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		50	ns
Rise Time[2]		t_r		20		75	
Turn-Off Delay Time[2]		$t_{d(off)}$		25		50	
Fall Time[2]		t_f		15		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current		I_S				25	A
Pulsed Current[3]		I_{SM}				100	
Forward Voltage[1]		V_{SD}	I_F = I_S, V_{GS} = 0 V	1.25		2.4	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	100			ns
Reverse Recovery Charge		Q_{rr}		0.15			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

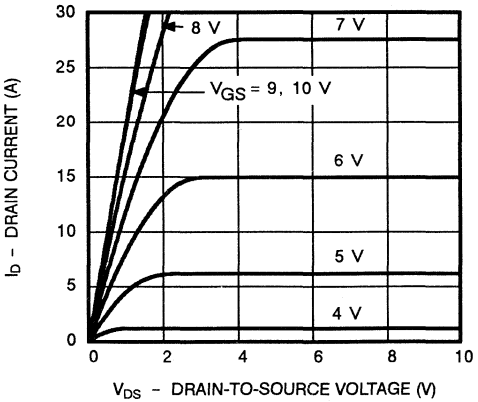


Figure 2. Transfer Characteristics

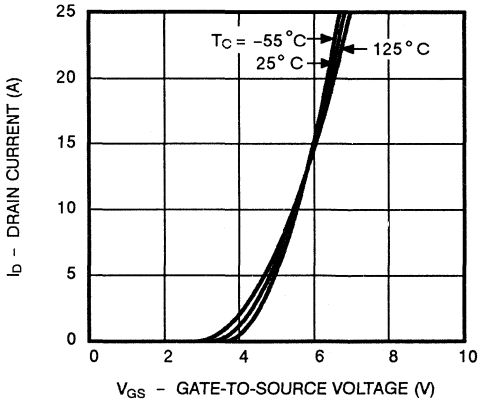


Figure 3. Transconductance

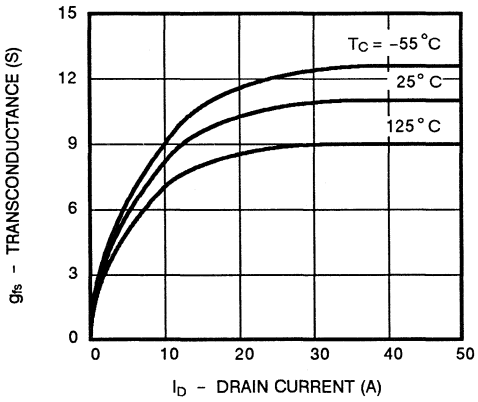


Figure 4. On-Resistance

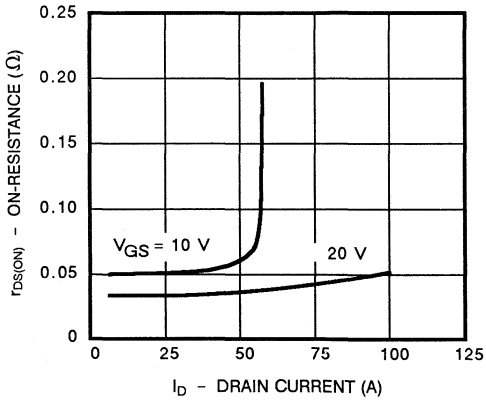


Figure 5. Capacitance

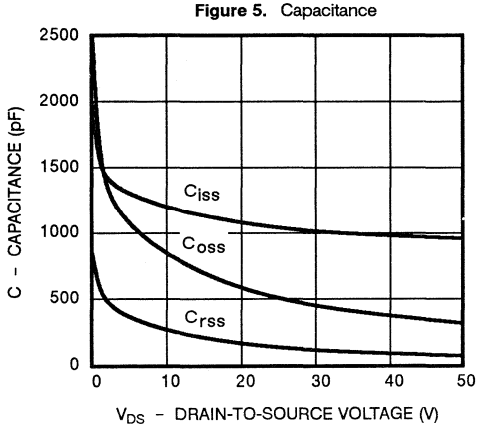
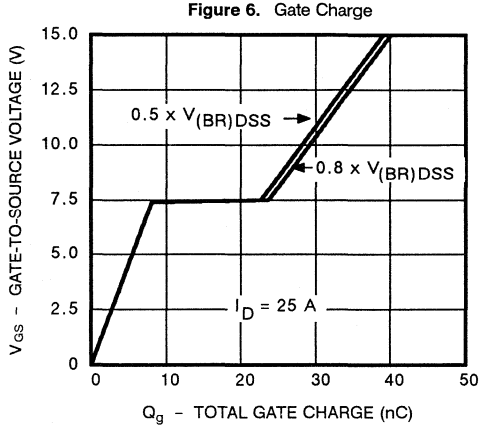


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

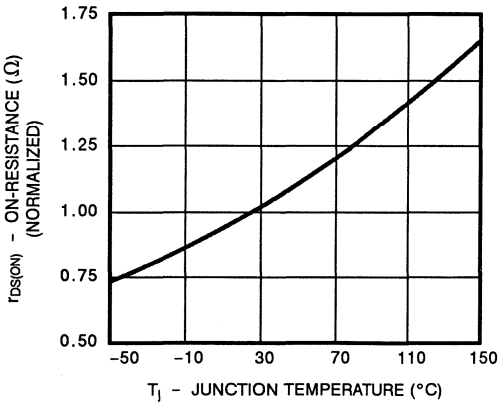
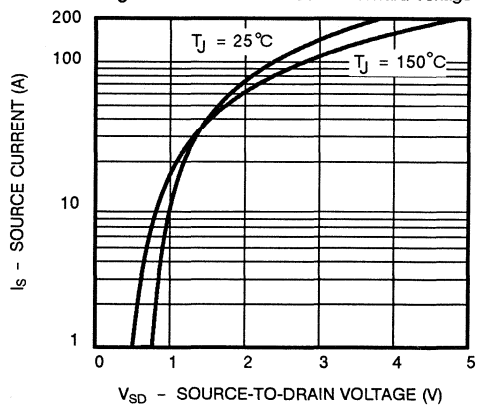


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

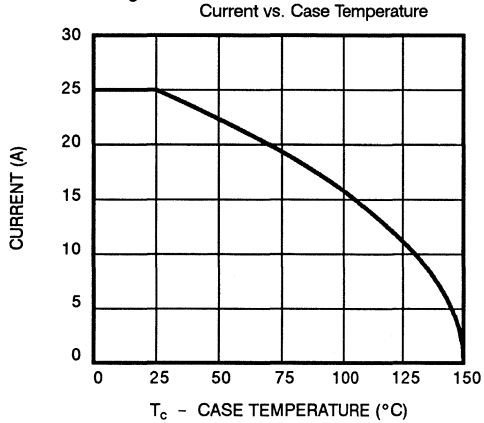
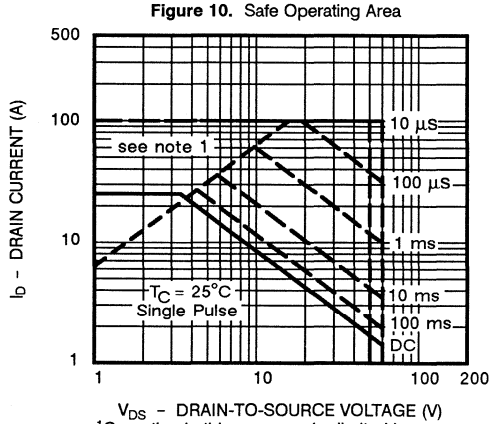
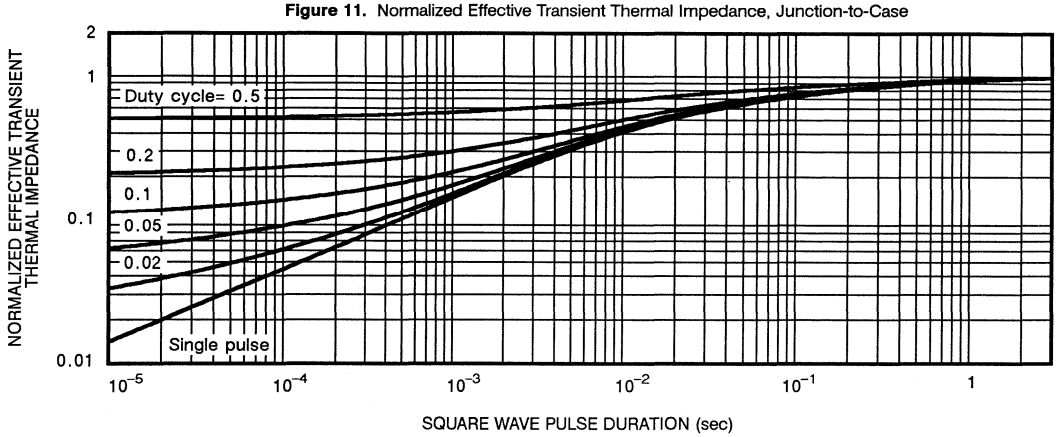


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

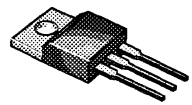
SMP30N10

N-Channel Enhancement Mode Transistor

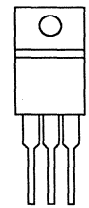
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.060	30

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		18	
Pulsed Drain Current[1]		I_{DM}	120	
Avalanche Current (See Figure 9)		I_{AR}	30	
Avalanche Energy	L = 0.3 mH	E_A	135	mJ
Repetitive Avalanche Energy[2]	L = 0.1 mH	E_{AR}	45	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	110	100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		30		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 18 A	0.045		0.060	Ω
		V_{GS} = 10 V, I_D = 18 A, T_J = 125°C	0.085		0.100	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 18 A	10.0	7.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1500			pF
Output Capacitance	C_{oss}		480			
Reverse Transfer Capacitance	C_{rss}		110			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A	35		50	nC
Gate-Source Charge[2]	Q_{gs}		10		19	
Gate-Drain Charge[2]	Q_{gd}		15		25	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.67 Ω, I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		80		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		30		60	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				30	A
Pulsed Current[3]	I_{SM}				120	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}		130			ns
Reverse Recovery Charge	Q_{rr}		0.45			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

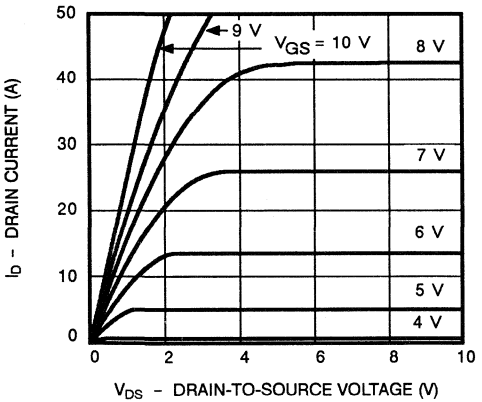


Figure 2. Transfer Characteristics

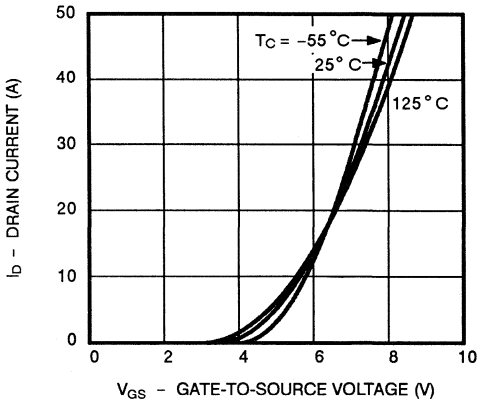


Figure 3. Transconductance

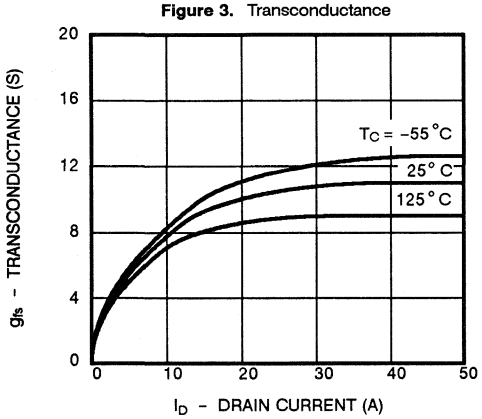


Figure 4. On-Resistance

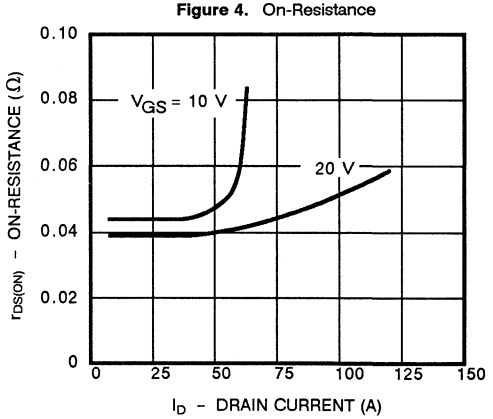


Figure 5. Capacitance

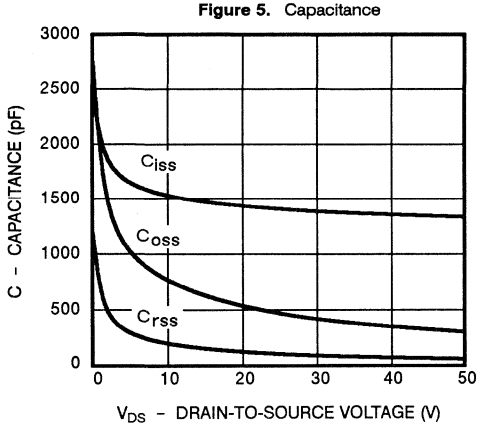
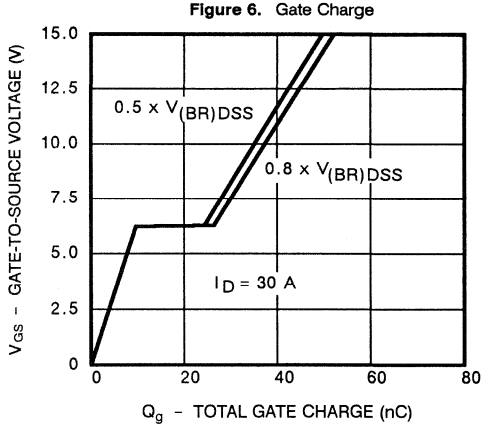


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

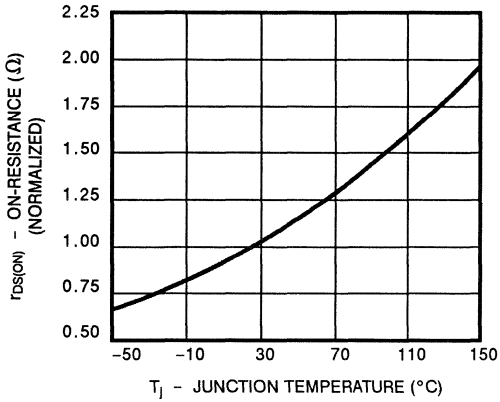
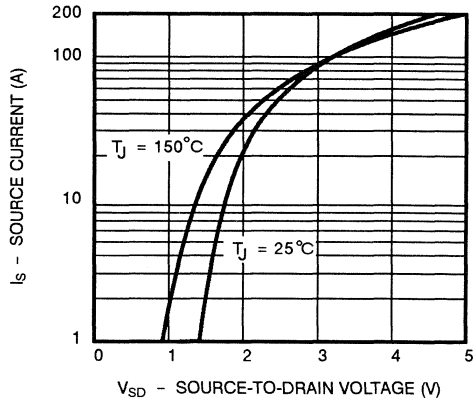


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

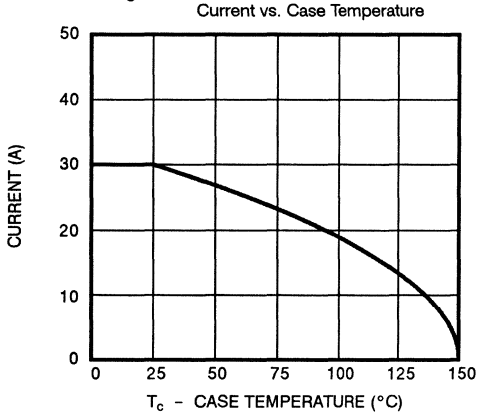
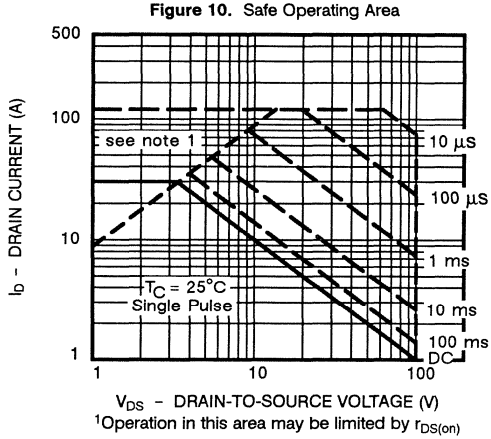
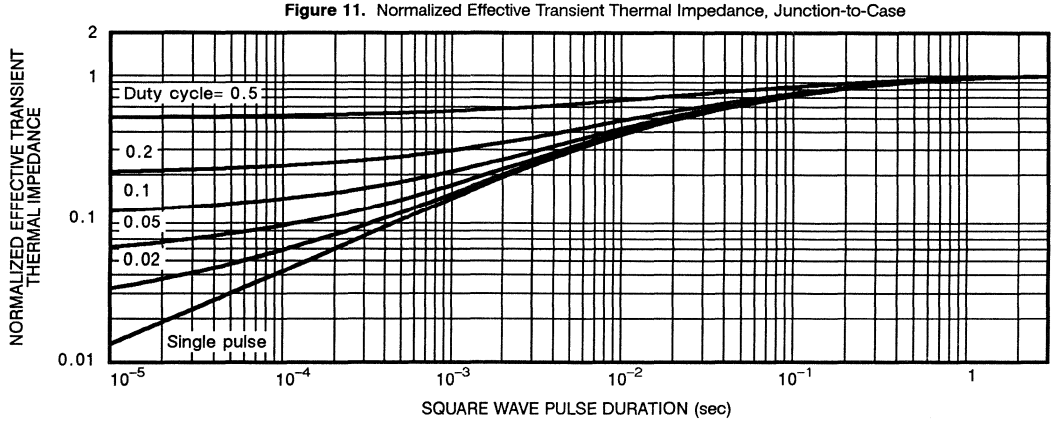


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

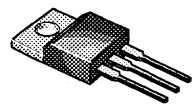
SMP40N10

N-Channel Enhancement Mode Transistor

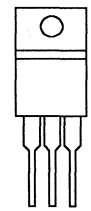
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.040	40

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	40	A
	T_C = 100°C		25	
Pulsed Drain Current[1]		I_{DM}	160	
Avalanche Current (See Figure 9)		I_{AR}	40	
Avalanche Energy	L = 0.3 mH	E_A	240	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	40	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		40		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 25 A	0.030		0.040	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C	0.055		0.072	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	20	15		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3000			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		150			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 40 A	62		80	nC
Gate-Source Charge[2]	Q_{gs}		20		30	
Gate-Drain Charge[2]	Q_{gd}		26		35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.25 Ω, $I_D \simeq$ 40 A, V_{GEN} = 10 V, R_G = 5 Ω	17		30	ns
Rise Time[2]	t_r		80		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				40	A
Pulsed Current[3]	I_{SM}				180	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}		120		250	ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

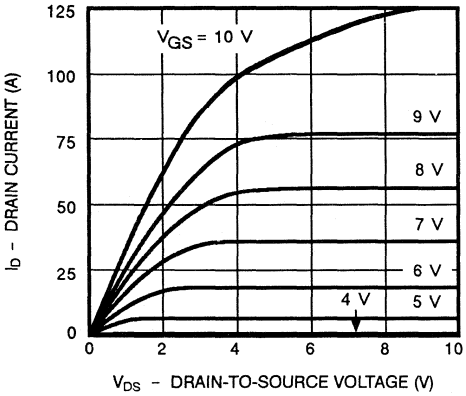


Figure 2. Transfer Characteristics

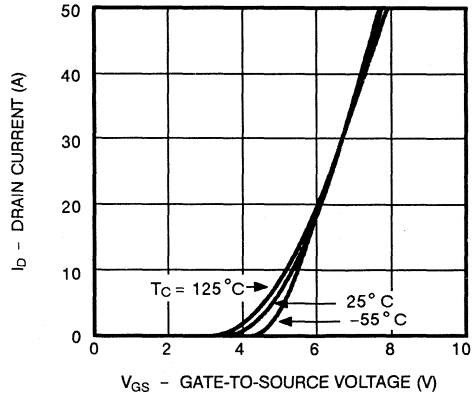


Figure 3. Transconductance

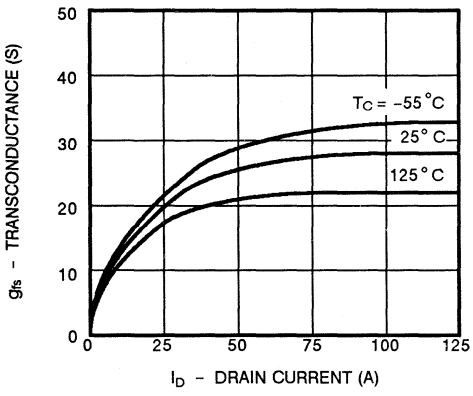


Figure 4. On-Resistance

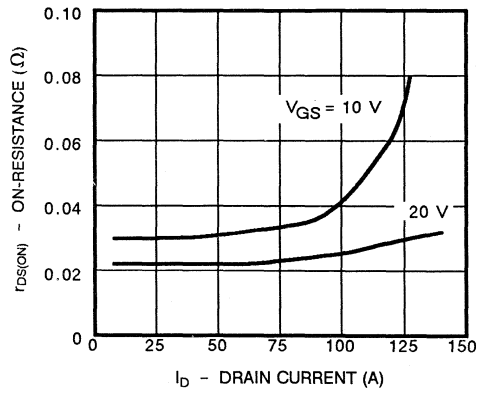


Figure 5. Capacitance

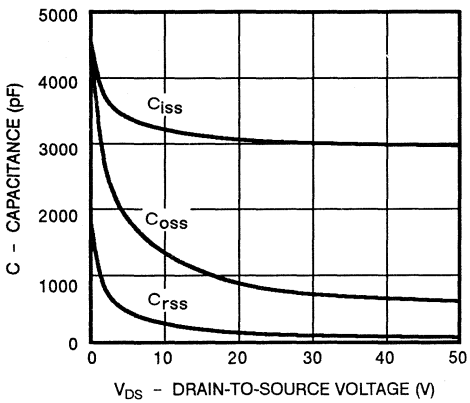
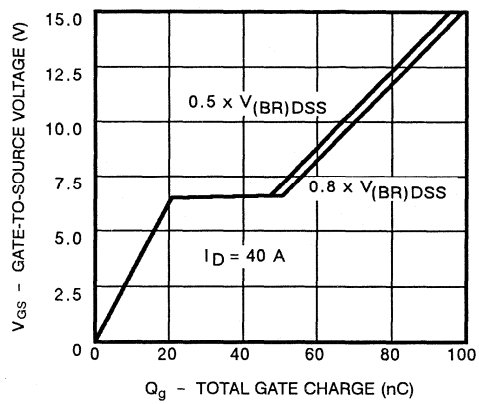


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

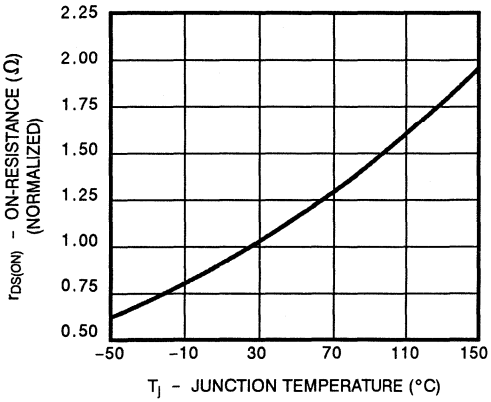
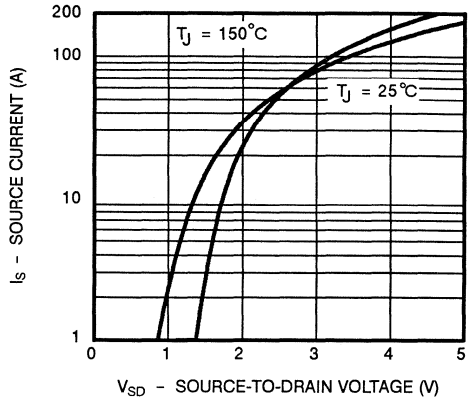


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

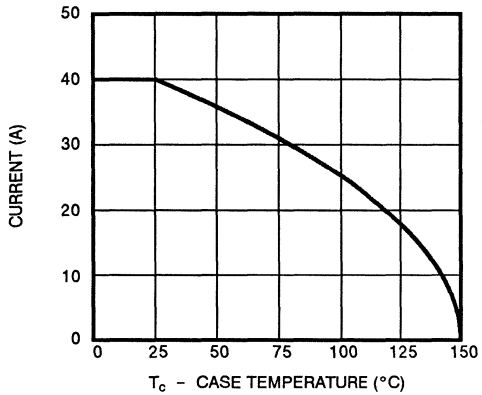
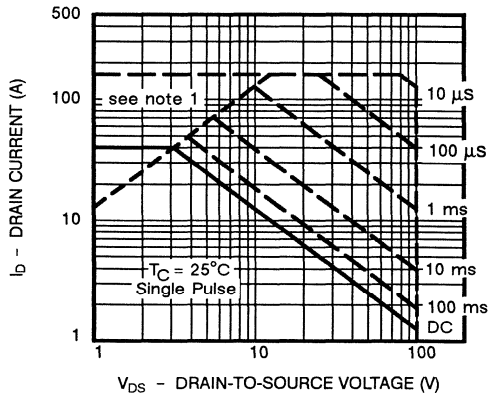
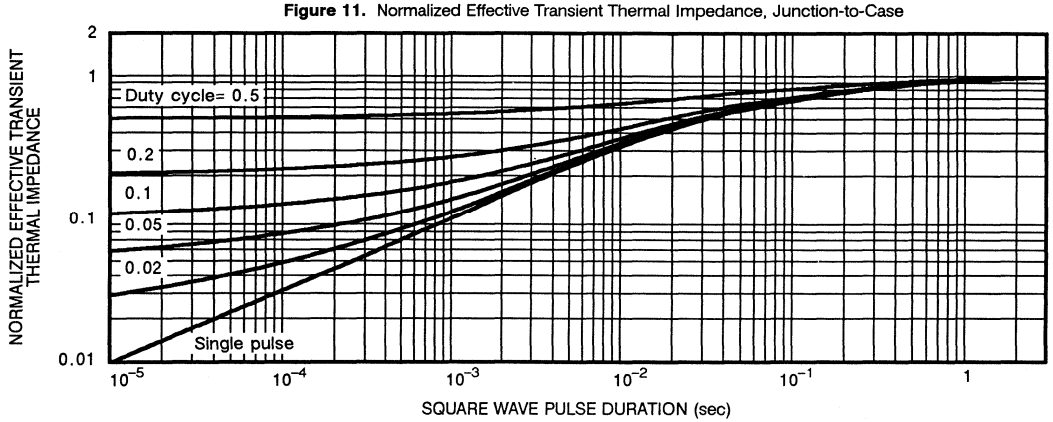


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

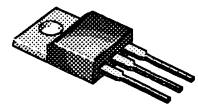
SMP50N06-25

N-Channel Enhancement Mode Transistor
25 milli ohm $r_{DS(ON)}$

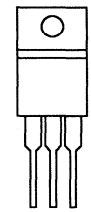
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.025	46

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	46	A
	T_C = 100°C		28	
Pulsed Drain Current[1]		I_{DM}	200	
Avalanche Current		I_{AR}	46	
Avalanche Energy	L = 0.1 mH	E_{AS}	125	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	62.5	
Power Dissipation	T_C = 25°C	P_D	90	W
	T_C = 100°C		36	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.4	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

Preliminary

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		50		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 25 A	0.020		0.025	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C	0.033		0.042	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	20			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1875			pF
Output Capacitance	C_{oss}		570			
Reverse Transfer Capacitance	C_{rss}		120			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A	55		80	nC
Gate-Source Charge[2]	Q_{gs}		9		15	
Gate-Drain Charge[2]	Q_{gd}		24		40	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.6 Ω, I_D ≃ 50 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				46	A
Pulsed Current[3]	I_{SM}				200	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		10			A
Reverse Recovery Charge	Q_{rr}		0.7			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

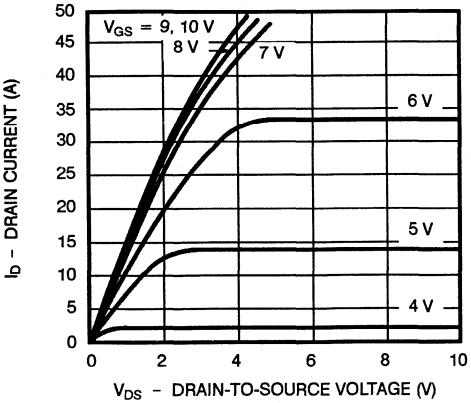


Figure 2. Transfer Characteristics

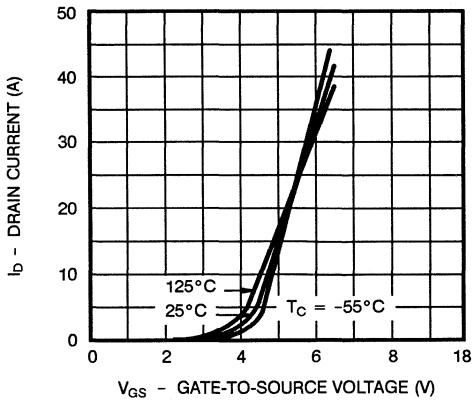


Figure 3. Transconductance

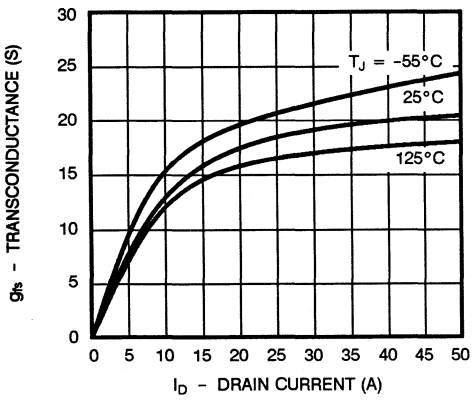


Figure 4. On-Resistance

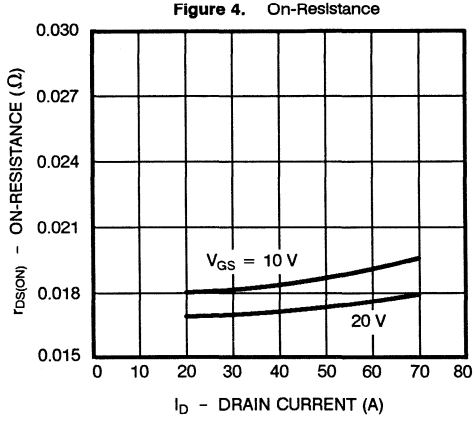


Figure 5. Capacitance

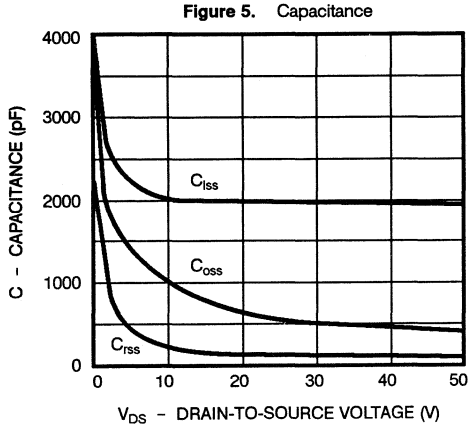
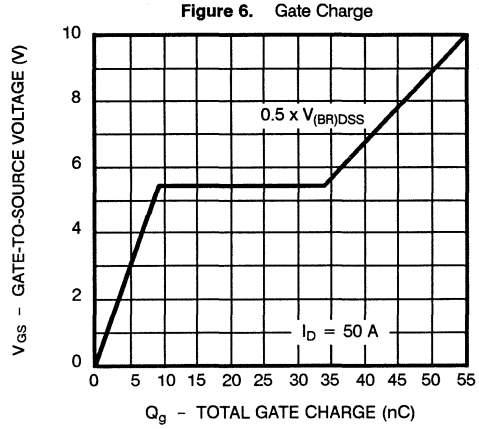


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

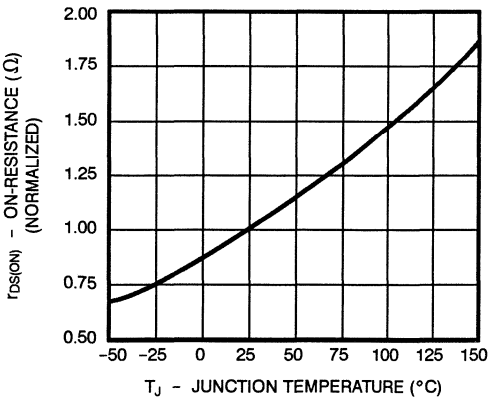
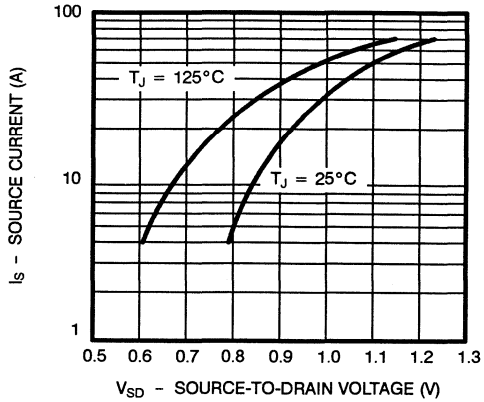


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

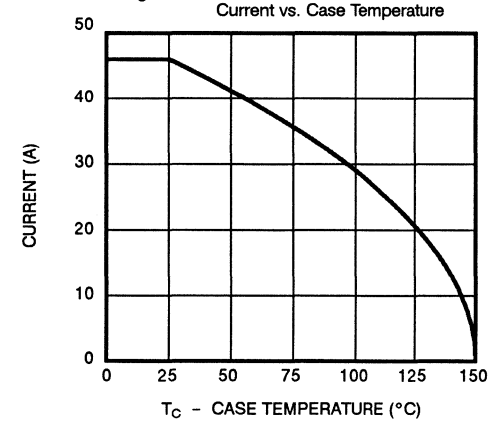
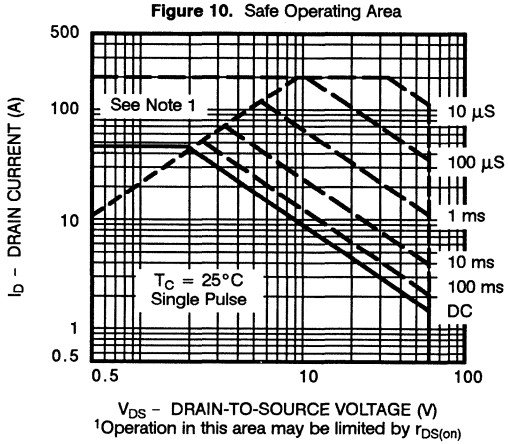
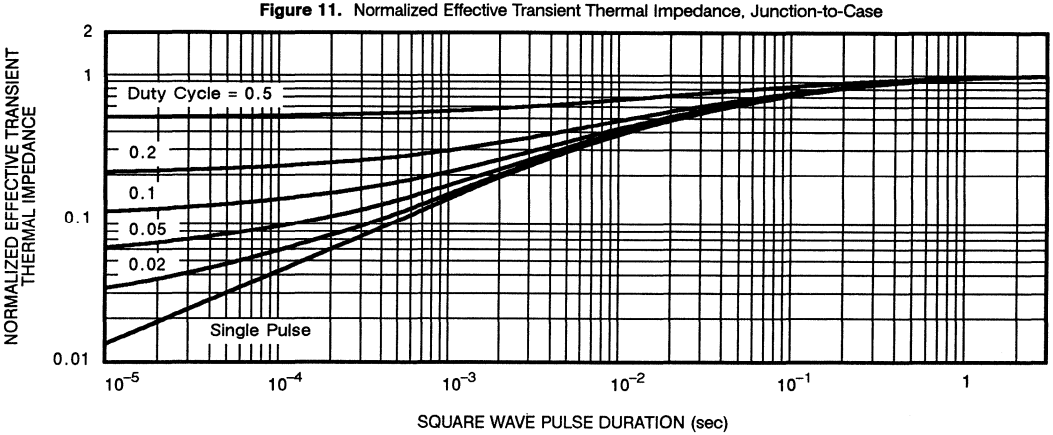


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

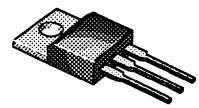
SMP60N03-10L

N-Channel Enhancement Mode Transistor
10 milli ohm $r_{DS(ON)}$
Logic Level

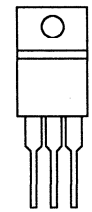
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
30	0.010	60

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		51	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.2	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%.

Advance Information

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		0.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.07		0.010	Ω
		V_{GS} = 5 V, I_D = 30 A	0.10		0.015	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.09		0.014	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		1700			
Reverse Transfer Capacitance	C_{rss}		750			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	100			nC
Gate-Source Charge[2]	Q_{gs}		10			
Gate-Drain Charge[2]	Q_{gd}		45			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω, I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω				ns
Rise Time[2]	t_r					
Turn-Off Delay Time[2]	$t_{d(off)}$					
Fall Time[2]	t_f					
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

Siliconix incorporated

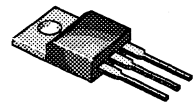
SMP60N06-14

N-Channel Enhancement Mode Transistor

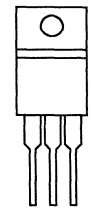
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.014	60[1]

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60[1]	A
	T_C = 100°C		45	
Pulsed Drain Current[2]		I_{DM}	240	
Avalanche Current[3]		I_{AR}	60	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Package limited.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3.0	2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		80		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.012		0.014	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.020		0.023	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	48	30		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3450			pF
Output Capacitance	C_{oss}		1000			
Reverse Transfer Capacitance	C_{rss}		230			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	95		130	nC
Gate-Source Charge[2]	Q_{gs}		20			
Gate-Drain Charge[2]	Q_{gd}		45			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω, I_D ≃ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		100	
Fall Time[2]	t_f		20		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130		200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		9			A
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

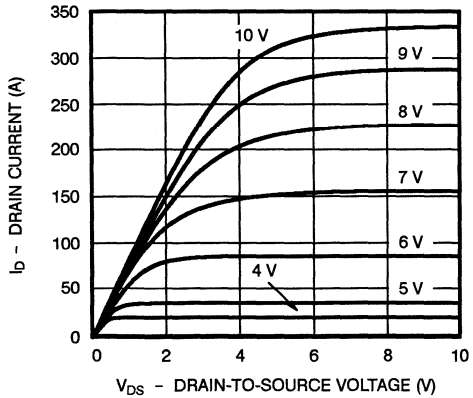


Figure 2. Transfer Characteristics

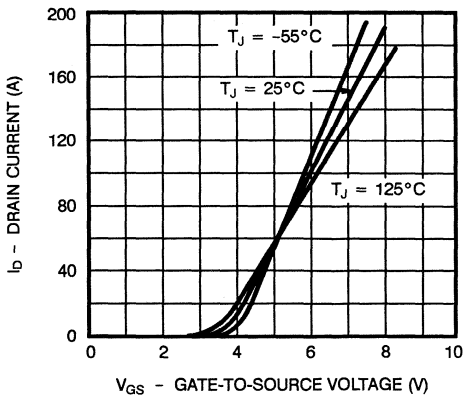


Figure 3. Transconductance

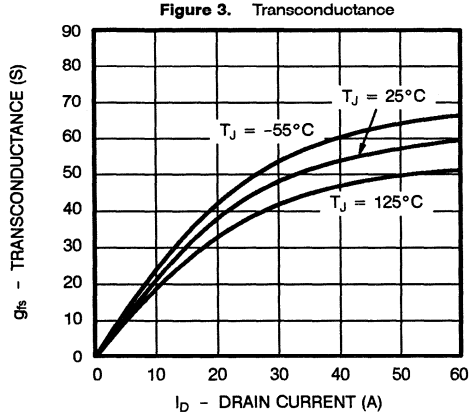


Figure 4. On-Resistance

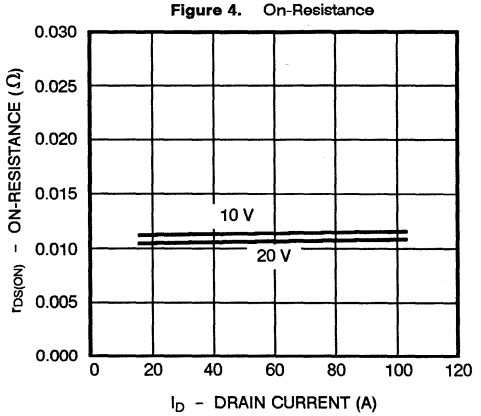


Figure 5. Capacitance

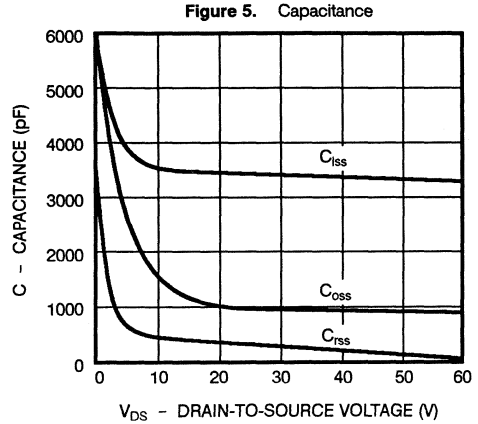
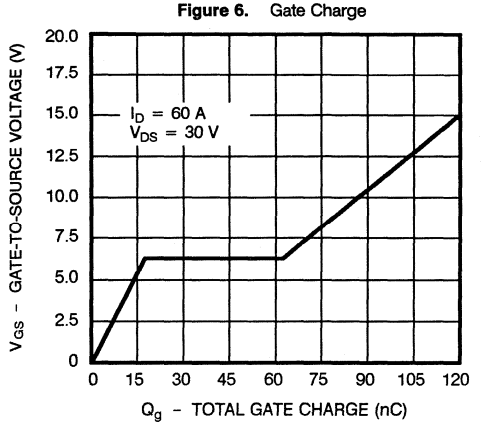


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

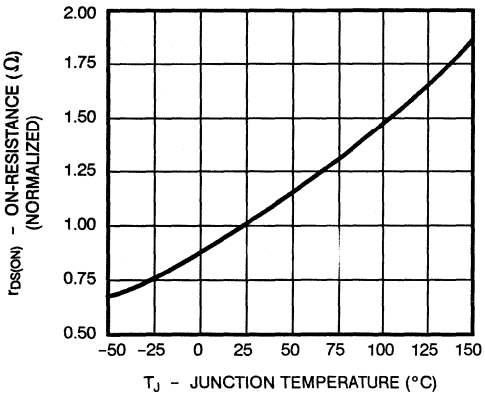
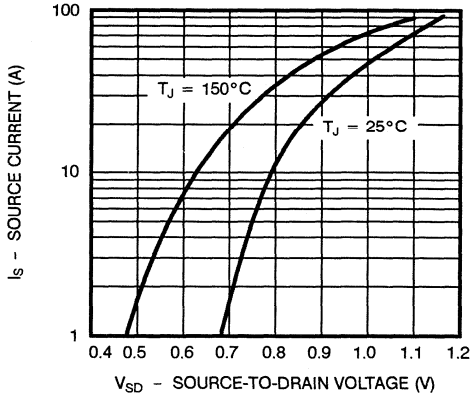


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

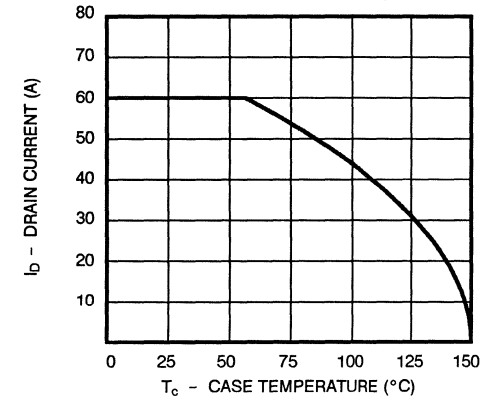
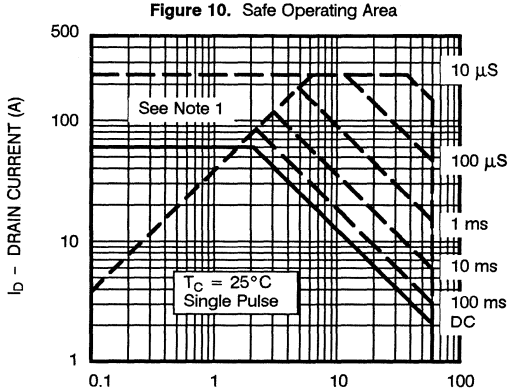
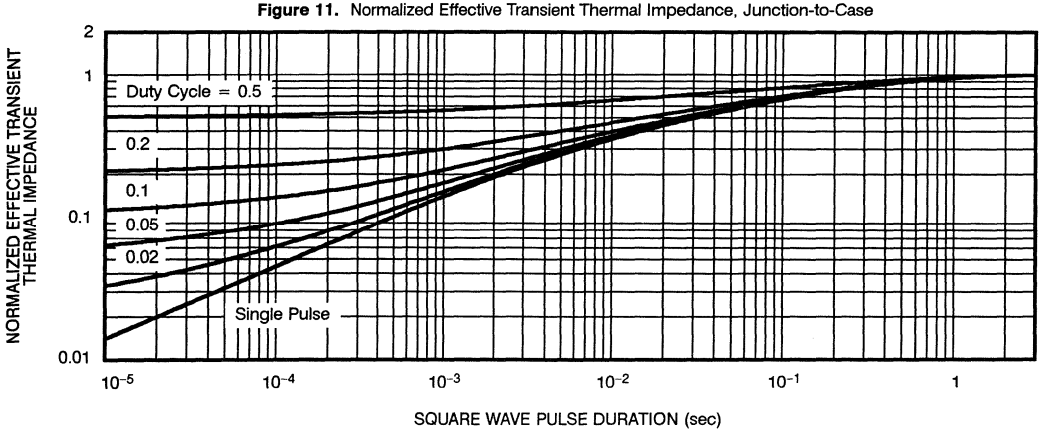


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

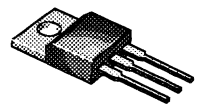
SMP60N06-18

N-Channel Enhancement Mode Transistor
18 milli ohm $r_{DS(ON)}$

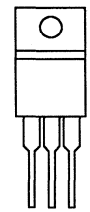
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.018	60

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		40	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.2	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.013		0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.023		0.030	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45	15		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		800			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	85		100	nC
Gate-Source Charge[2]	Q_{gs}		15		20	
Gate-Drain Charge[2]	Q_{gd}		35		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω, I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

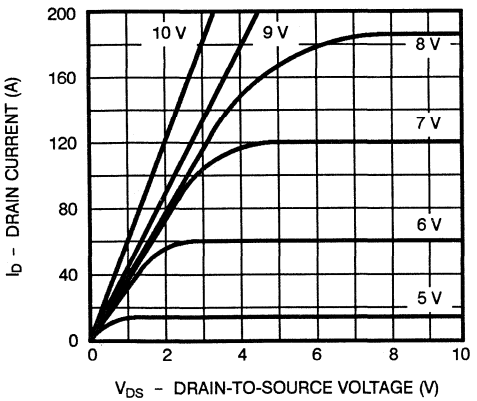


Figure 2. Transfer Characteristics

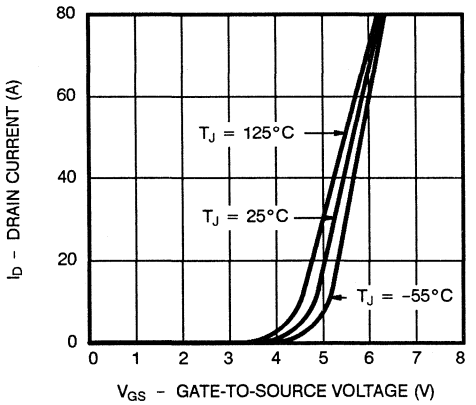


Figure 3. Transconductance

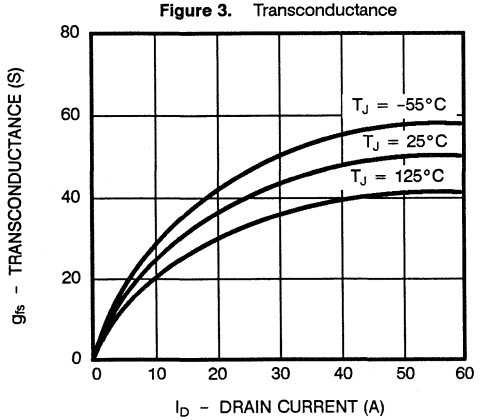


Figure 4. On-Resistance

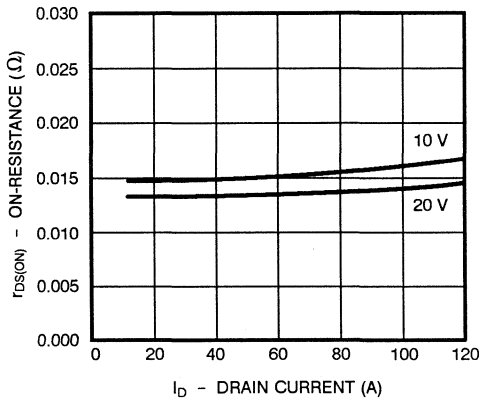


Figure 5. Capacitance

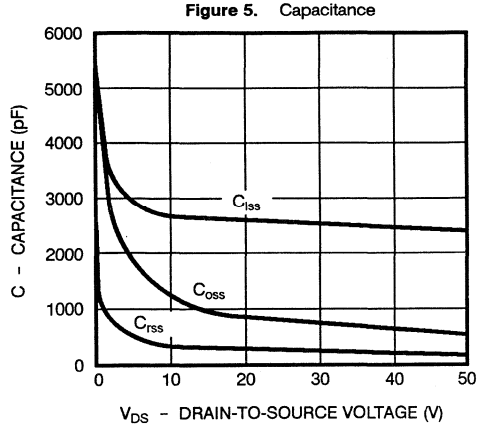
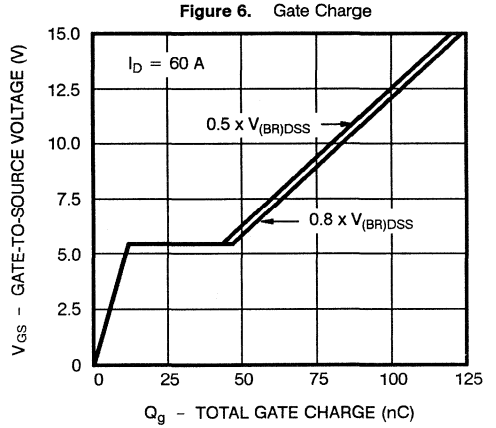


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

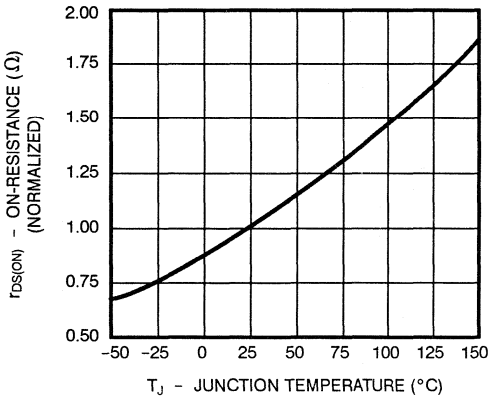
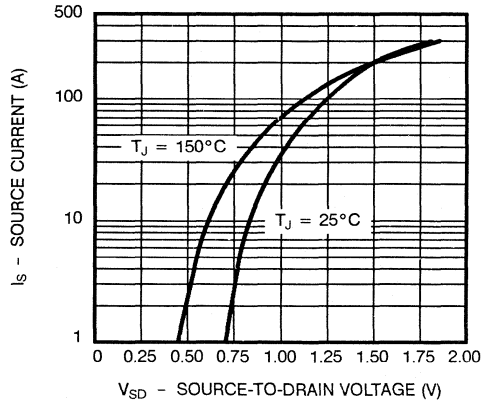


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

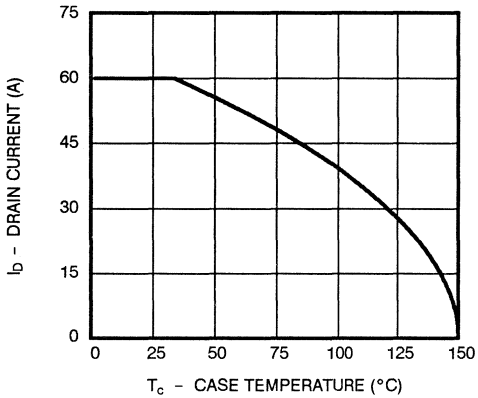
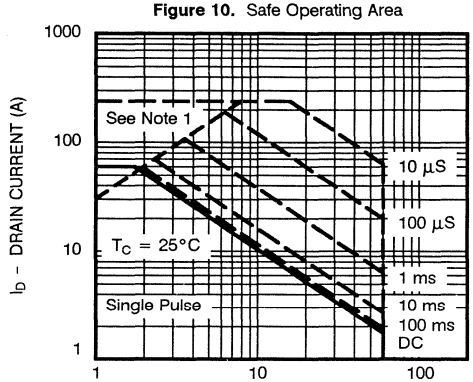
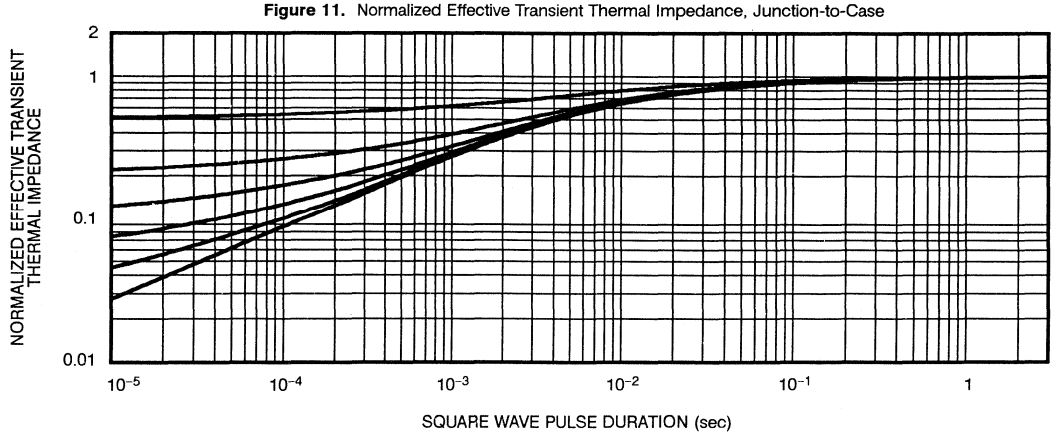


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

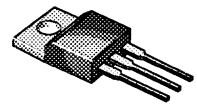


Siliconix incorporated

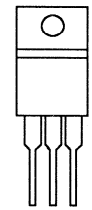
SMP60N06, SMP60N05*

N-Channel Enhancement Mode Transistors

TO-220AB



TOP VIEW



1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
SMP60N06	60	0.023	60
SMP60N05	50	0.023	60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SMP60N06	LIMITS SMP60N05	UNITS
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	60	A
	T_C = 100°C		38	38	
Pulsed Drain Current[1]		I_{DM}	240	240	
Avalanche Current (See Figure 9)		I_{AR}	60	60	
Avalanche Energy	L = 0.05 mH	E_A	90	90	mJ
Repetitive Avalanche Energy[2]	L = 0.01 mH	E_{AR}	18	18	
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11.
[2]Duty cycle ≤ 1%.

***SMP60N06 Recommended for New Designs**

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	SMP60N06 SMP60N05	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	65 65	60 50		V
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.0	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	10		±100	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]		$I_{D(ON)}$	V_{DS} = 25 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]		$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.019		0.023	Ω
			V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.025		0.030	
Forward Transconductance[1]		g_{fs}	V_{DS} = 25 V, I_D = 30 A	18	15		S
DYNAMIC							
Input Capacitance		C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2900			pF
Output Capacitance		C_{oss}		1500			
Reverse Transfer Capacitance		C_{rss}		500			
Total Gate Charge[2]		Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	70		100	nC
Gate-Source Charge[2]		Q_{gs}		22		35	
Gate-Drain Charge[2]		Q_{gd}		35		50	
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	20		40	ns
Rise Time[2]		t_r		25		50	
Turn-Off Delay Time[2]		$t_{d(off)}$		30		60	
Fall Time[2]		t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current		I_S				60	A
Pulsed Current[3]		I_{SM}				190	
Forward Voltage[1]		V_{SD}	I_F = I_S, V_{GS} = 0 V			2.4	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	75		100	ns
Reverse Recovery Charge		Q_{rr}		0.19			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

*SMP60N06 Recommended for New Designs

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

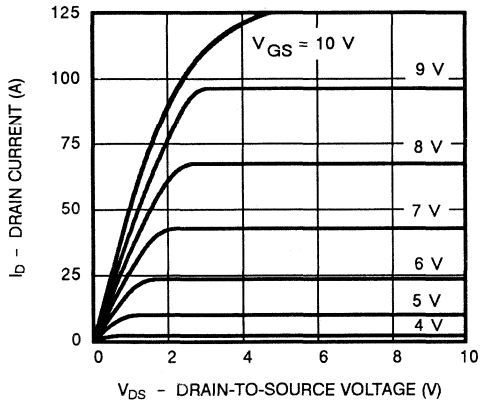


Figure 2. Transfer Characteristics

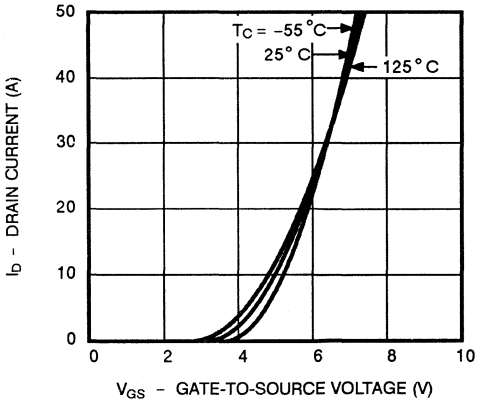


Figure 3. Transconductance

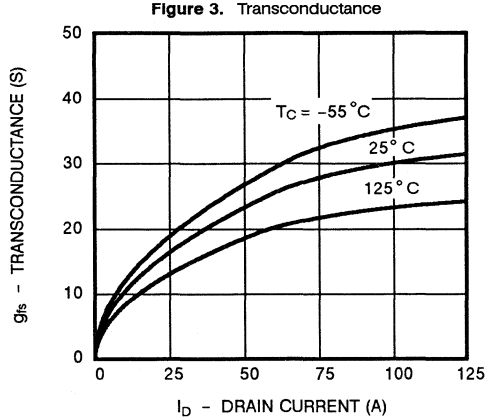


Figure 4. On-Resistance

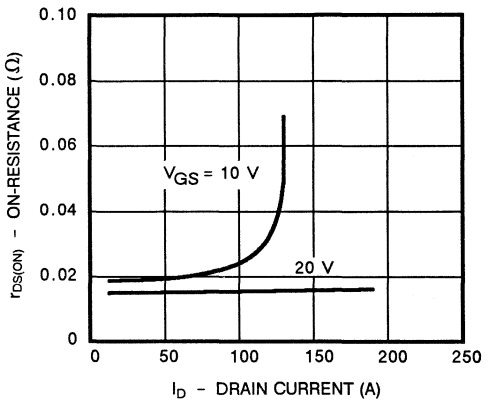


Figure 5. Capacitance

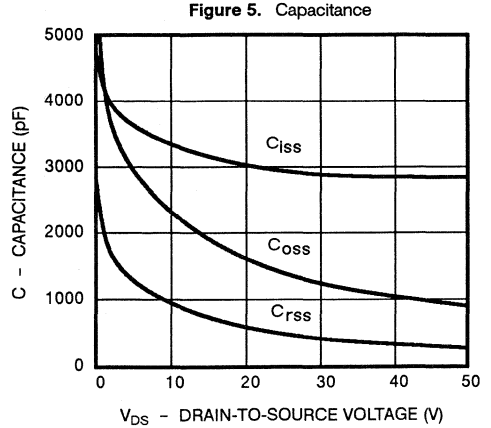
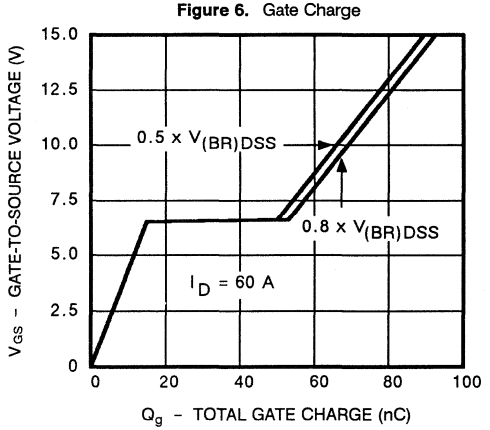


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

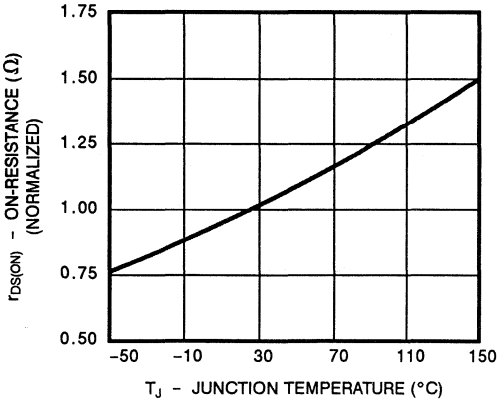
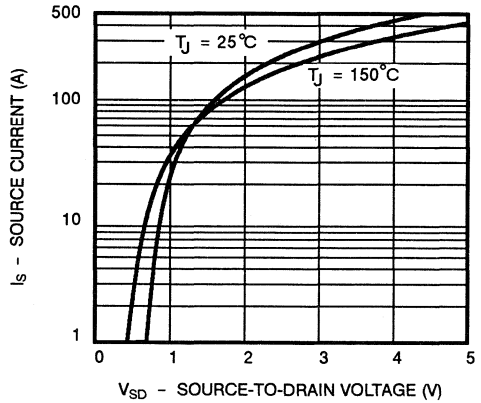


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

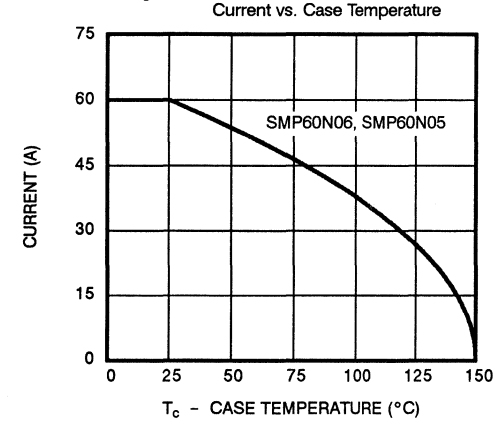
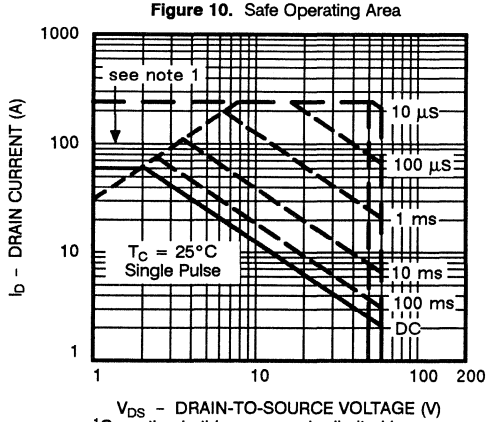
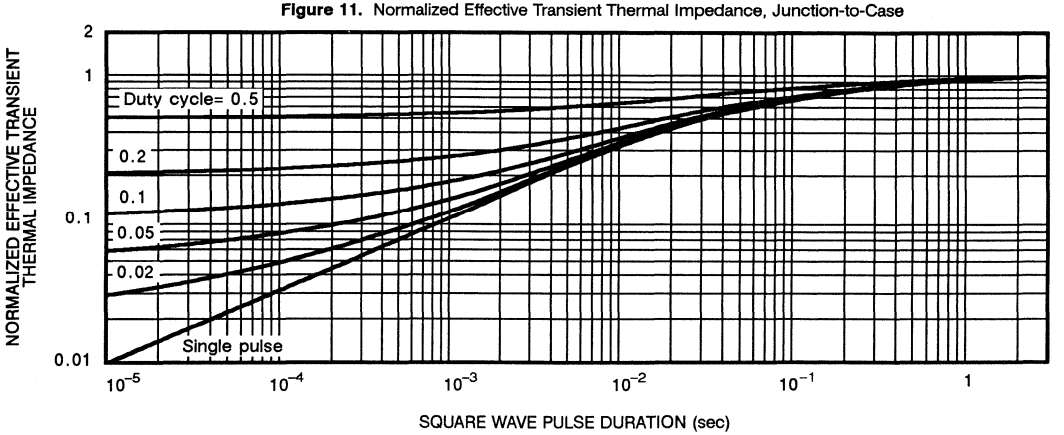


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



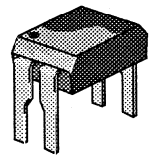
*SMP60N06 Recommended for New Designs

Siliconix incorporated

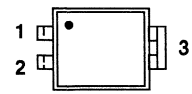
SMV1P10

P-Channel Enhancement Mode Transistor

4-PIN DIP
(Similar to TO-250)



TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
−100	1.2	−0.70

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.70	A
	T_A = 100°C		0.44	
Pulsed Drain Current[2]		I_{DM}	3.0	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	R_{thJA}		120	K/W

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		0.70		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 0.3 A	1		1.2	Ω
		V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	1.6		2.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 0.3 A	0.5	0.3		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	150		250	pF
Output Capacitance	C_{oss}		65		120	
Reverse Transfer Capacitance	C_{rss}		25		45	
Total Gate Charge[2]	Q_g	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.70 A	6		15	nC
Gate-Source Charge[2]	Q_{gs}		1			
Gate-Drain Charge[2]	Q_{gd}		3.5			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 130 Ω, $I_D \simeq$ 0.3 A, V_{GEN} = 10 V, R_G = 25 Ω	7		30	ns
Rise Time[2]	t_r		45		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		38		60	
Fall Time[2]	t_f		55		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_A = 25°C)						
Continuous Current	I_S				0.7	A
Pulsed Current[3]	I_{SM}				3.0	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			5.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	70			ns
Reverse Recovery Charge	Q_{rr}		0.20			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

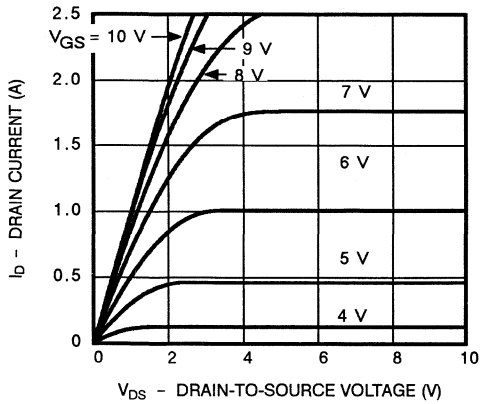


Figure 2. Transfer Characteristics

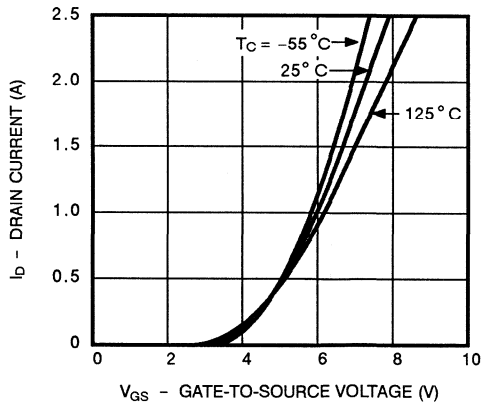


Figure 3. Transconductance

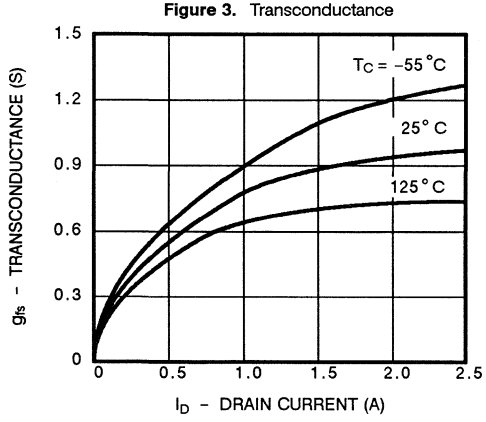


Figure 4. On-Resistance

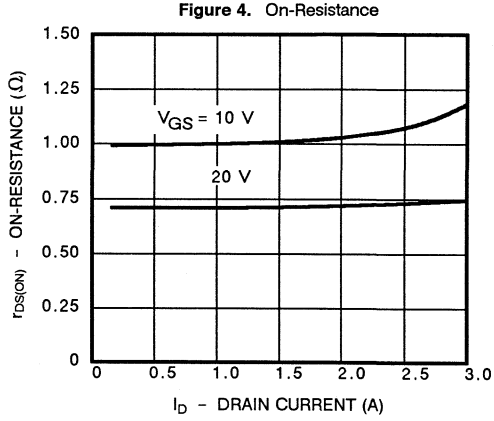


Figure 5. Capacitance

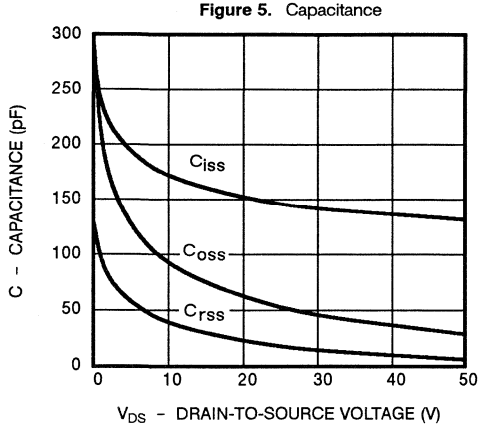
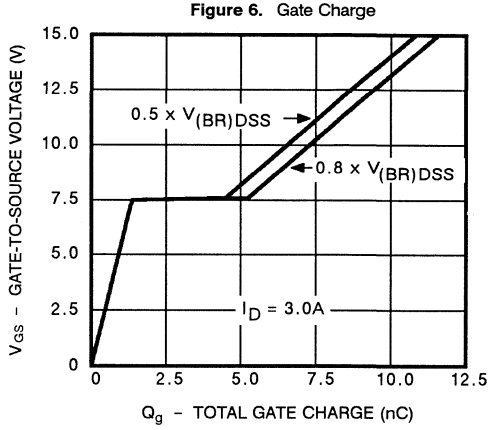


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

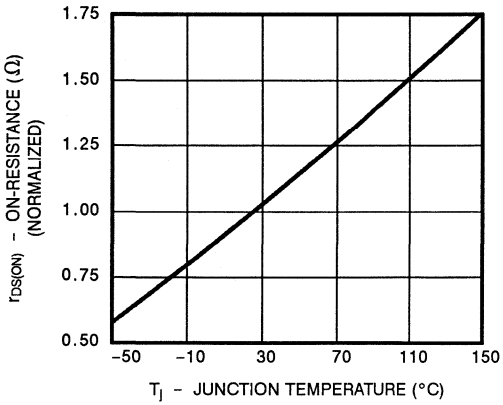
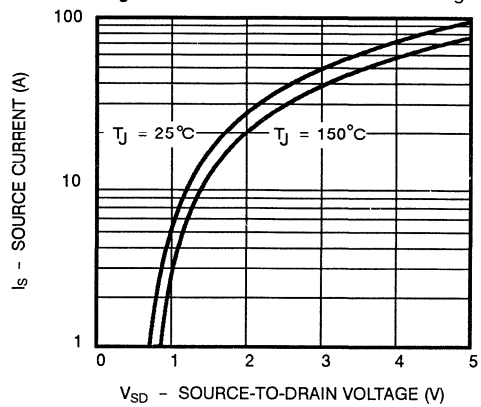


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

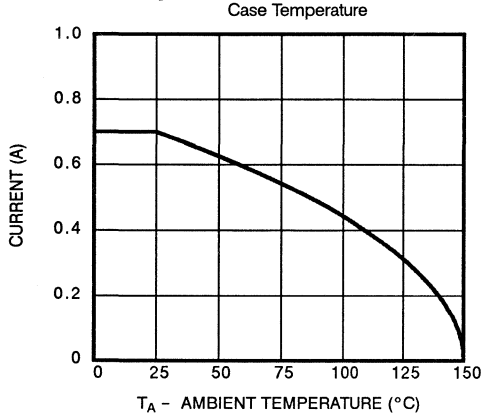
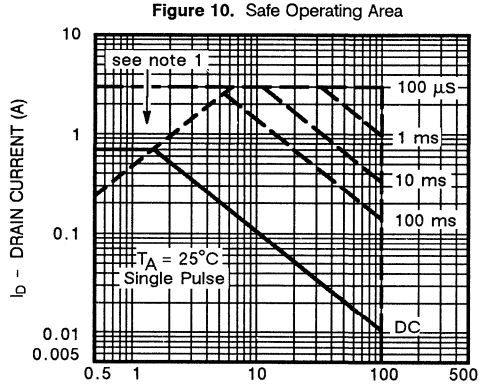


Figure 10. Safe Operating Area



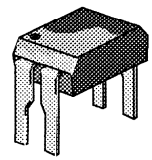
[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

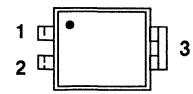
SMV1P20

P-Channel Enhancement Mode Transistor

4-PIN DIP
(Similar to TO-250)



TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	3.0	-0.40

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.40	A
	T_A = 100°C		0.25	
Pulsed Drain Current[2]		I_{DM}	1.6	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	R_{thJA}		120	K/W

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		0.40		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 0.3 A	2.2		3.0	Ω
		V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	4.0		5.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 0.3 A	0.6	0.3		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	180		300	pF
Output Capacitance	C_{oss}		70		100	
Reverse Transfer Capacitance	C_{rss}		25		35	
Total Gate Charge[2]	Q_g	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.40 A	5.0		11	nC
Gate-Source Charge[2]	Q_{gs}		0.8			
Gate-Drain Charge[2]	Q_{gd}		3			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 330 Ω, I_D ≃ 0.3 A, V_{GEN} = 10 V, R_G = 25 Ω	7.5		15	ns
Rise Time[2]	t_r		13		25	
Turn-Off Delay Time[2]	$t_{d(off)}$		45		60	
Fall Time[2]	t_f		28		45	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_A = 25°C)						
Continuous Current	I_S				0.4	A
Pulsed Current[3]	I_{SM}				1.6	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			5.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	100			ns
Reverse Recovery Charge	Q_{rr}		0.36			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

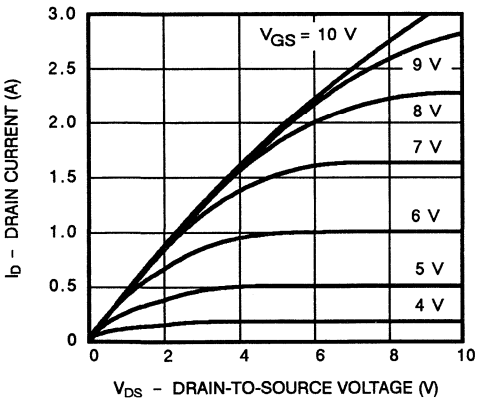


Figure 2. Transfer Characteristics

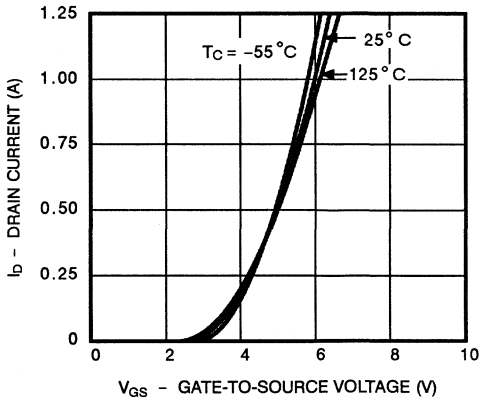


Figure 3. Transconductance

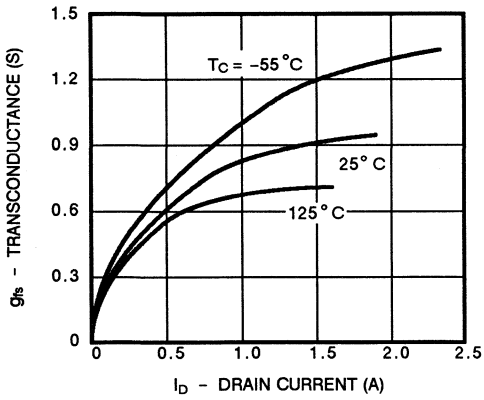


Figure 4. On-Resistance

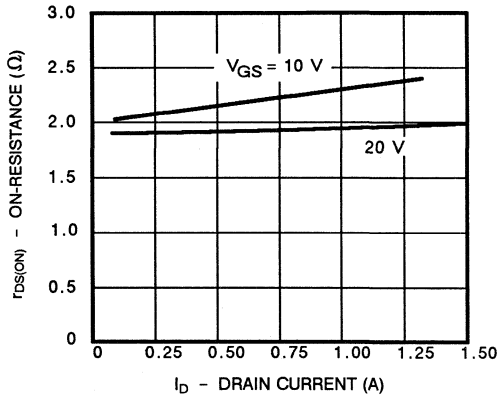


Figure 5. Capacitance

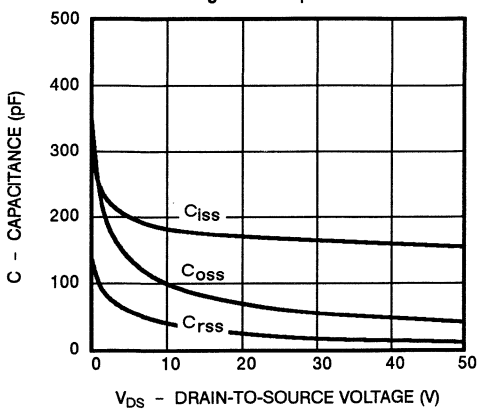
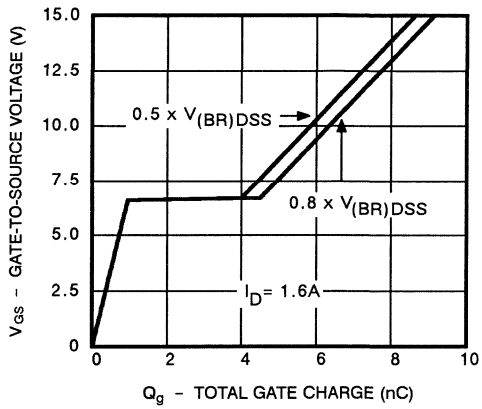


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

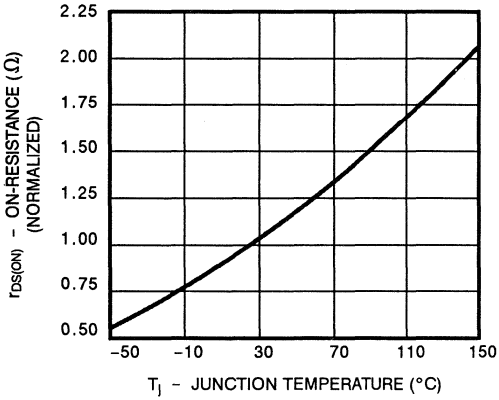
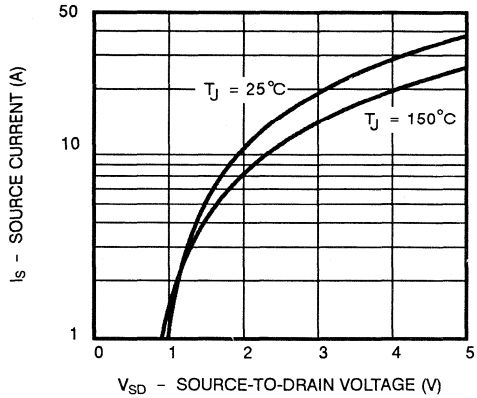


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Ambient Temperature

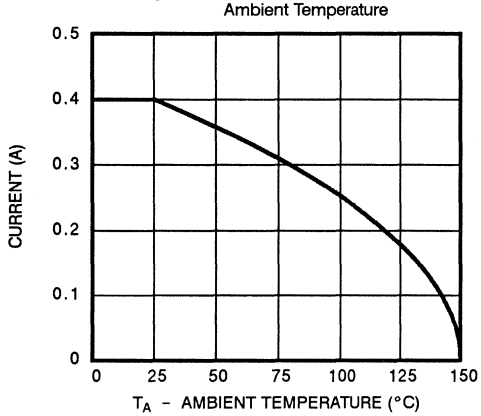
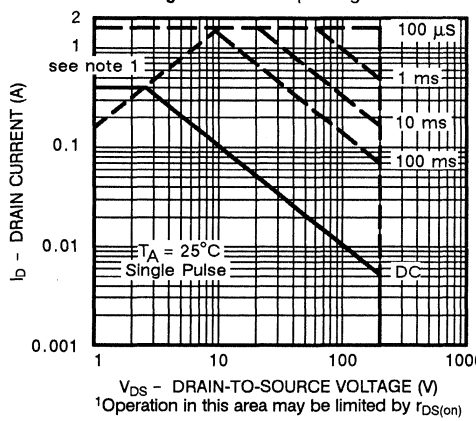


Figure 10. Safe Operating Area



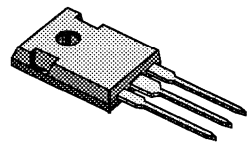
[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

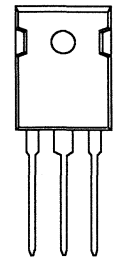
SMW12P20

P-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-12

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		7.5	
Pulsed Drain Current[2]		I_{DM}	48	
Avalanche Current (See Figure 9)		I_{AR}	12	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	7.2	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		12		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7.5 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C	0.50		0.90	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A	5	4.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A	55		90	nC
Gate-Source Charge[2]	Q_{gs}		8		15	
Gate-Drain Charge[2]	Q_{gd}		30		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 8.3 Ω, I_D ≃ 12 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		30		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		80	
Fall Time[2]	t_f		16		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				12	A
Pulsed Current[3]	I_{SM}				48	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µS	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

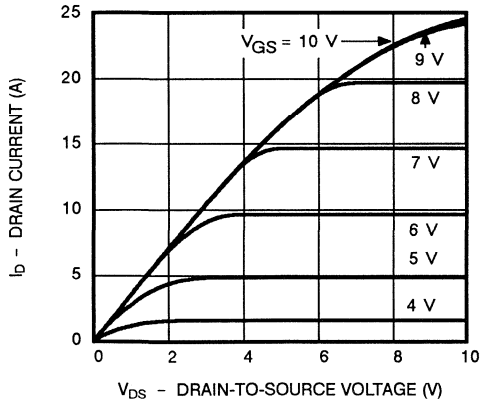


Figure 2. Transfer Characteristics

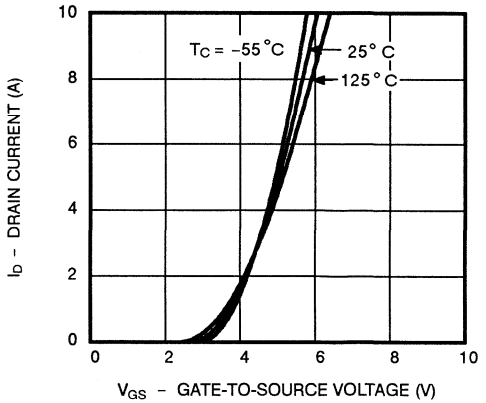


Figure 3. Transconductance

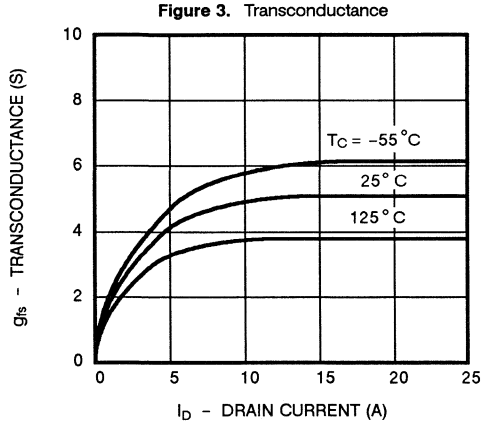


Figure 4. On-Resistance

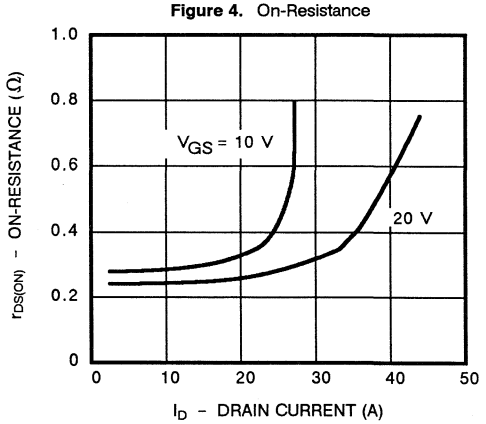


Figure 5. Capacitance

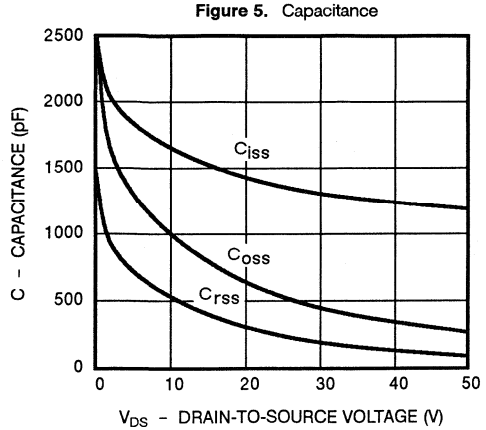
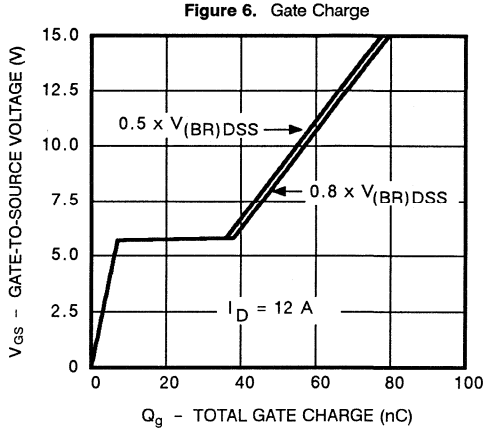


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

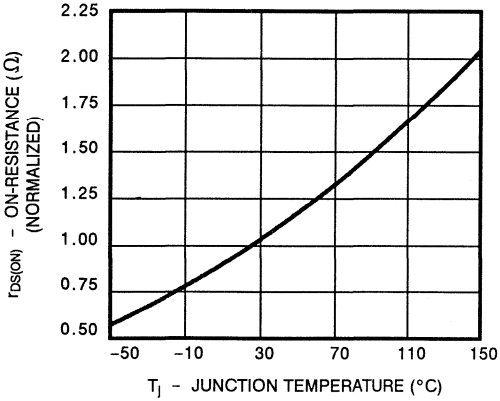
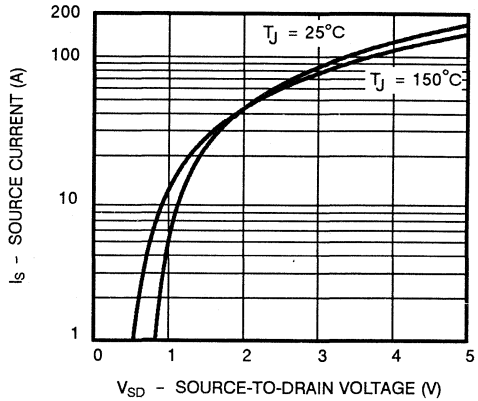


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

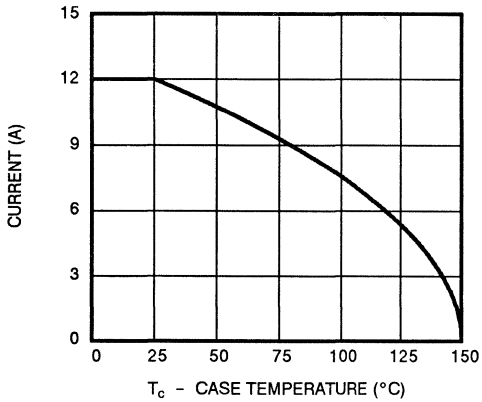
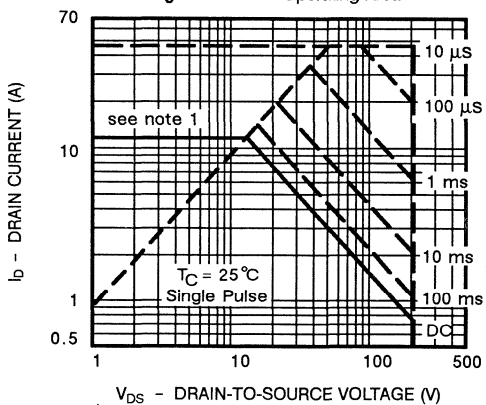
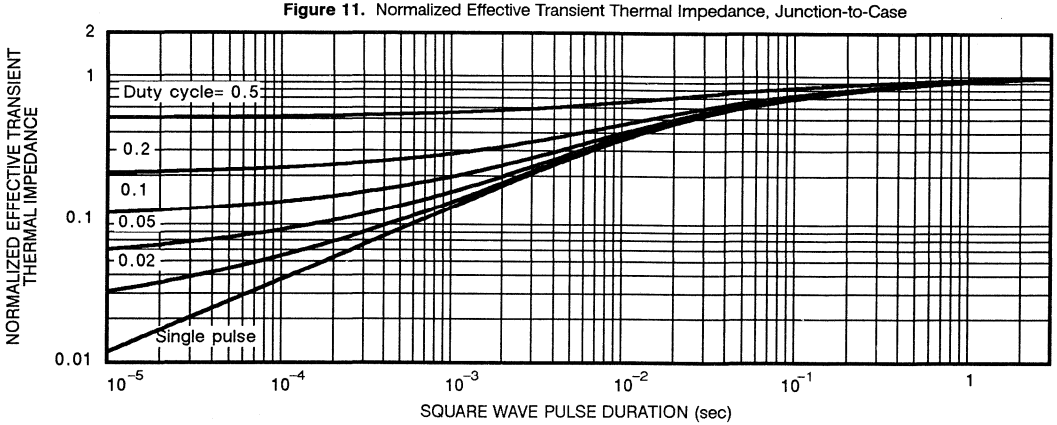


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

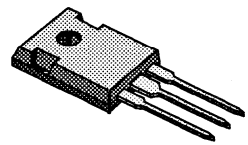


Siliconix incorporated

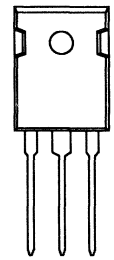
SMW14N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	0.4	14	250

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		8.8	
Pulsed Drain Current[1]		I_{DM}	56	
Avalanche Current (See Figure 9)		I_{AR}	14	
Repetitive Avalanche Energy[2]	L = 0.3 mH	E_{AR}	30	mJ
Power Dissipation	T_C = 25°C	P_D	180	W
	T_C = 100°C		75	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.70	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			14		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7 A		0.32		0.40	Ω
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C		0.70		0.88	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7 A		6.2	5		S
DYNAMIC							
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2500			pF
Output Capacitance	C_{oss}			460			
Reverse Transfer Capacitance	C_{rss}			140			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A		73		130	nC
Gate-Source Charge[2]	Q_{gs}			15		22	
Gate-Drain Charge[2]	Q_{gd}			40		64	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 17 Ω, I_D ≃ 14 A, V_{GEN} = 10 V, R_G = 4.7 Ω		16		27	ns
Rise Time[2]	t_r			44		66	
Turn-Off Delay Time[2]	$t_{d(off)}$			60		100	
Fall Time[2]	t_f			35		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					14	A
Pulsed Current[3]	I_{SM}					56	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.4	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 150 A/µs, V_{DD} = 250 V	T_J = 25°C	205		250	ns
			T_J = 125°C	275		350	
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C	13			A
			T_J = 125°C	18			
Reverse Recovery Charge	Q_{rr}		T_J = 25°C	1.4		2.2	µC
			T_J = 125°C	2.5		4.0	

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

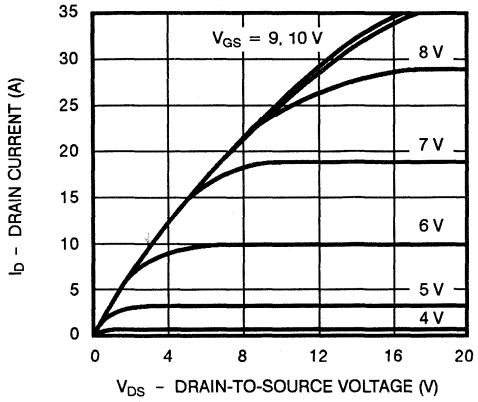


Figure 2. Transfer Characteristics

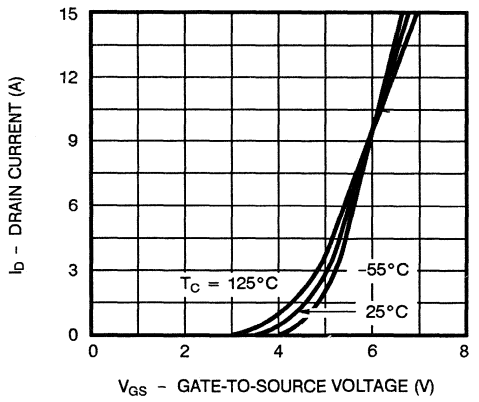


Figure 3. Transconductance

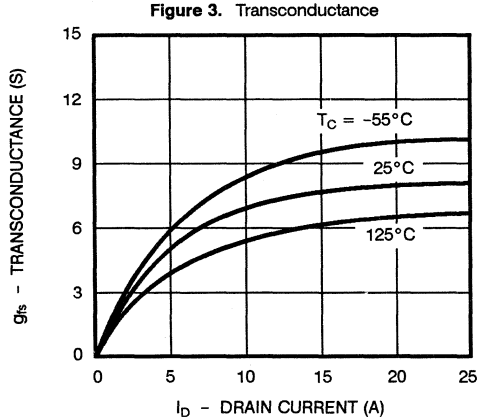


Figure 4. On-Resistance

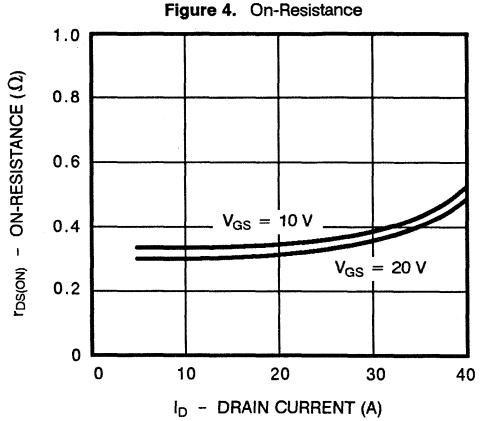


Figure 5. Capacitance

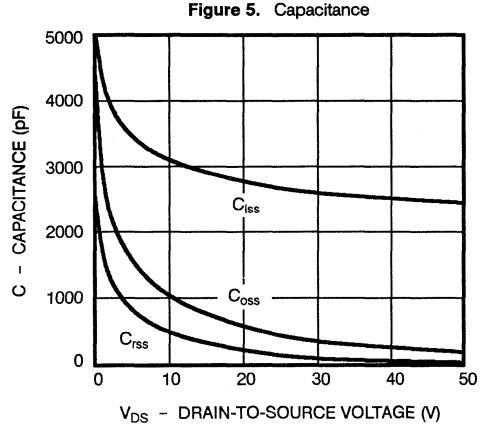
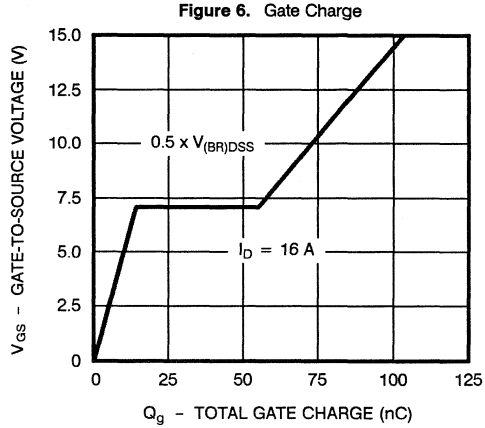


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

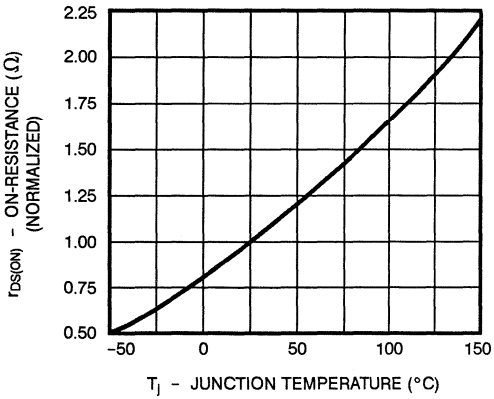
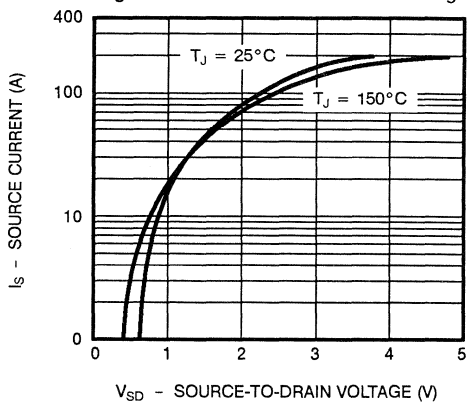


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

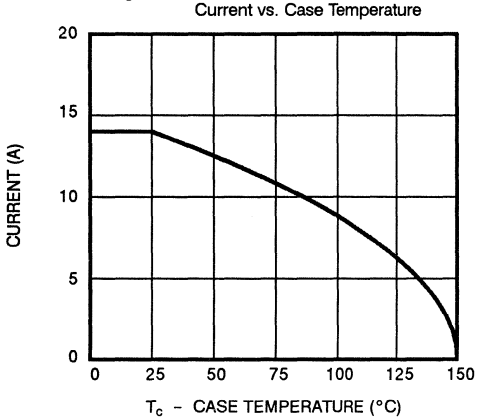
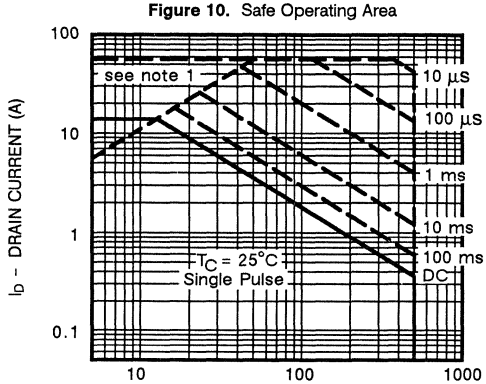
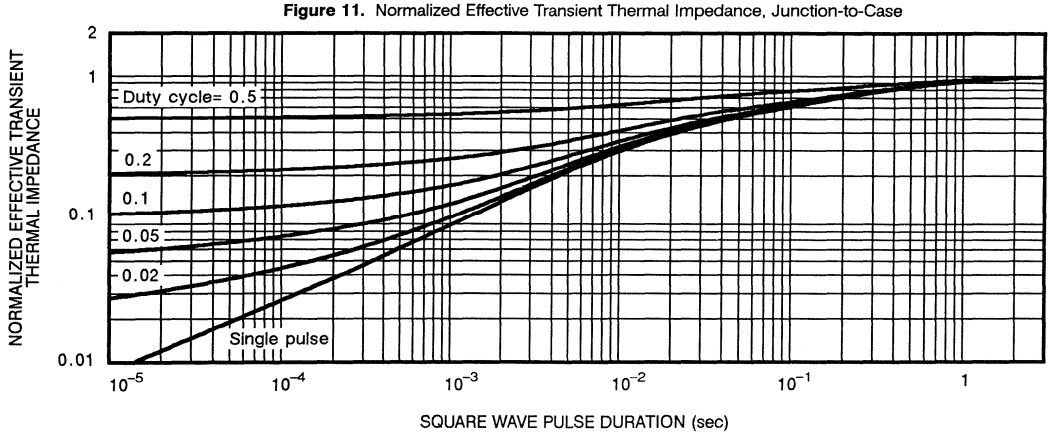


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

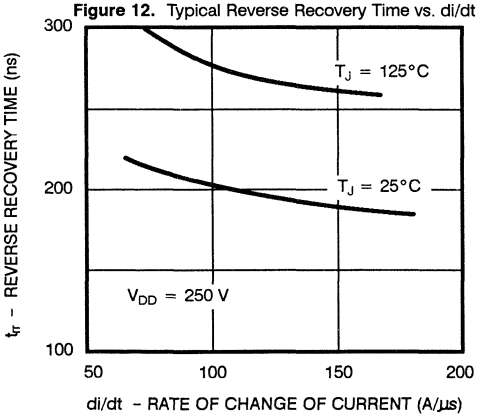


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

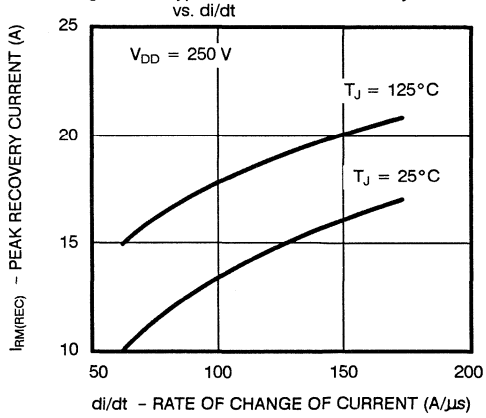


Figure 14. Commutating Safe Operating Area

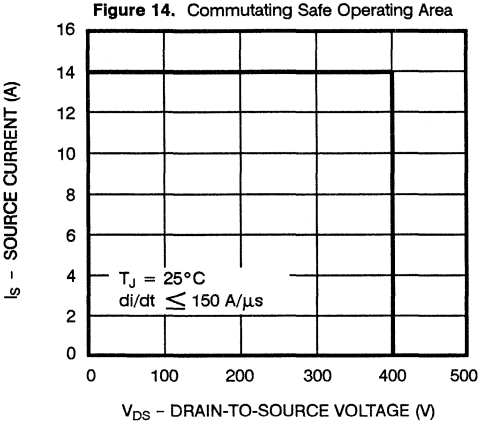


Figure 15. Typical dv/dt vs. di/dt

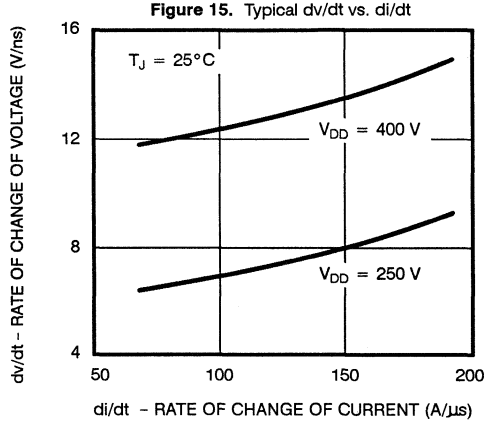
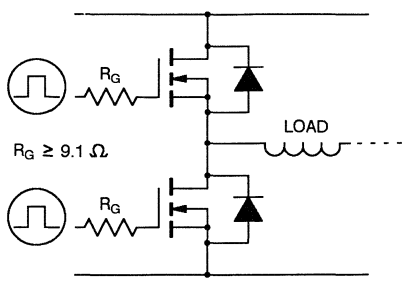
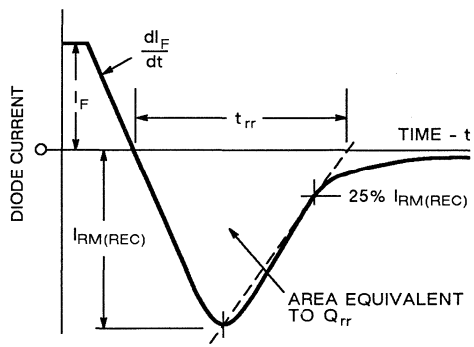


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



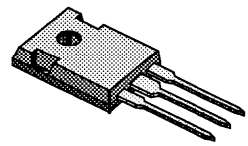
4

Siliconix incorporated

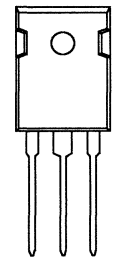
SMW20P10

P-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	0.20	-20

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		13	
Pulsed Drain Current[2]		I_{DM}	80	
Avalanche Current (See Figure 9)		I_{AR}	20	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	20	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)
P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 13 A	0.14		0.20	Ω
		V_{GS} = 10 V, I_D = 13 A, T_J = 125°C	0.22		0.32	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 13 A	6	5.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1150			pF
Output Capacitance	C_{oss}		680			
Reverse Transfer Capacitance	C_{rss}		195			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	47		62	nC
Gate-Source Charge[2]	Q_{gs}		10		15	
Gate-Drain Charge[2]	Q_{gd}		27		35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 2.5 Ω, $I_D \simeq$ 20 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		80	
Fall Time[2]	t_f		15		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				80	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

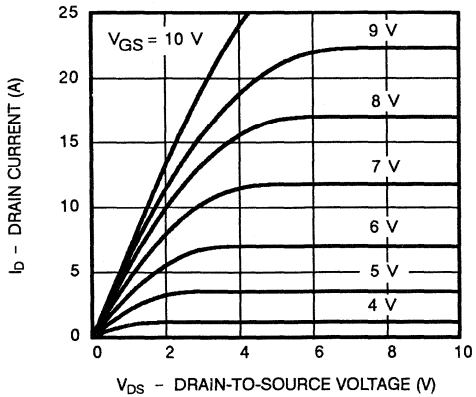


Figure 2. Transfer Characteristics

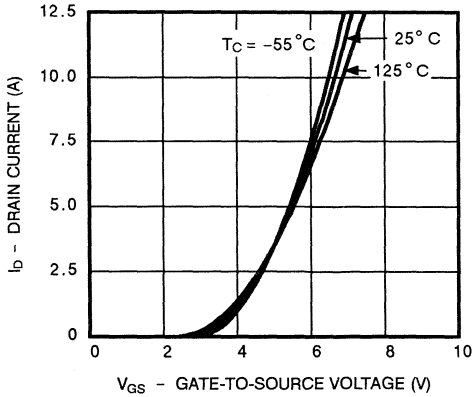


Figure 3. Transconductance

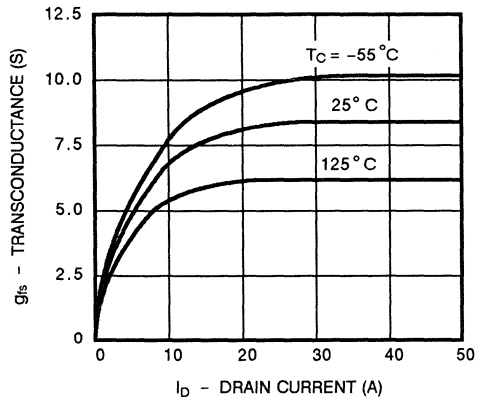


Figure 4. On-Resistance

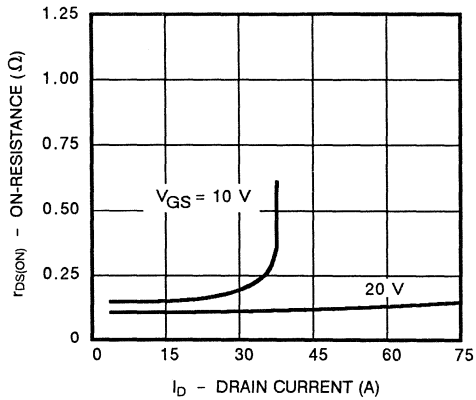


Figure 5. Capacitance

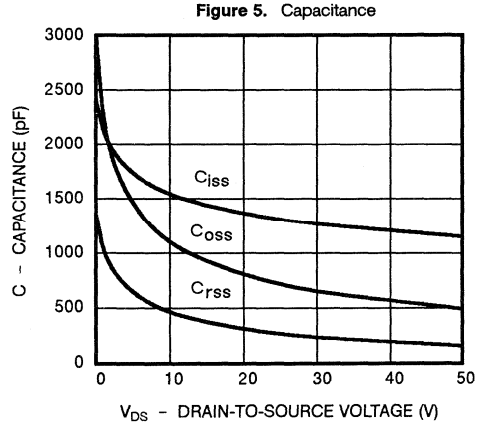
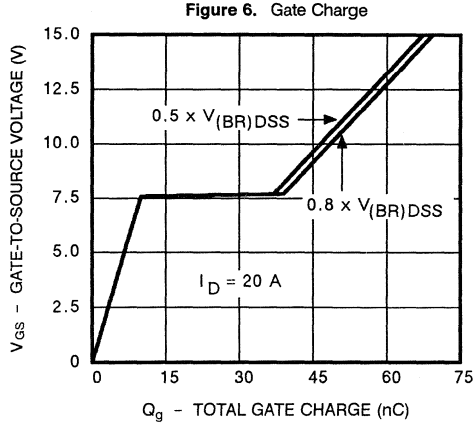


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

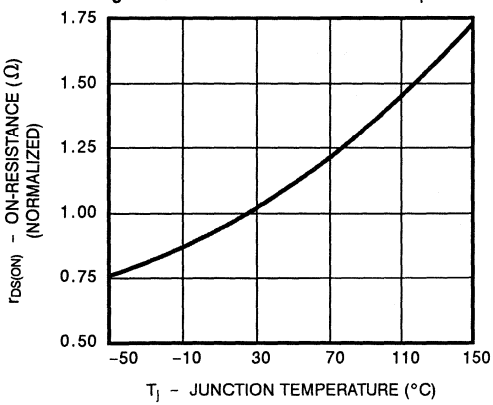
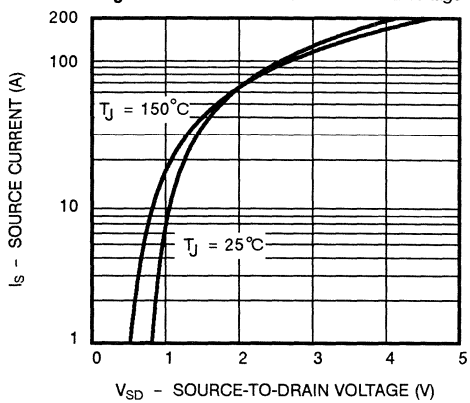


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

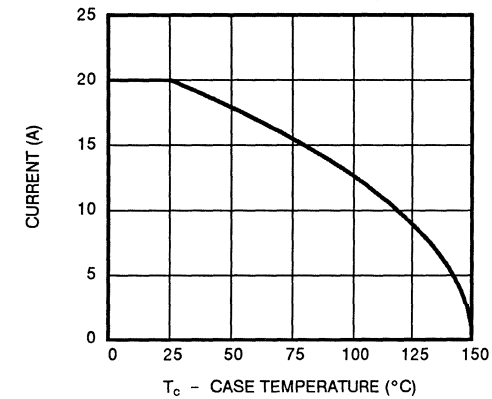
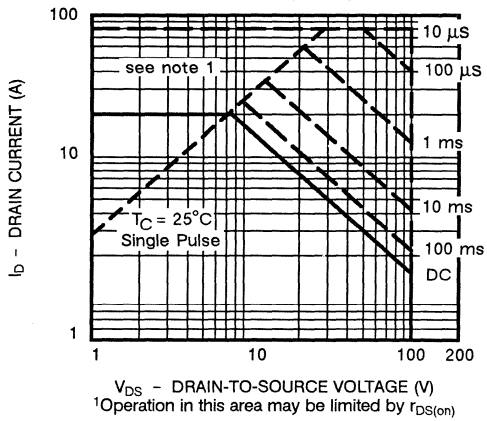
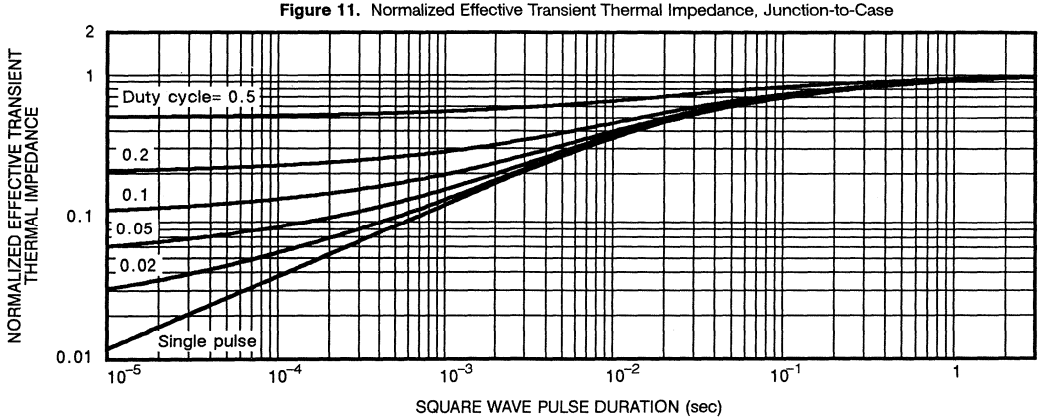


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

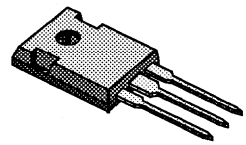


Siliconix incorporated

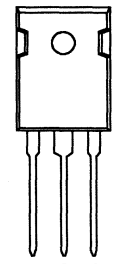
SMW45N10

N-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.040	45

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	45	A
	T_C = 100°C		27	
Pulsed Drain Current[1]		I_{DM}	180	
Avalanche Current (See Figure 9)		I_{AR}	45	
Avalanche Energy	L = 0.3 mH	E_A	300	mJ
Repetitive Avalanche Energy[2]	L = 0.02 mH	E_{AR}	20	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%, T_C = 25°C.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		45		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 27 A	0.030		0.040	Ω
		V_{GS} = 10 V, I_D = 27 A, T_J = 125°C	0.058		0.072	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 27 A		15		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3000			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		150			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 45 A	72		100	nC
Gate-Source Charge[2]	Q_{gs}		26		35	
Gate-Drain Charge[2]	Q_{gd}		31		40	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.1 Ω, $I_D \simeq$ 45 A, V_{GEN} = 10 V, R_G = 2.5 Ω	17		30	ns
Rise Time[2]	t_r		80		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				45	A
Pulsed Current[3]	I_{SM}				180	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130			ns
Reverse Recovery Charge	Q_{rr}		0.31			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

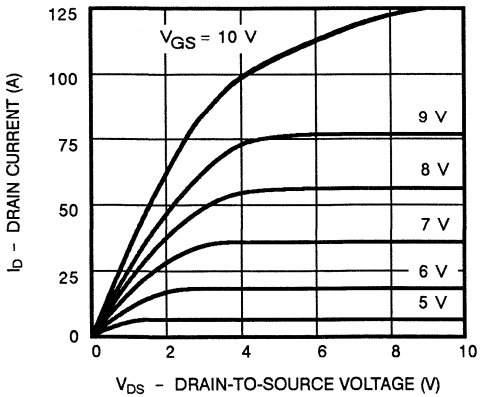


Figure 2. Transfer Characteristics

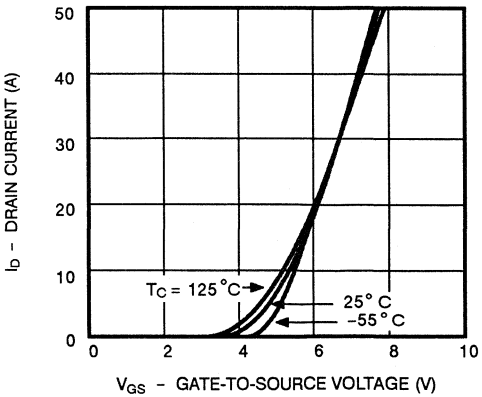


Figure 3. Transconductance

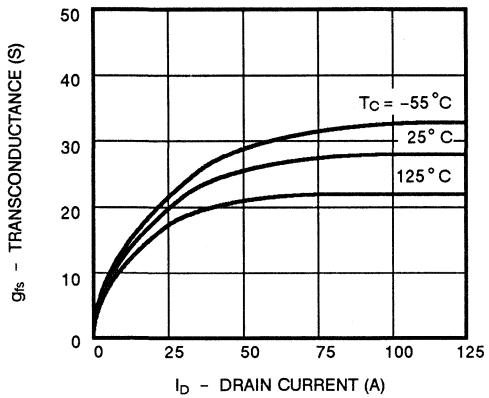


Figure 4. On-Resistance

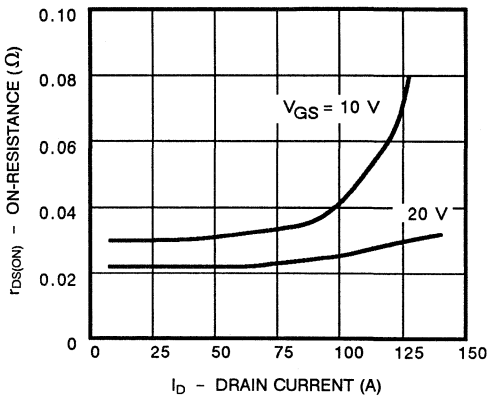


Figure 5. Capacitance

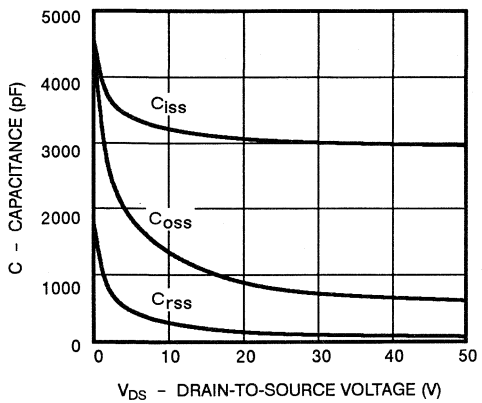
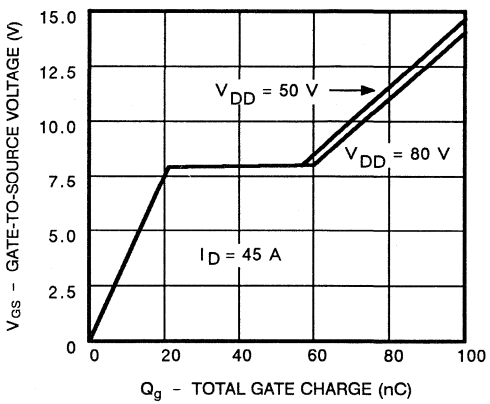


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

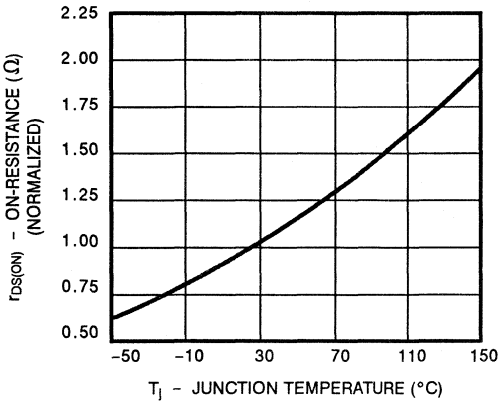
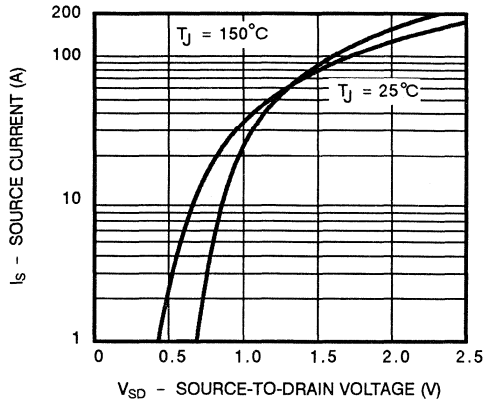


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

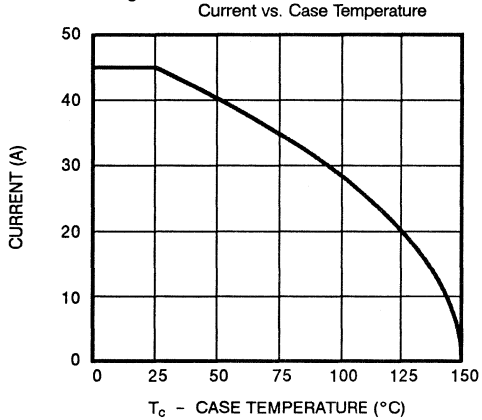


Figure 10. Safe Operating Area

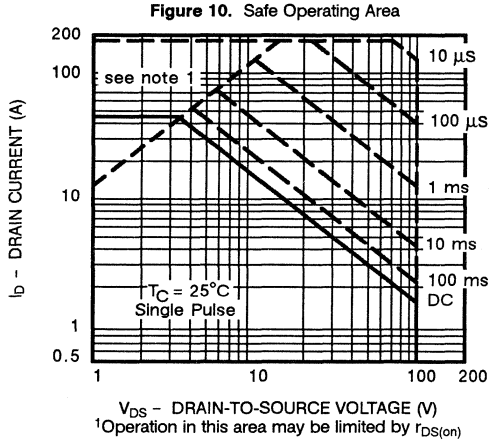
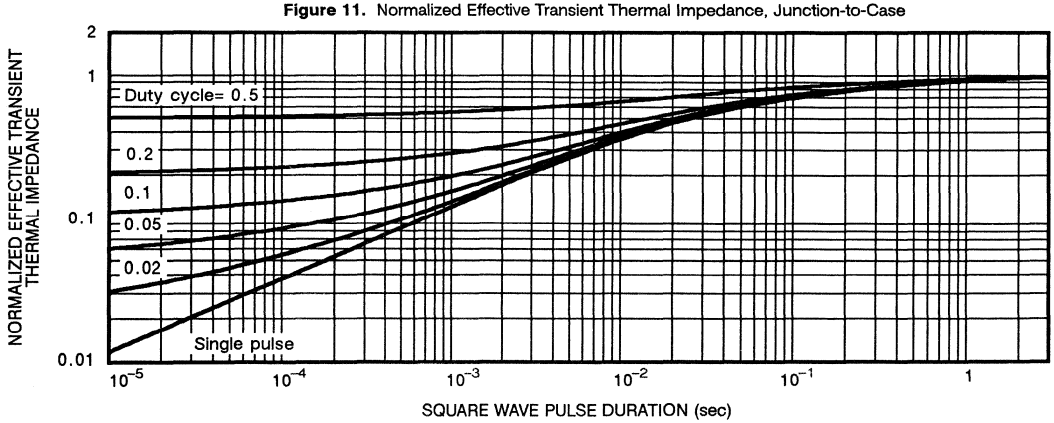


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

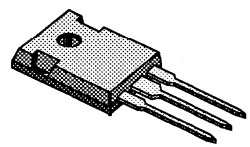


Siliconix incorporated

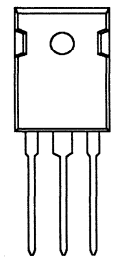
SMW60N06-18

N-Channel Enhancement Mode Transistor
18 milli ohm $r_{DS(ON)}$

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.018	60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		40	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.013		0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.023		0.030	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45	15		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		800			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	85		100	nC
Gate-Source Charge[2]	Q_{gs}		15		20	
Gate-Drain Charge[2]	Q_{gd}		35		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω, $I_D \simeq$ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

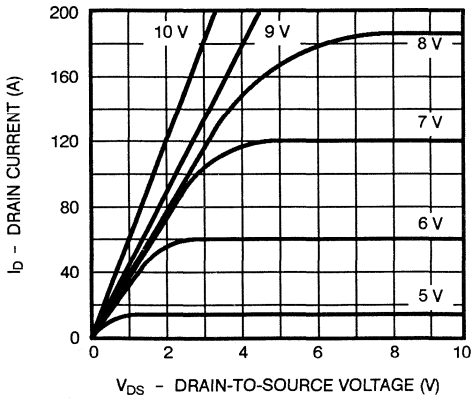


Figure 2. Transfer Characteristics

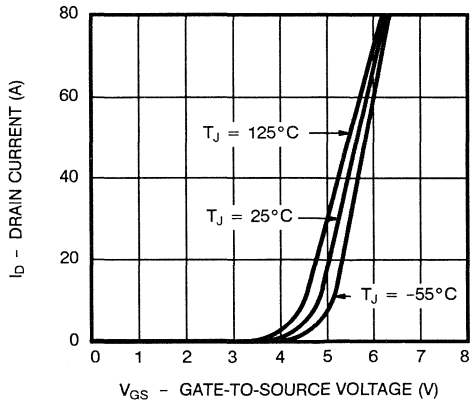


Figure 3. Transconductance

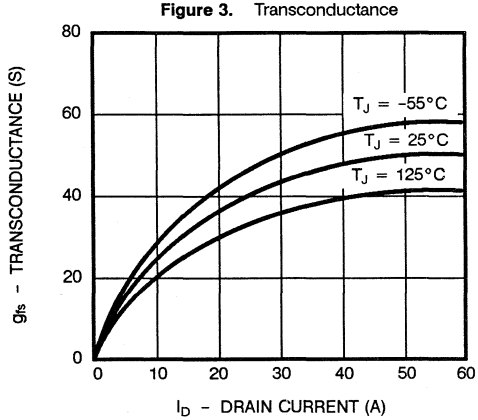


Figure 4. On-Resistance

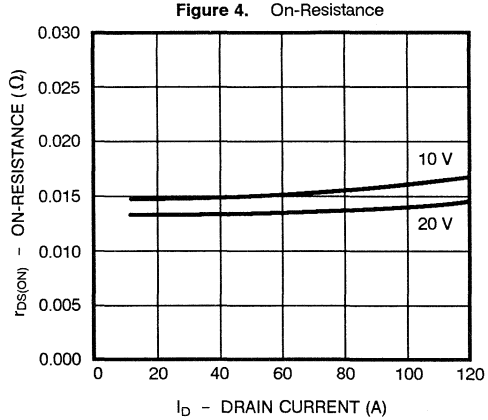


Figure 5. Capacitance

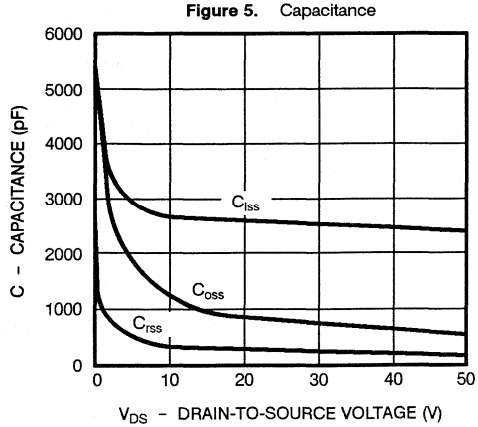
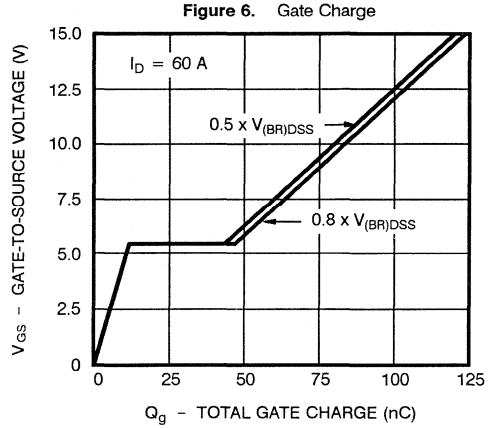


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

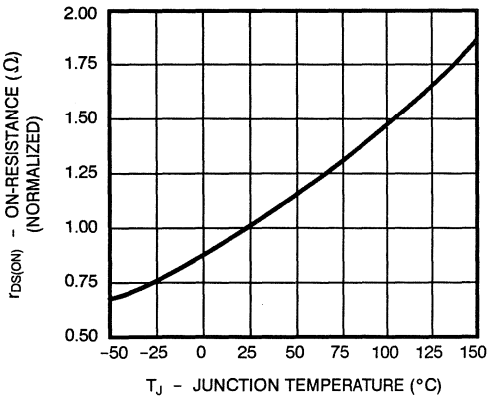
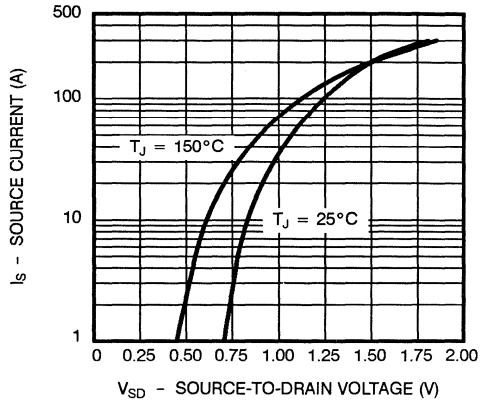


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

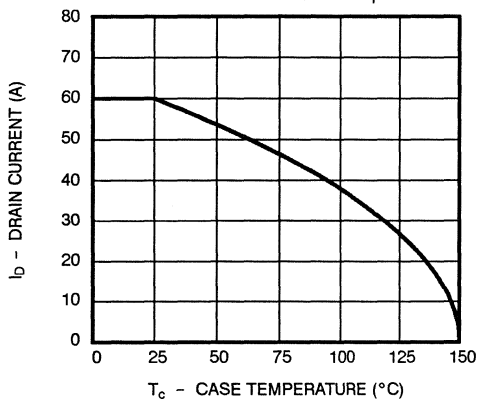
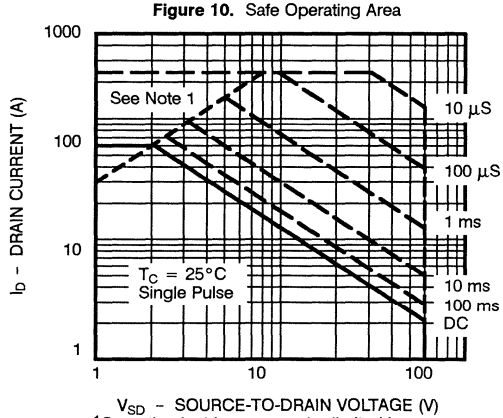
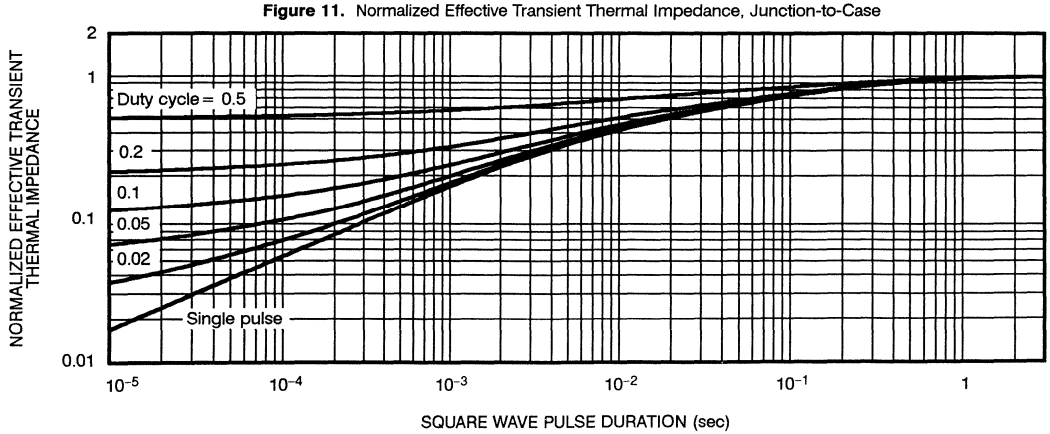


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

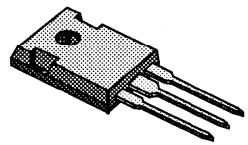


Siliconix incorporated

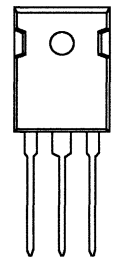
SMW60N10

N-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.025	60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		37	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current (See Figure 9)		I_{AR}	60	
Avalanche Energy	L = 0.3 mH	E_A	540	mJ
Repetitive Avalanche Energy[2]	L = 0.02 mH	E_{AR}	36	
Power Dissipation	T_C = 25°C	P_D	180	W
	T_C = 100°C		70	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.7	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .
[2]Duty cycle ≤ 1%, T_C = 25°C.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 37 A	0.020		0.025	Ω
		V_{GS} = 10 V, I_D = 37 A, T_J = 125°C	0.034		0.045	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 37 A		20		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	4100			pF
Output Capacitance	C_{oss}		1200			
Reverse Transfer Capacitance	C_{rss}		310			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	110		140	nC
Gate-Source Charge[2]	Q_{gs}		30		40	
Gate-Drain Charge[2]	Q_{gd}		52		80	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 0.83 Ω, $I_D \simeq$ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω	20		40	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	125			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

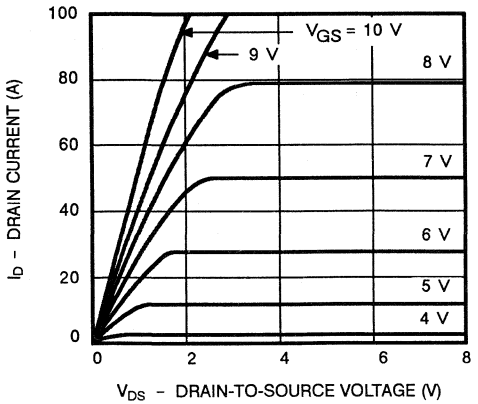


Figure 2. Transfer Characteristics

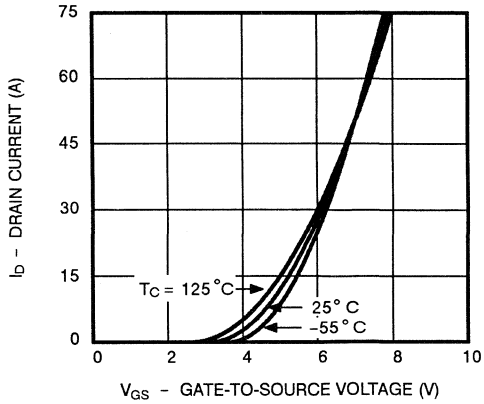


Figure 3. Transconductance

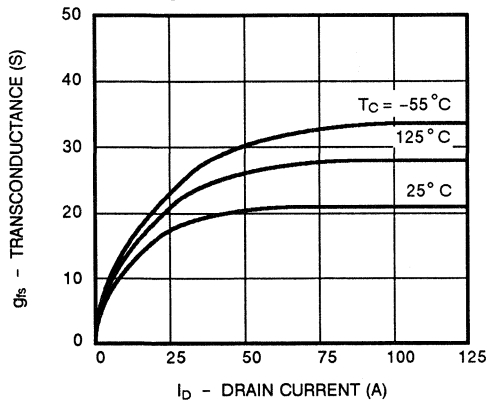


Figure 4. On-Resistance

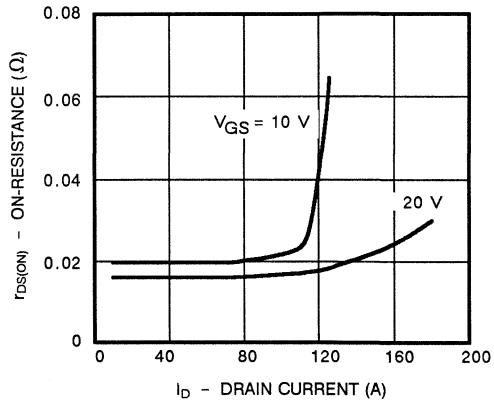


Figure 5. Capacitance

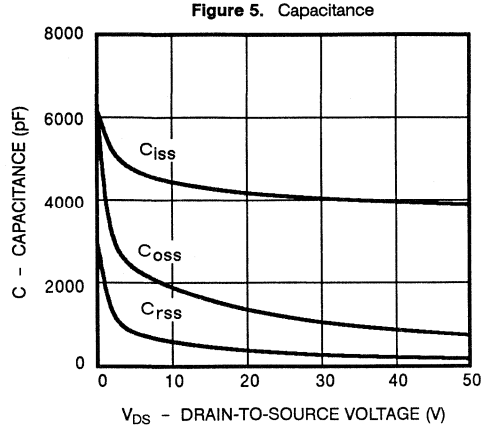
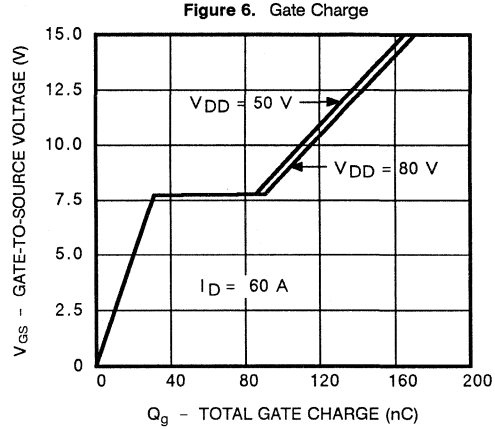


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

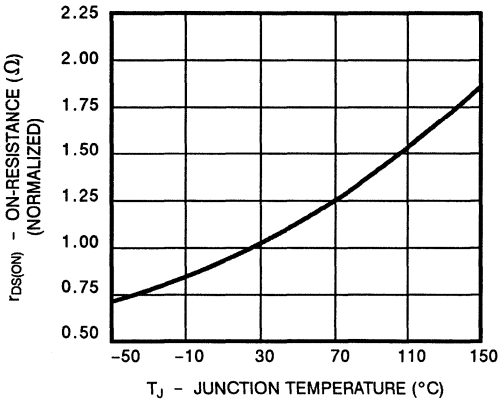
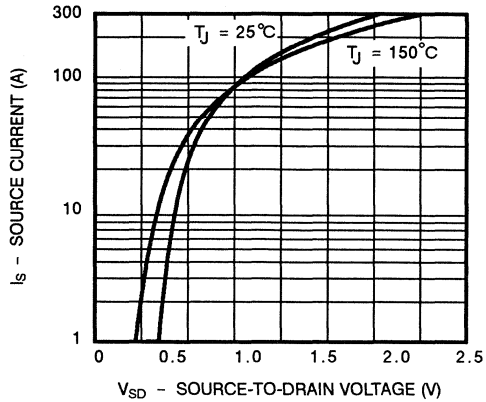


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

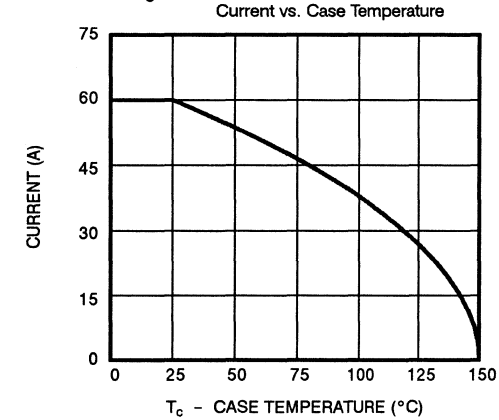
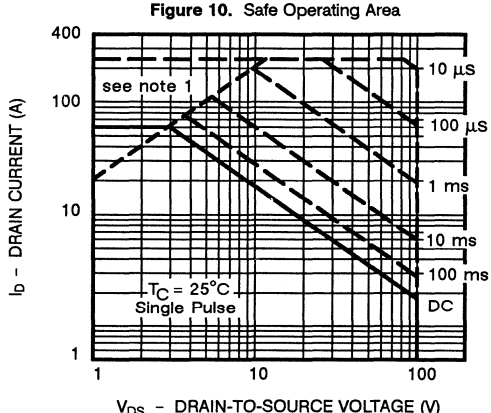
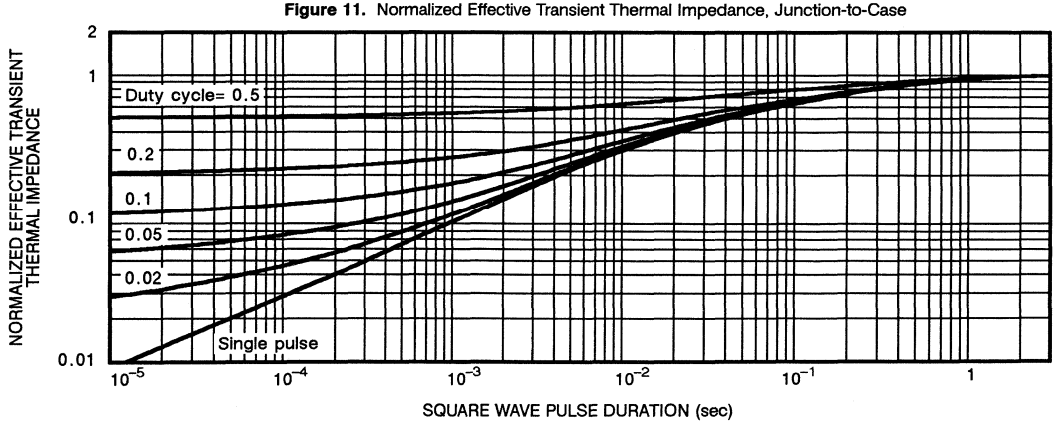


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

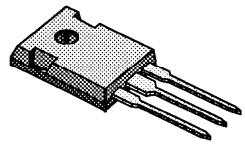


Siliconix incorporated

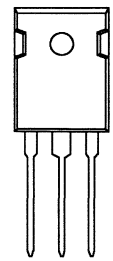
SMW70N06-14

N-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN (Conneccted to TAB)
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.014	70[1]

SiMOS 2.5 $R_{DS(ON)}$

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	70[1]	A
	T_C = 100°C		48	
Pulsed Drain Current[2]		I_{DM}	280	
Avalanche Current[3]		I_{AR}	70	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	245	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Package limited.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3.0	2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		80		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 35 A	0.012		0.014	Ω
		V_{GS} = 10 V, I_D = 35 A, T_J = 125°C	0.020		0.023	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 35 A	50	30		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3450			pF
Output Capacitance	C_{oss}		1000			
Reverse Transfer Capacitance	C_{rss}		230			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 70 A	95		130	nC
Gate-Source Charge[2]	Q_{gs}		22			
Gate-Drain Charge[2]	Q_{gd}		44			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.39 Ω, $I_D \simeq$ 70 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		100	
Fall Time[2]	t_f		20		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				70	A
Pulsed Current[3]	I_{SM}				280	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130		200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		9			A
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

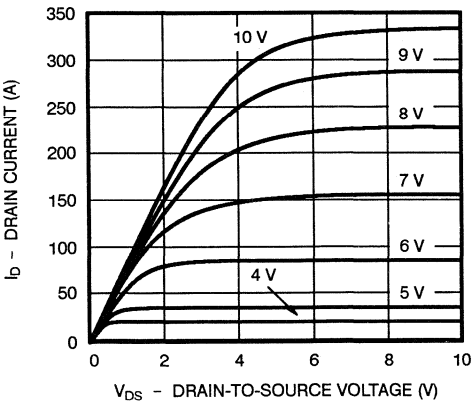


Figure 2. Transfer Characteristics

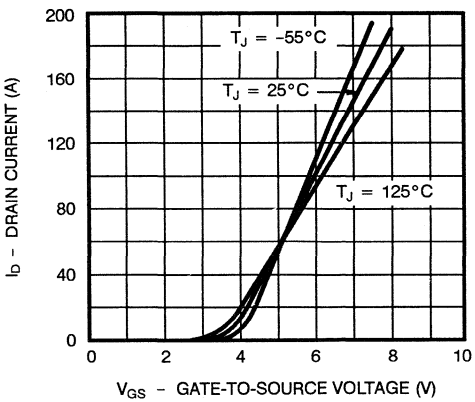


Figure 3. Transconductance

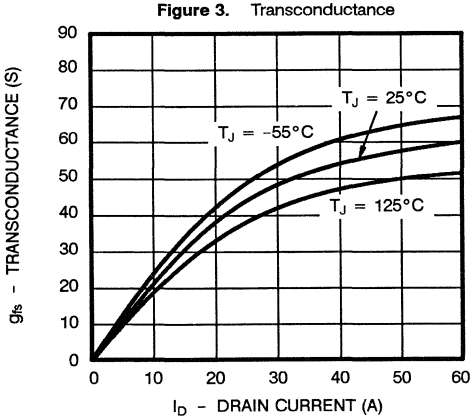


Figure 4. On-Resistance

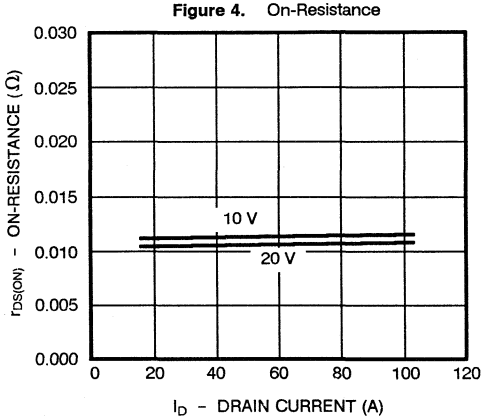


Figure 5. Capacitance

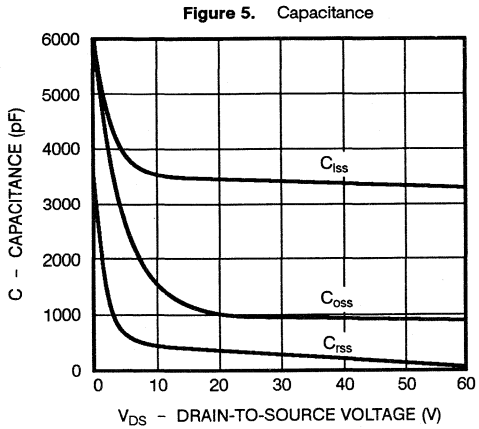
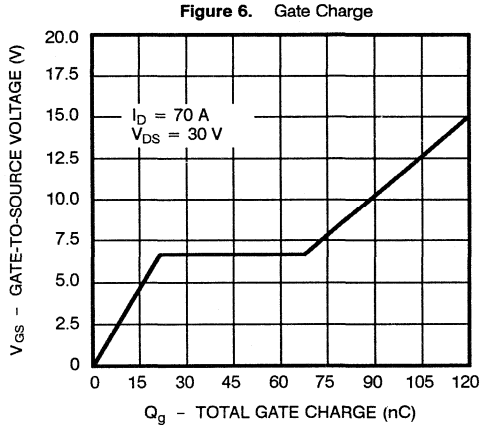


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

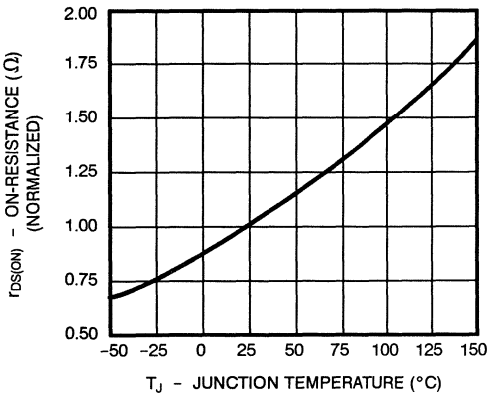
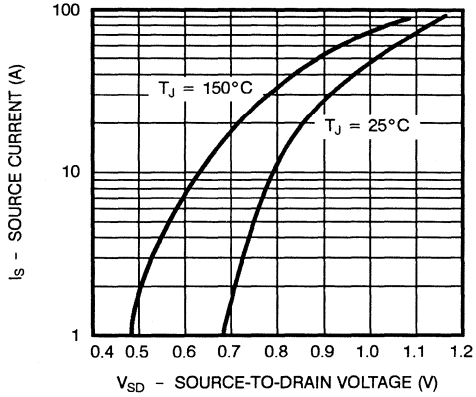


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

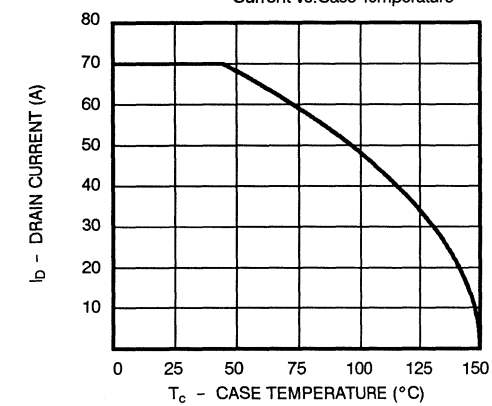
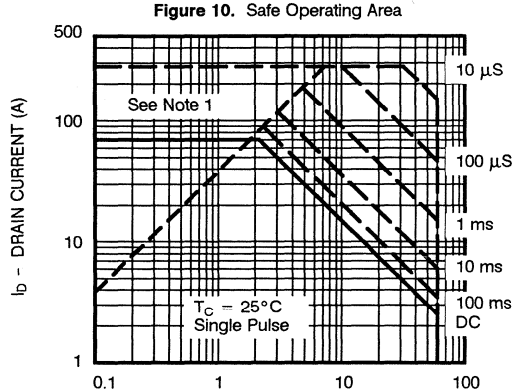
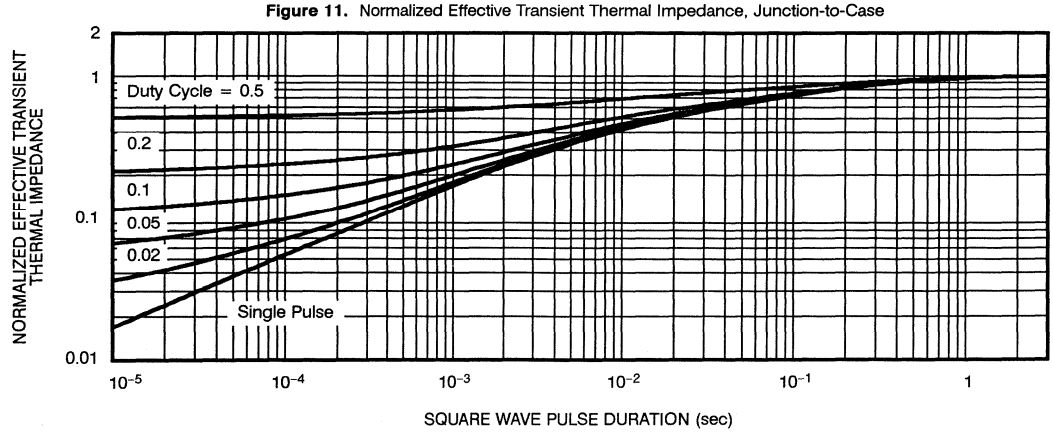


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

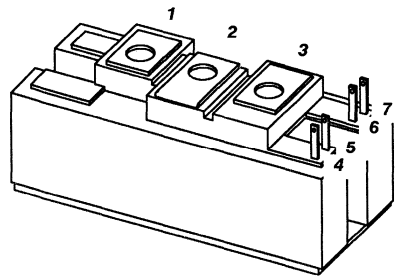
Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

SPMB50A500

Power MOSFET Module



PRODUCT SUMMARY

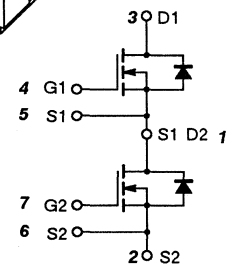
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	V_{ISOL} (V)
500	0.100	50	2500

FEATURES:

- Half-bridge Circuit
- Fast Intrinsic Diode (270 ns)
- Short Circuit Withstand Time Rated
- Isolated Plastic Package
- Very Low On-Resistance
- High Frequency Operation (>20 kHz)

APPLICATIONS:

- Uninterruptible Power Supply
- Switch-mode Power
- Motor Control
- Arc Welding Inverters
- Induction Heating



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±20	
Operating Drain Current[1]	I_D	50	A
Pulsed Drain Current[2]	I_{DM}	200	
Total Power Dissipation (per Transistor)	P_D	300	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-40 to 125	
Isolation Voltage (RMS)	V_{ISO}	2500	V
Short Circuit Withstand Time (V_{DD} = 350 V, V_{GS} = 10 V)	SCWT	12	µS

MECHANICAL DATA

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Mounting Torque (Maximum)	Mounting Base (M6)		50 (43 in-lbs)	kgf.cm
	Terminals (M5)		50 (43 in-lbs)	
Mass			220	g
Thermal Resistance (Junction to Baseplate per MOSFET)		R_{thJC}	0.41	°C/W

[1]For duty cycles ≤ 60%.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 mA		1.5	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			1.0	mA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			4.0	
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 15 V, I_D = 25 A	0.08		0.10	Ω
		V_{GS} = 15 V, I_D = 25 A, T_J = 125°C	0.15		0.22	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 25 A	20			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	11000			pF
Output Capacitance	C_{oss}		1600			
Reverse Transfer Capacitance	C_{rss}		800			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 15 V, I_D = 50 A	400		600	nC
Gate-Source Charge[2]	Q_{gs}		40		64	
Gate-Drain Charge[2]	Q_{gd}		160		320	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{GS} = 15 V, R_L = 12 Ω $I_D \simeq$ 25 A, V_{DD} = 300 V, R_G = 10 Ω	70			ns
Rise Time[2]	t_r		100			
Turn-Off Delay Time[2]	$t_{d(off)}$		950			
Fall Time[2]	t_f		250			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				50	A
Pulsed Current[3]	I_{SM}				200	
Source-Drain Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 200 A/µs, I_F = 25 A, V_R = 100 V	270		300	ns

Siliconix modules utilize the intrinsic Drain-Source diodes of the MOSPOWER chips as anti-parallel diodes. Through proprietary technology these diodes are processed for fast recovery and low V_{SD}. This means that the current handling capability of Siliconix modules is symmetrical, that is, the diode portion can handle the same peak and average current as the transistor and has the same low thermal impedance.

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

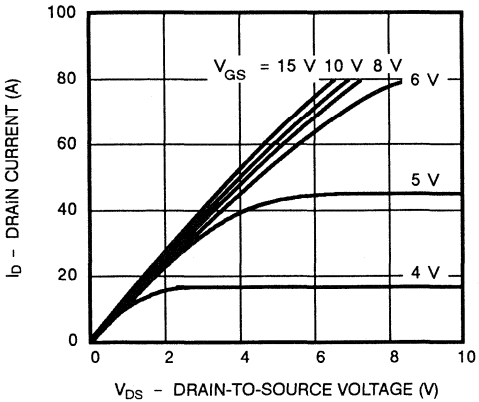


Figure 2. Transfer Characteristics

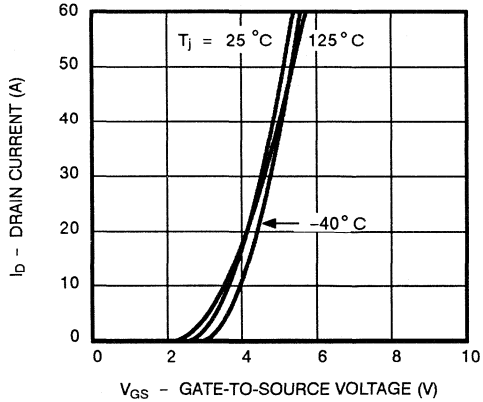


Figure 3. Transconductance

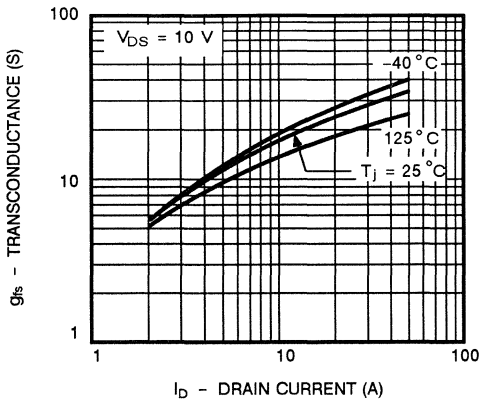


Figure 4. On-Resistance

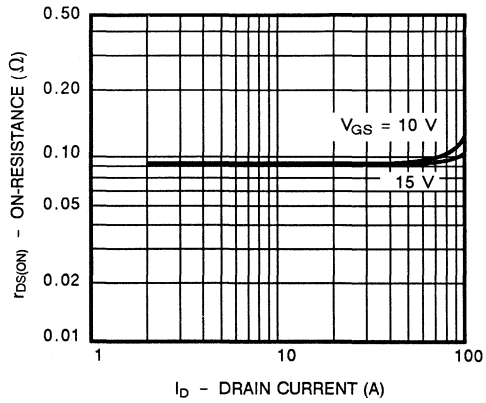


Figure 5. Capacitance

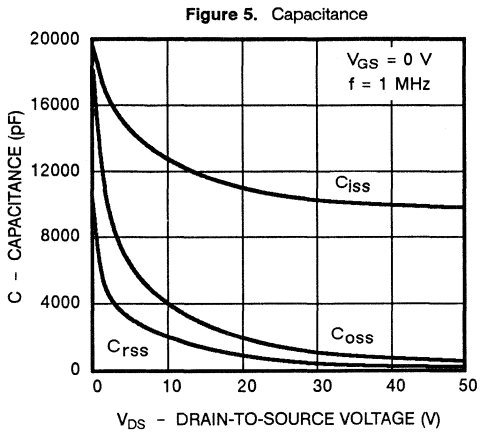
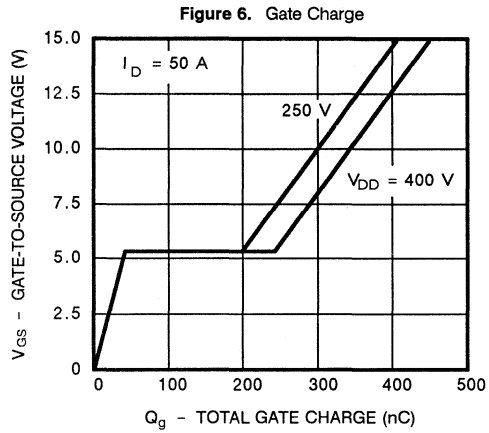


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

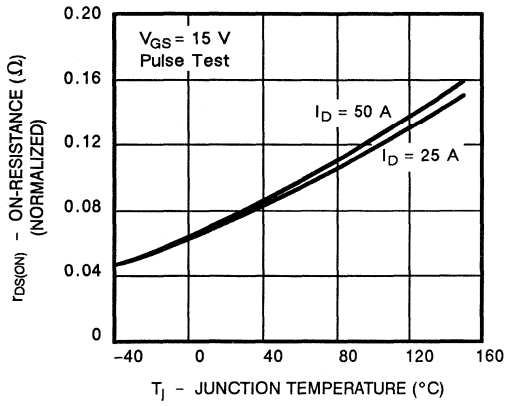
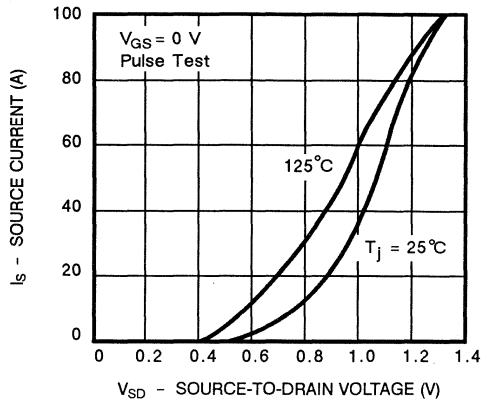


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Safe Operating Area

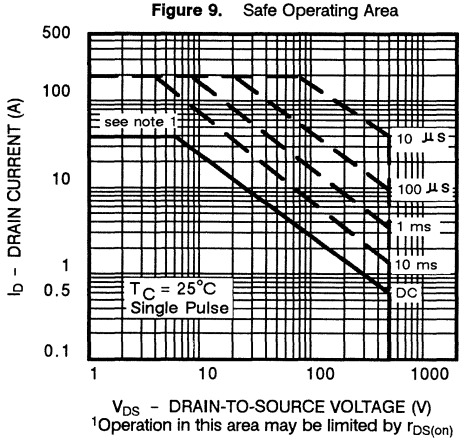
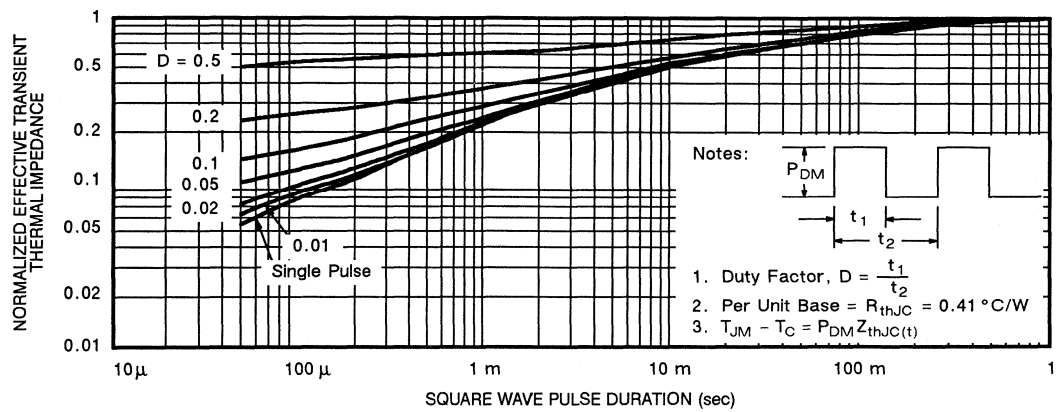


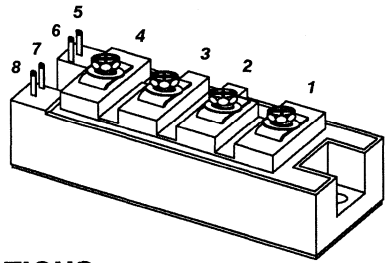
Figure 10. Normalized Effective Transient Thermal Impedance, Junction-to-Case

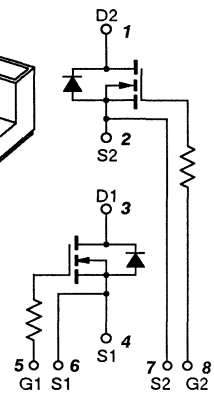


Siliconix incorporated

SPMF50A500

Power MOSFET Module





PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	V_{ISOL} (V)
500	0.100	50	2500

FEATURES:

- Two Independent Transistors
- Fast Intrinsic Diode (270 ns)
- Short Circuit Withstand Time Rated
- Isolated Plastic Package
- Very Low On-Resistance
- High Frequency Operation (>20 kHz)

APPLICATIONS:

- Uninterruptible Power Supply
- Switch-mode Power
- Motor Control
- Arc Welding Inverters
- Induction Heating

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±20	
Operating Drain Current[1]	I_D	50	A
Pulsed Drain Current[2]	I_{DM}	200	
Total Power Dissipation (per Transistor)	P_D	400	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-40 to 125	
Isolation Voltage (RMS)	V_{ISO}	2500	V
Short Circuit Withstand Time (V_{DD} = 350 V, V_{GS} = 10 V)	SCWT	12	µS

MECHANICAL DATA

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Mounting Torque (Maximum)	Mounting Base (M6)		50 (43 in-lbs)	kgf.cm
	Terminals (M5)		50 (43 in-lbs)	
Mass			240	g
Thermal Resistance (Junction to Baseplate per MOSFET)		R_{thJC}	0.31	°C/W

[1]For duty cycles ≤ 80%.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 mA		1.5	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			1.0	mA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			4.0	
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 15 V, I_D = 25 A	0.08		0.10	Ω
		V_{GS} = 15 V, I_D = 25 A, T_J = 125°C	0.15		0.22	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 25 A	20			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	11000			pF
Output Capacitance	C_{oss}		1600			
Reverse Transfer Capacitance	C_{rss}		800			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 15 V, I_D = 50 A	400		600	nC
Gate-Source Charge[2]	Q_{gs}		40		64	
Gate-Drain Charge[2]	Q_{gd}		160		320	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{GS} = 15 V, R_L = 12 Ω $I_D \simeq$ 25 A, V_{DD} = 300 V, R_G = 10 Ω	70			ns
Rise Time[2]	t_r		100			
Turn-Off Delay Time[2]	$t_{d(off)}$		950			
Fall Time[2]	t_f		250			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				50	A
Pulsed Current[3]	I_{SM}				200	
Source-Drain Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 200 A/µs, I_F = 25 A, V_R = 100 V	270		300	ns

Siliconix modules utilize the intrinsic Drain-Source diodes of the MOSPOWER chips as anti-parallel diodes. Through proprietary technology these diodes are processed for fast recovery and low V_{SD}. This means that the current handling capability of Siliconix modules is symmetrical, that is, the diode portion can handle the same peak and average current as the transistor and has the same low thermal impedance.

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

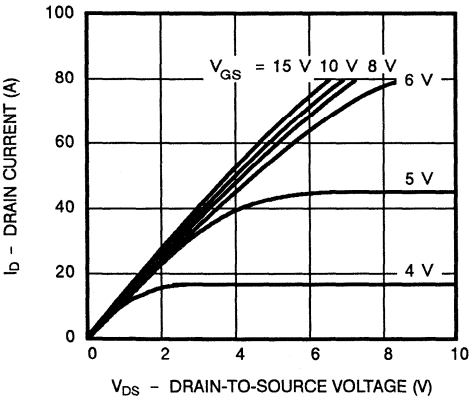


Figure 2. Transfer Characteristics

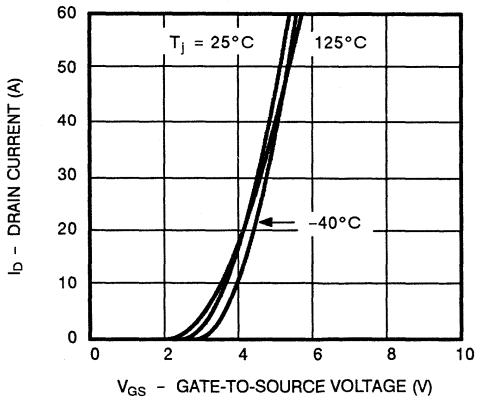


Figure 3. Transconductance

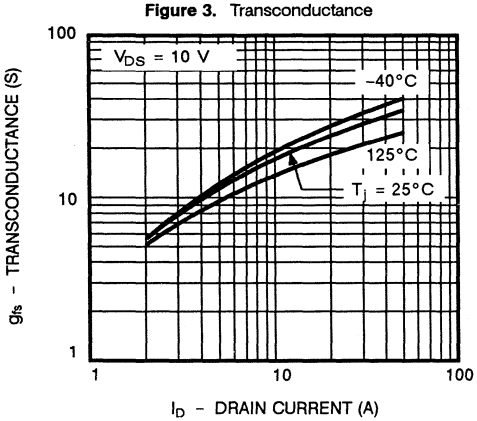


Figure 4. On-Resistance

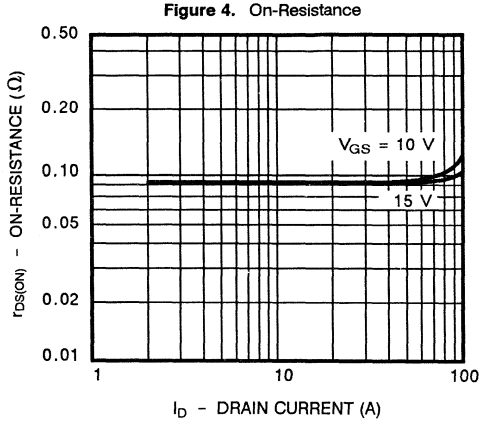


Figure 5. Capacitance

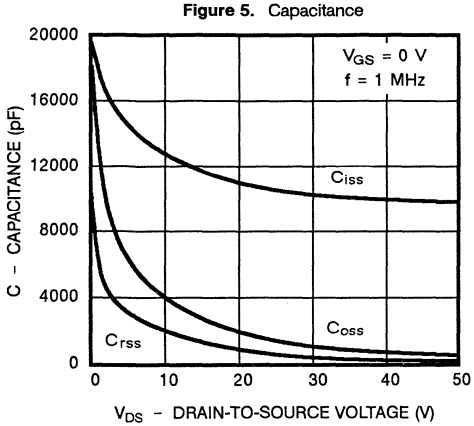
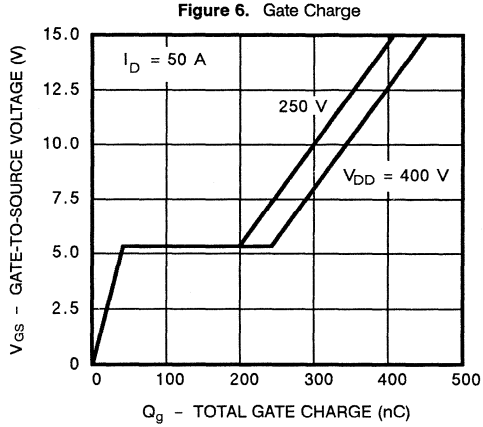


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

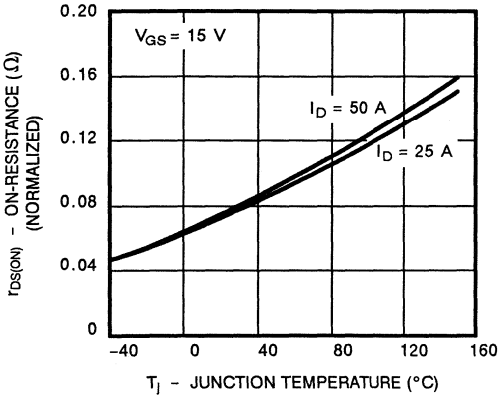
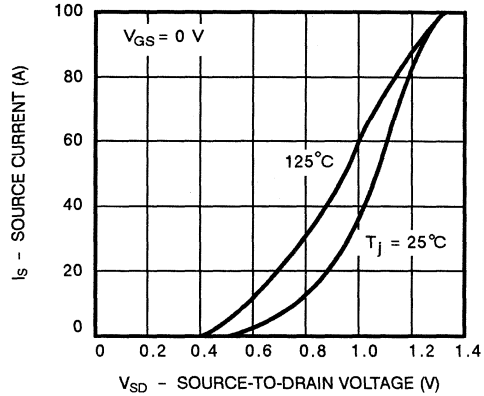


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Safe Operating Area

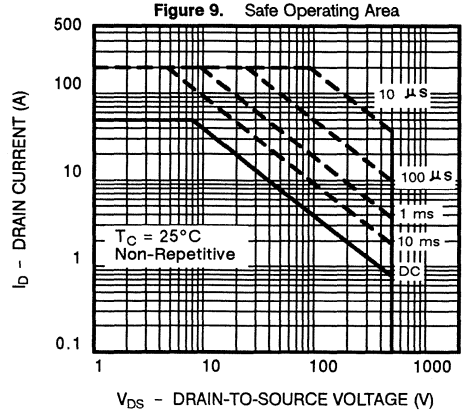
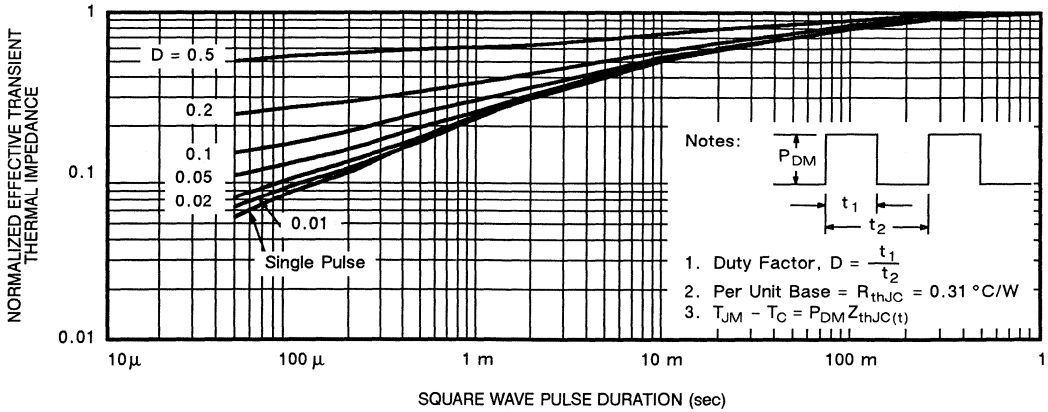


Figure 10. Normalized Effective Transient Thermal Impedance, Junction-to-Case

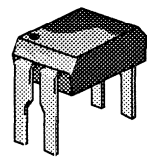


Siliconix incorporated

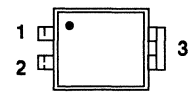
2N7012

N-Channel Enhancement Mode Transistor

4-PIN DIP
(Similar to TO-250)



TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.35	1.2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	1.2	A
	T_A = 100°C		0.80	
Pulsed Drain Current[1]		I_{DM}	10	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	R_{thJA}		120	K/W

[1]Pulse width limited by maximum junction temperature.

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		1.2		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1.0 A	0.3		0.35	Ω
		V_{GS} = 10 V, I_D = 1.0 A, T_J = 125°C	0.55		0.64	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1.0 A	1.5	1.2		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	220		300	pF
Output Capacitance	C_{oss}		120		200	
Reverse Transfer Capacitance	C_{rss}		30		100	
Total Gate Charge[2]	Q_g	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A	4.8		6.0	nC
Gate-Source Charge[2]	Q_{gs}		1			
Gate-Drain Charge[2]	Q_{gd}		2			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 25 Ω, $I_D \simeq$ 1.2 A, V_{GEN} = 10 V, R_G = 25 Ω	7		20	ns
Rise Time[2]	t_r		13		30	
Turn-Off Delay Time[2]	$t_{d(off)}$		18		30	
Fall Time[2]	t_f		13		25	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_A = 25°C)						
Continuous Current	I_S				1.2	A
Pulsed Current[3]	I_{SM}				10	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	45			ns
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

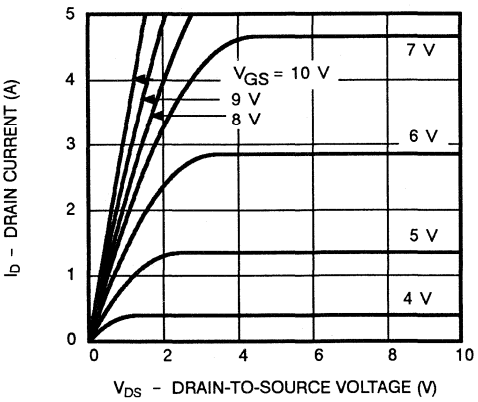


Figure 2. Transfer Characteristics

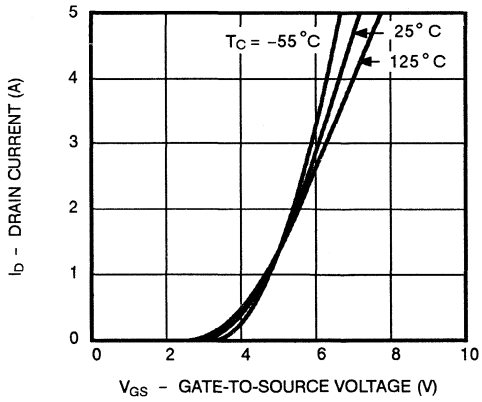


Figure 3. Transconductance

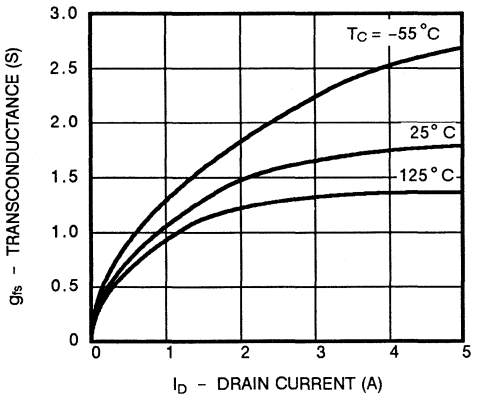


Figure 4. On-Resistance

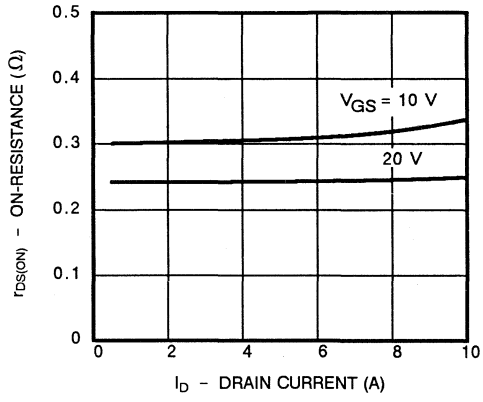


Figure 5. Capacitance

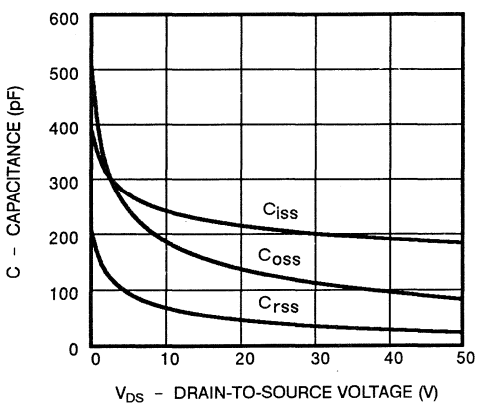
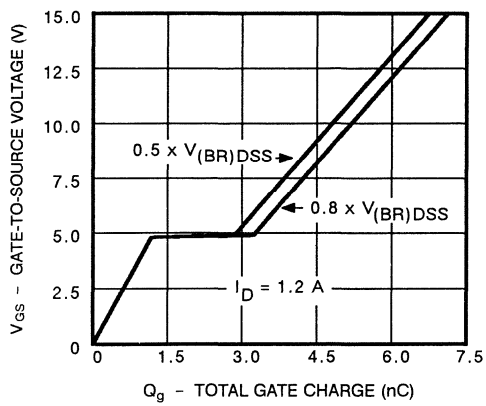


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

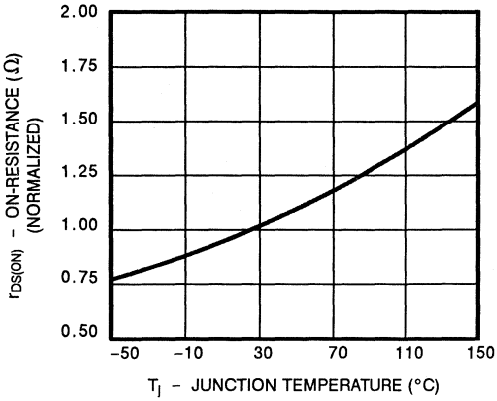
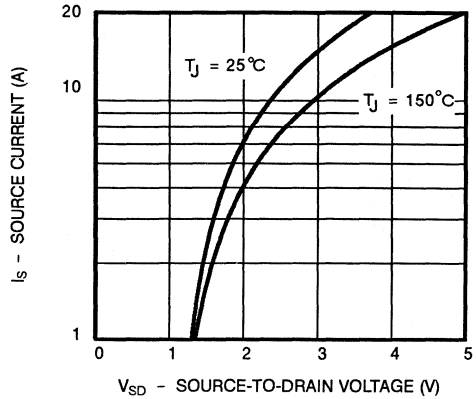


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

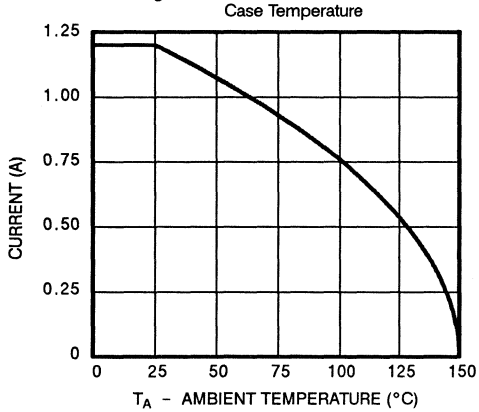
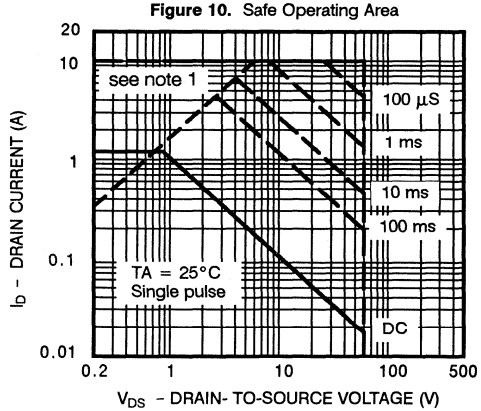


Figure 10. Safe Operating Area



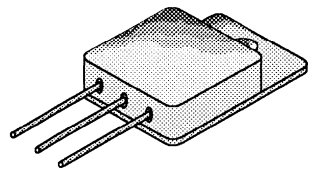
[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

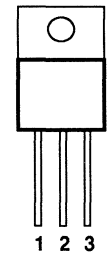
2N7071

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.100	23

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	23	A
	T_C = 100°C		15	
Pulsed Drain Current[1]		I_{DM}	92	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		24		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A	0.075		0.100	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	0.12		0.16	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 15 A	10	6.0	18	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1550			pF
Output Capacitance	C_{oss}		550			
Reverse Transfer Capacitance	C_{rss}		150			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D ≃ 23 A	50	30	77	nC
Gate-Source Charge[2]	Q_{gs}		10	4.6	13	
Gate-Drain Charge[2]	Q_{gd}		23	13	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 2.1 Ω, I_D ≃ 23 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		30	ns
Rise Time[2]	t_r		80		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		30		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				23	A
Pulsed Current[3]	I_{SM}				92	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150		300	ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

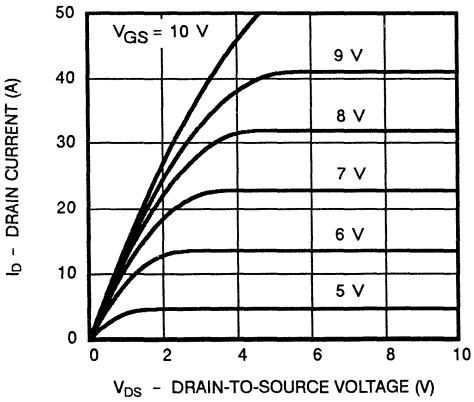


Figure 2. Transfer Characteristics

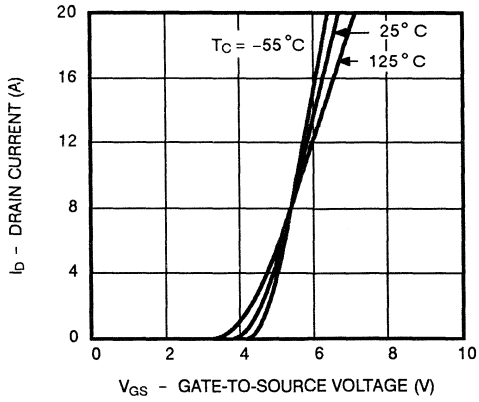


Figure 3. Transconductance

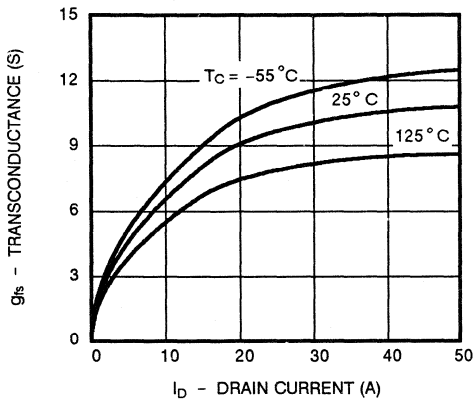


Figure 4. On-Resistance

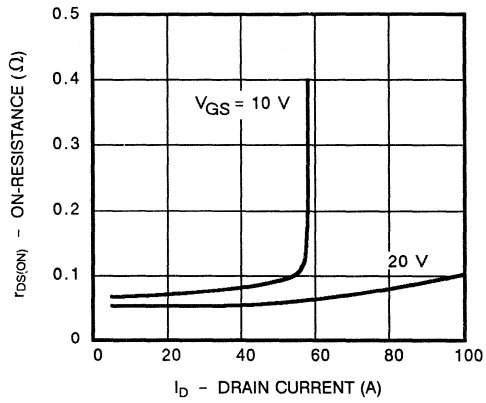


Figure 5. Capacitance

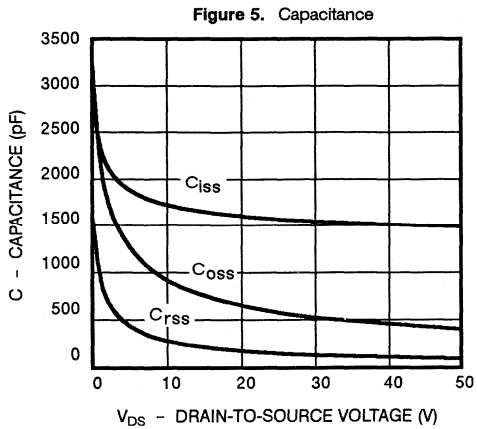
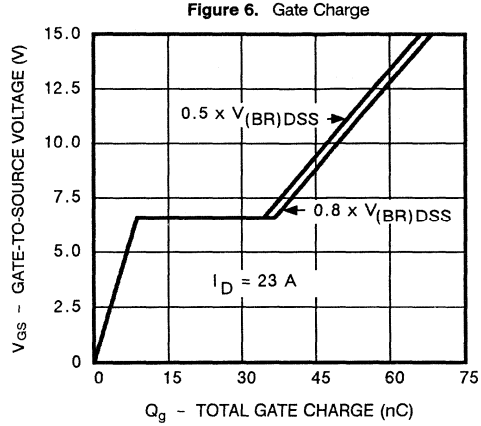


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

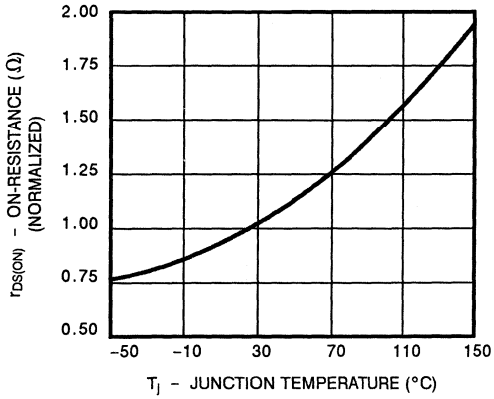
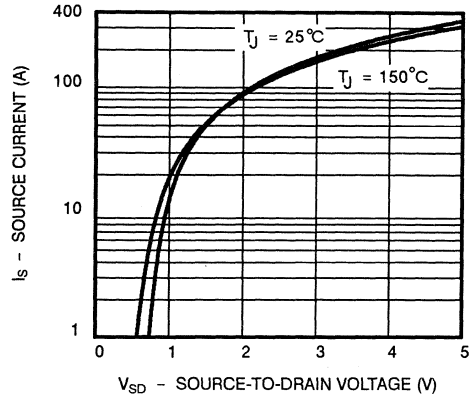


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

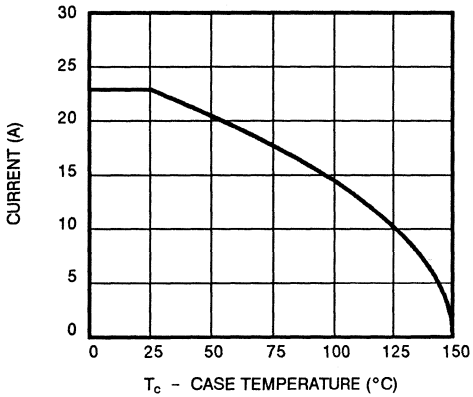
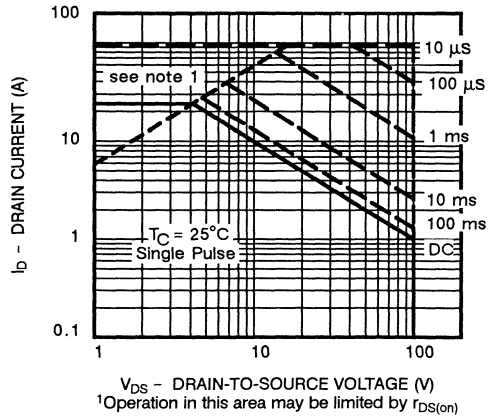
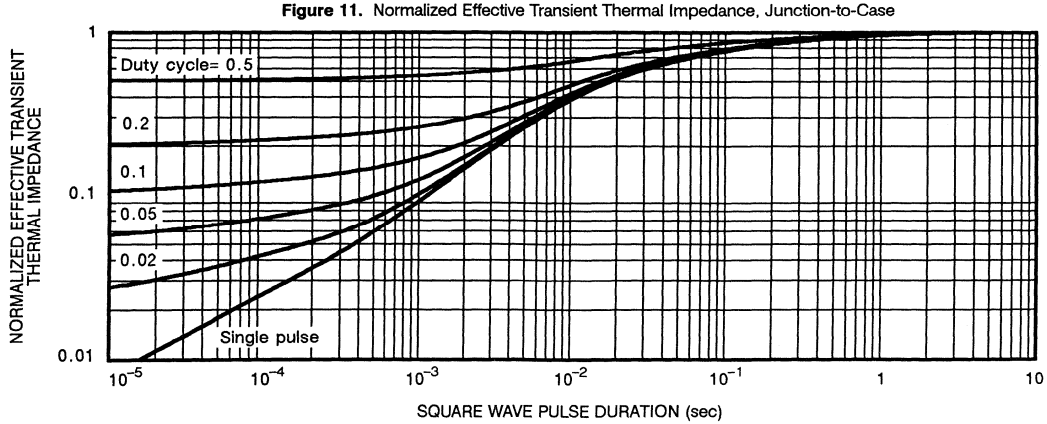


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

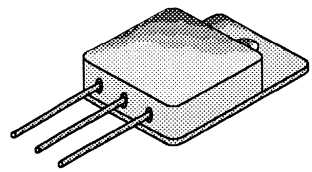


Siliconix incorporated

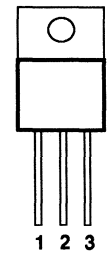
2N7072

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	0.20	16

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	16	A
	T_C = 100°C		10	
Pulsed Drain Current[1]		I_{DM}	64	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		16		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 A	0.14		0.20	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	0.26		0.36	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	8.0	6.0	18	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1550			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		220			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 16 A	42	30	77	nC
Gate-Source Charge[2]	Q_{gs}		9	4.6	13	
Gate-Drain Charge[2]	Q_{gd}		22	13	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 6.25 Ω, $I_D \simeq$ 16 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		30	ns
Rise Time[2]	t_r		60		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		20		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				16	A
Pulsed Current[3]	I_{SM}				64	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150		300	ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

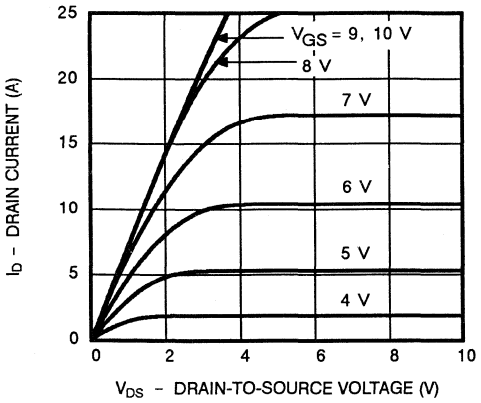


Figure 2. Transfer Characteristics

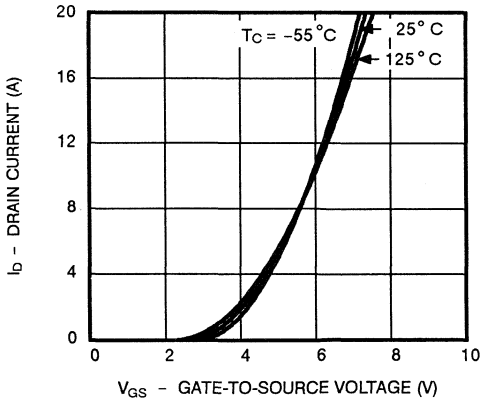


Figure 3. Transconductance

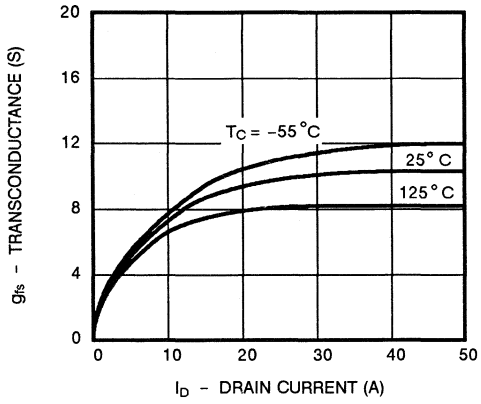


Figure 4. On-Resistance

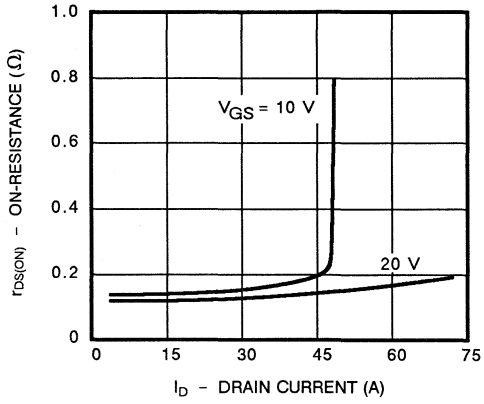


Figure 5. Capacitance

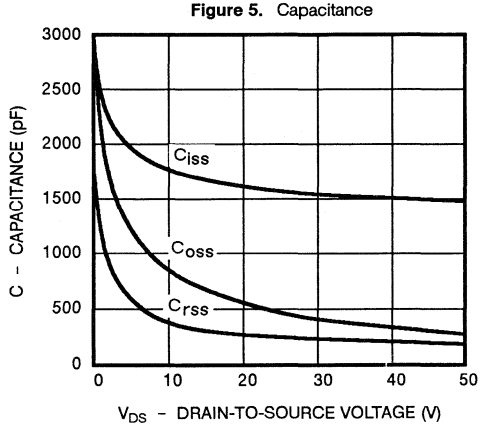
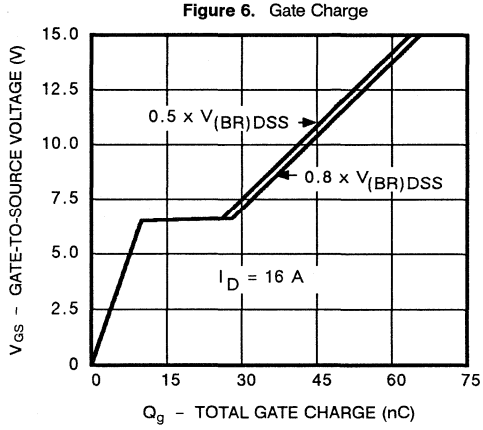


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

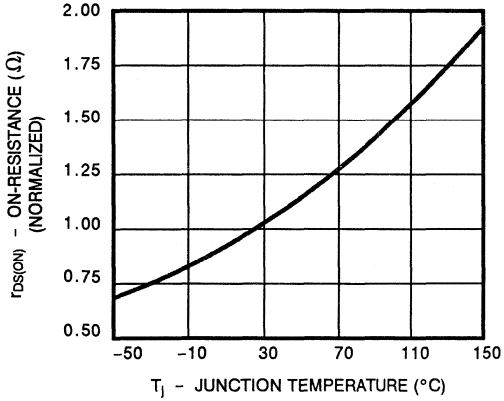
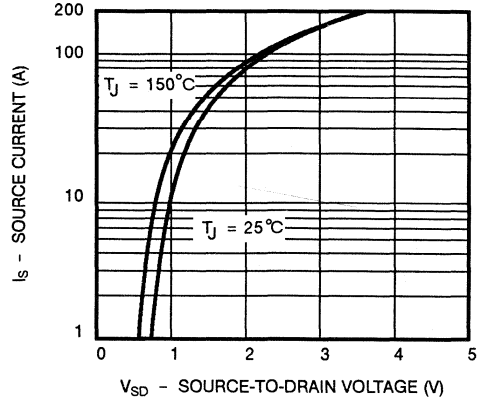


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

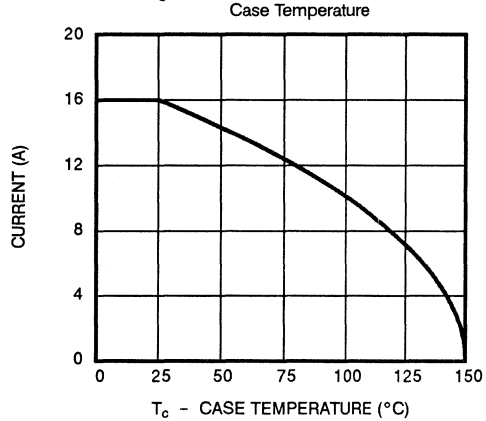
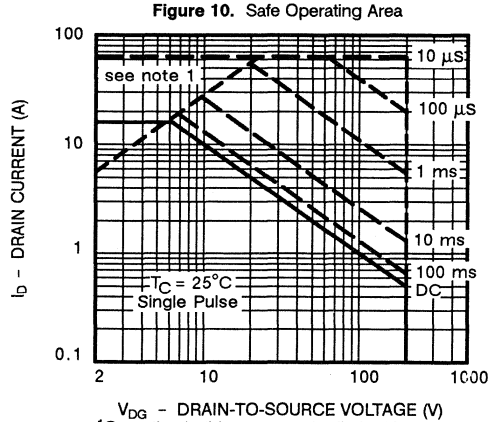
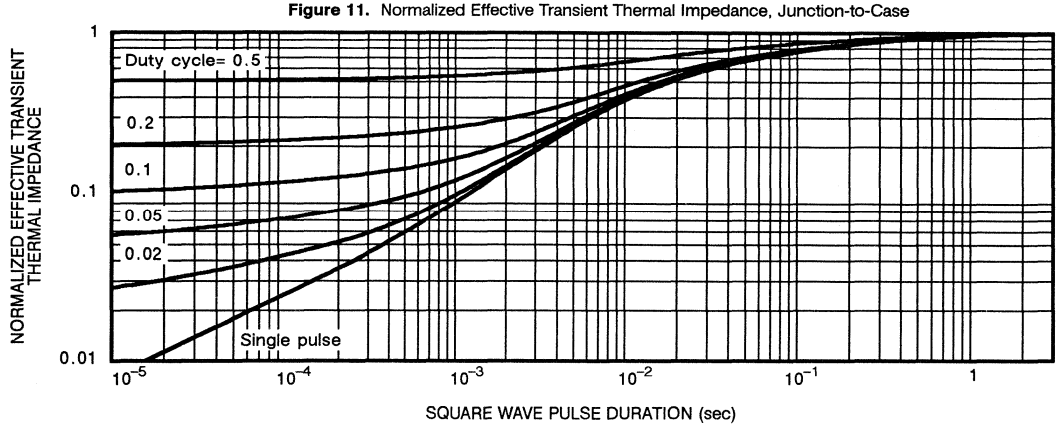


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

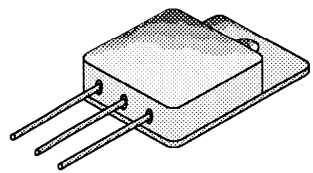


Siliconix incorporated

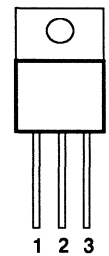
2N7073

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
400	0.55	9.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	9.0	A
	T_C = 100°C		5.5	
Pulsed Drain Current[1]		I_{DM}	36	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		400		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 320 V, V_{GS} = 0 V			25	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		9.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5.5 A	0.45		0.55	Ω
		V_{GS} = 10 V, I_D = 5.5 A, T_J = 125°C	0.90		1.1	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5.5 A	4.8	4.0	12	S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1500			pF
Output Capacitance	C_{oss}		300			
Reverse Transfer Capacitance	C_{rss}		120			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9 A	58	30	77	nC
Gate-Source Charge[2]	Q_{gs}		10	4.6	13	
Gate-Drain Charge[2]	Q_{gd}		27	13	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 200 V, R_L = 22 Ω, $I_D \simeq$ 9 A, V_{GEN} = 10 V, R_G = 4.7 Ω	16		40	ns
Rise Time[2]	t_r		28		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		54		110	
Fall Time[2]	t_f		30		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				9.0	A
Pulsed Current[3]	I_{SM}				36	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	250		500	ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

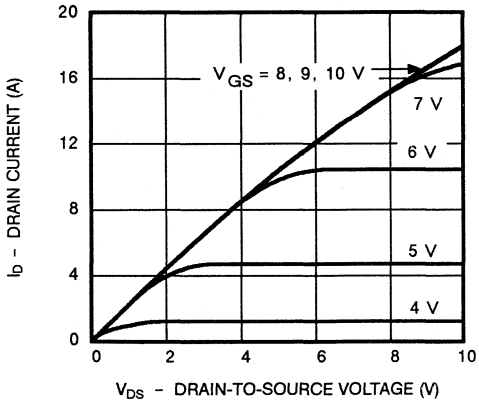


Figure 2. Transfer Characteristics

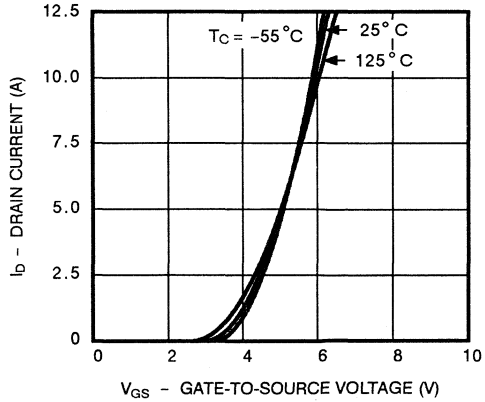


Figure 3. Transconductance

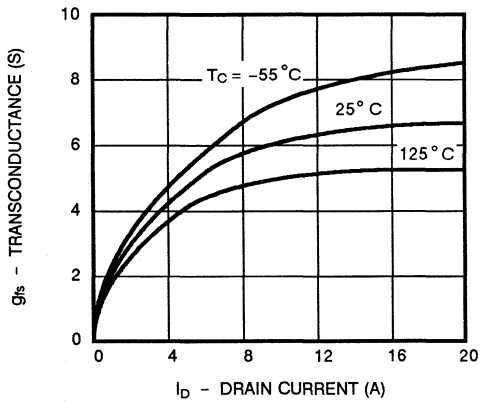


Figure 4. On-Resistance

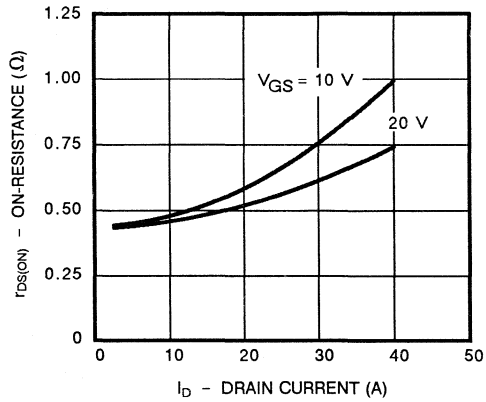


Figure 5. Capacitance

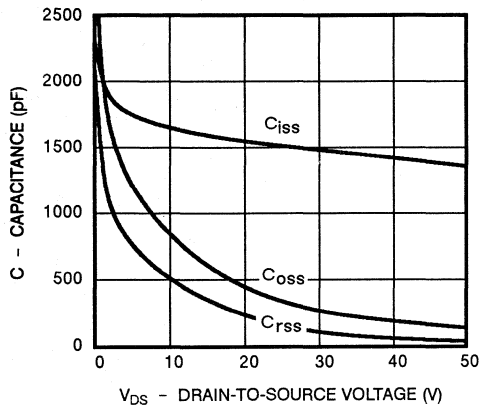
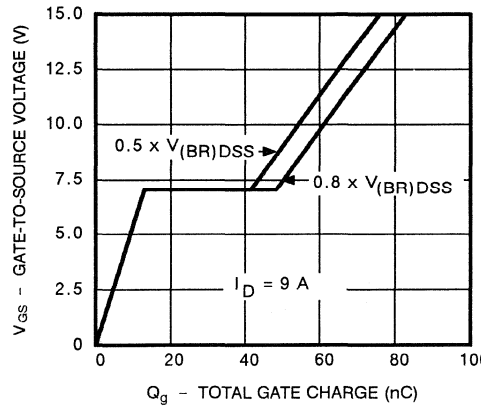


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

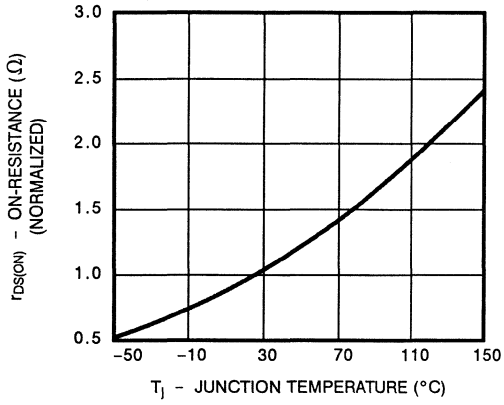
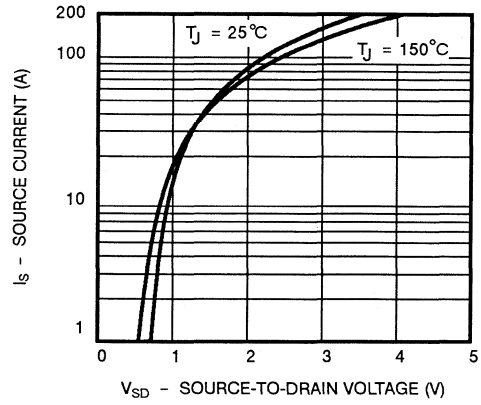


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

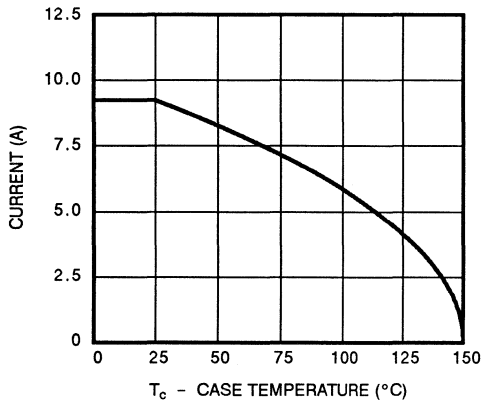
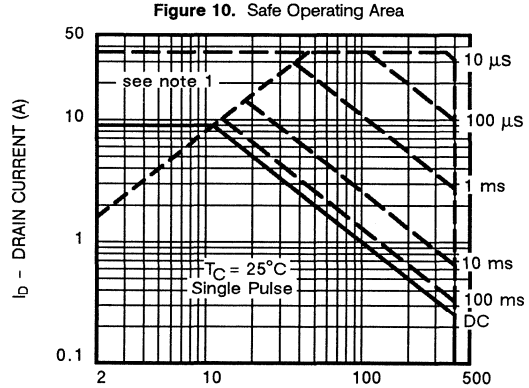
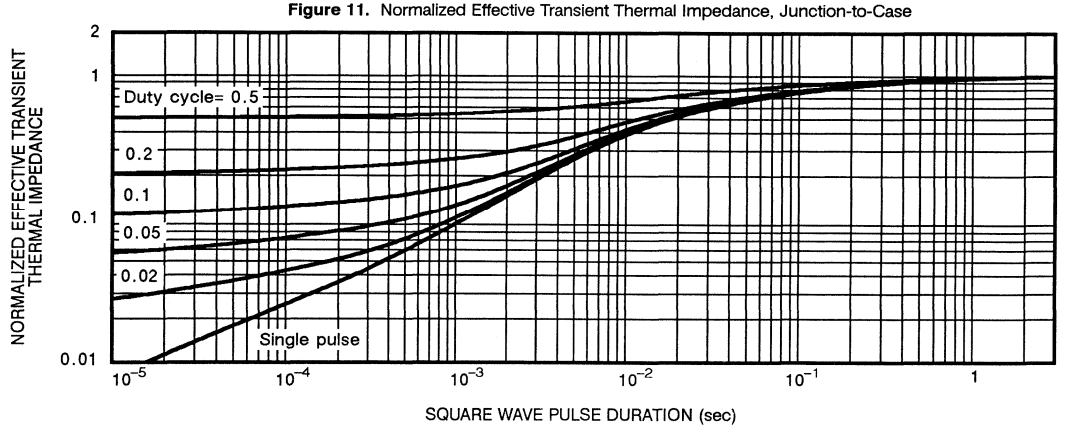


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

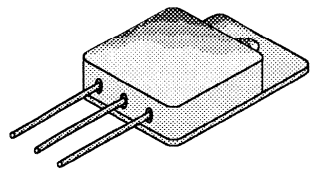


Siliconix incorporated

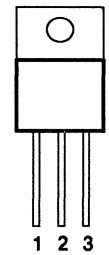
2N7074

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
500	0.85	7.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.5	
Pulsed Drain Current[1]		I_{DM}	28	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V			25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		7.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 4.5 A	0.8		0.85	Ω
		V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C	1.40		1.62	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A	4.3	4.0	12	S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1500			pF
Output Capacitance	C_{oss}		250			
Reverse Transfer Capacitance	C_{rss}		75			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7 A	54	30	77	nC
Gate-Source Charge[2]	Q_{gs}		10	4.6	13	
Gate-Drain Charge[2]	Q_{gd}		26	13	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 36 Ω, $I_D \simeq$ 7 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		40	ns
Rise Time[2]	t_r		20		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		110	
Fall Time[2]	t_f		18		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				7.0	A
Pulsed Current[3]	I_{SM}				28	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	250		500	ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

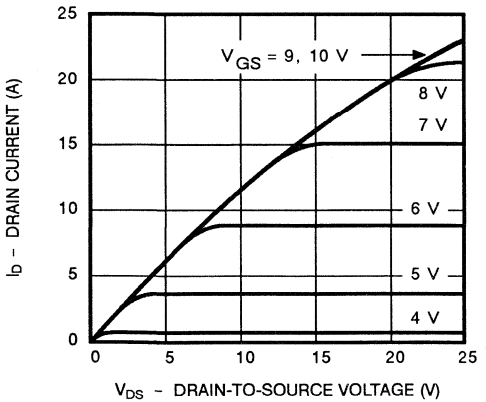


Figure 2. Transfer Characteristics

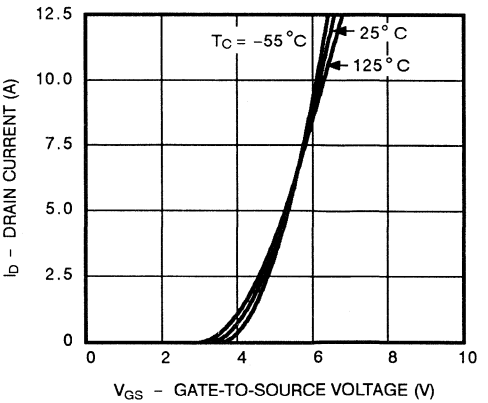


Figure 3. Transconductance

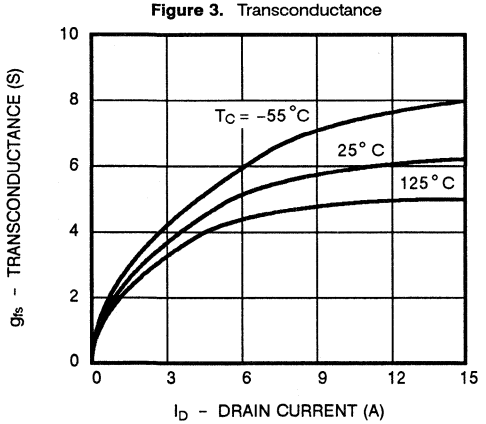


Figure 4. On-Resistance

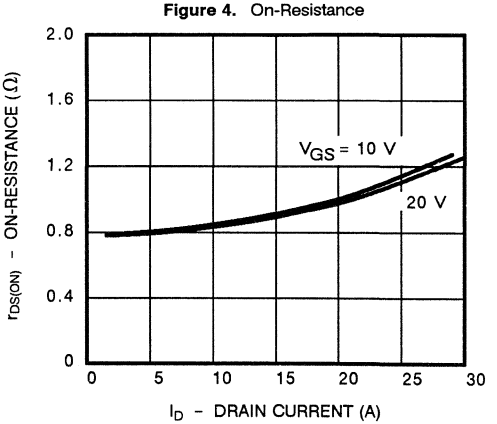


Figure 5. Capacitance

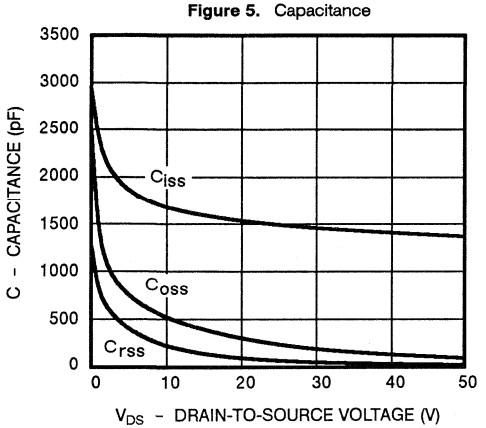
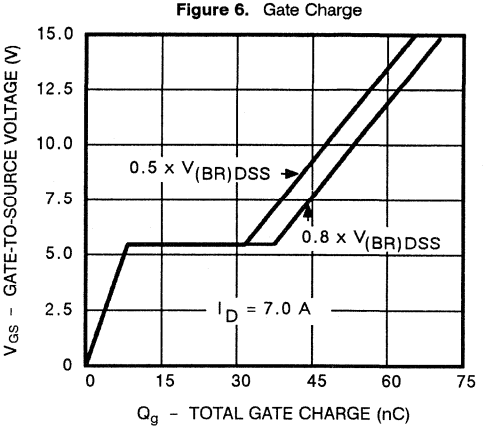


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

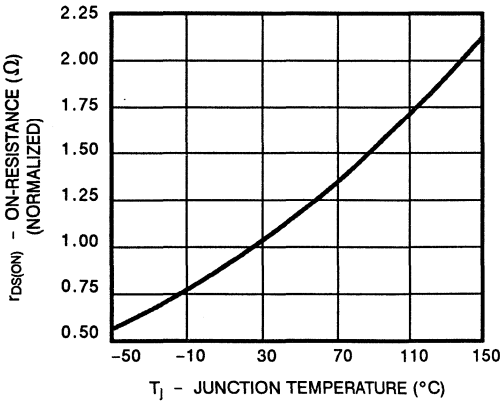
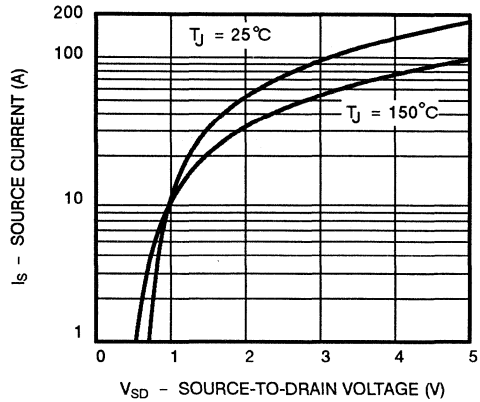


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

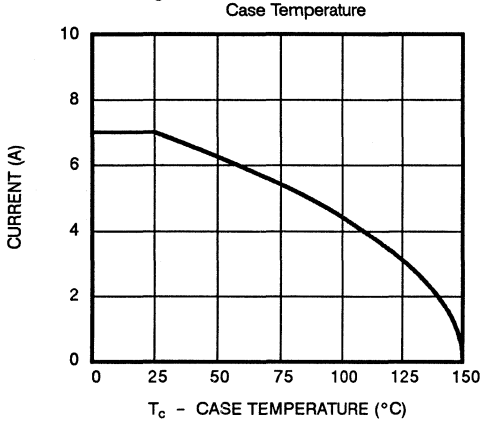
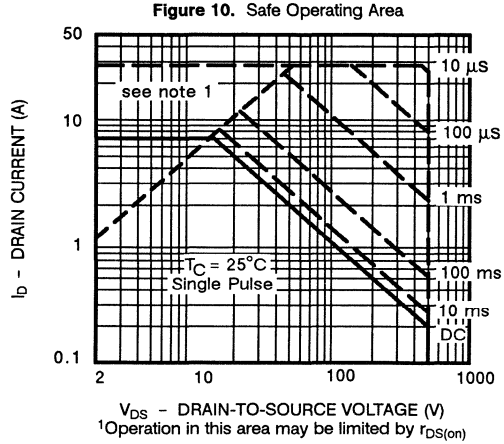
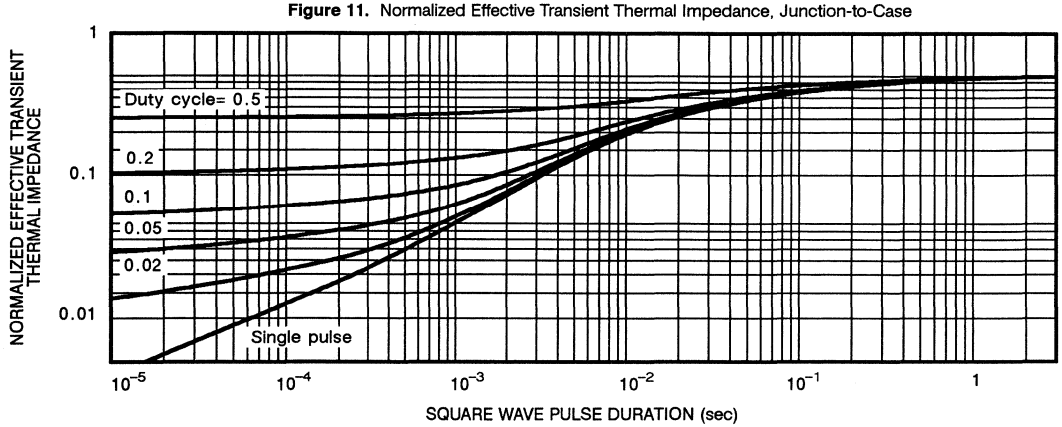


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

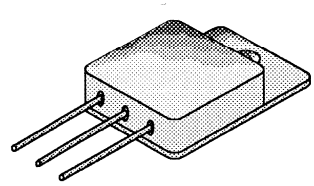


Siliconix incorporated

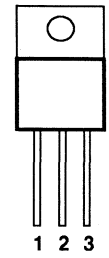
2N7075

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.065	30

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		24	
Pulsed Drain Current[1]		I_{DM}	120	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		30		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 24 A	0.053		0.065	Ω
		V_{GS} = 10 V, I_D = 24 A, T_J = 125°C	0.08		0.10	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 24 A	11	9	27	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2800			pF
Output Capacitance	C_{oss}		1100			
Reverse Transfer Capacitance	C_{rss}		400			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A	62	50	125	nC
Gate-Source Charge[2]	Q_{gs}		17	8.0	22	
Gate-Drain Charge[2]	Q_{gd}		35	25	65	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.67 Ω, I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.4 Ω	15		35	ns
Rise Time[2]	t_r		80		150	
Turn-Off Delay Time[2]	$t_{d(off)}$		60		125	
Fall Time[2]	t_f		50 •		100	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				30	A
Pulsed Current[3]	I_{SM}				120	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	1.9	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	180		400	ns
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

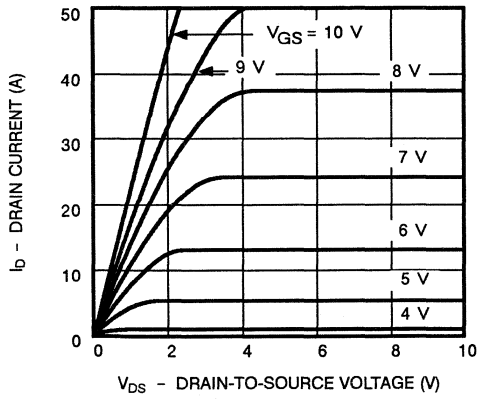


Figure 2. Transfer Characteristics

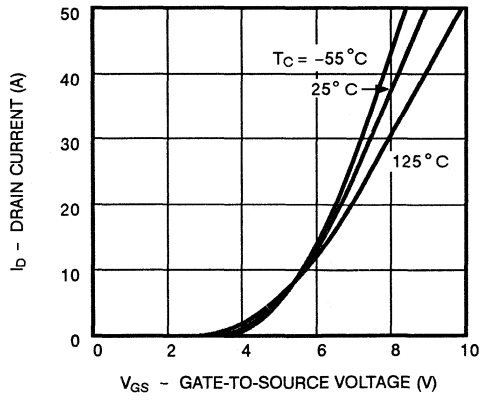


Figure 3. Transconductance

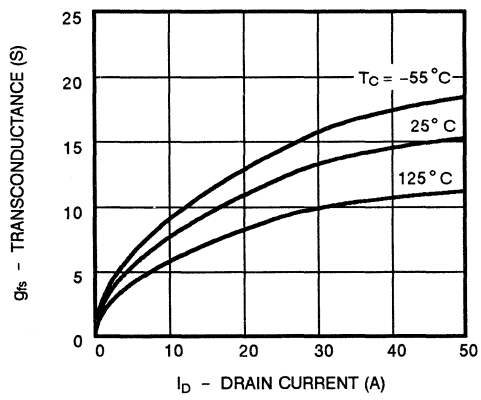


Figure 4. On-Resistance

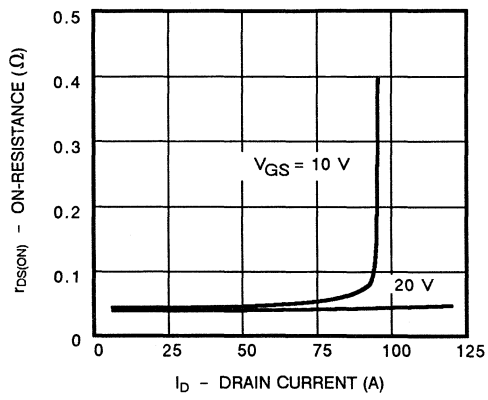


Figure 5. Capacitance

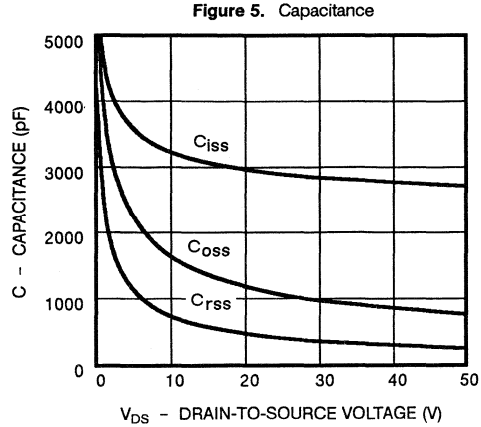
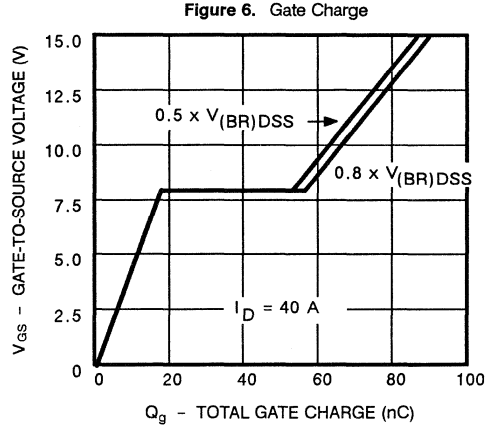


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

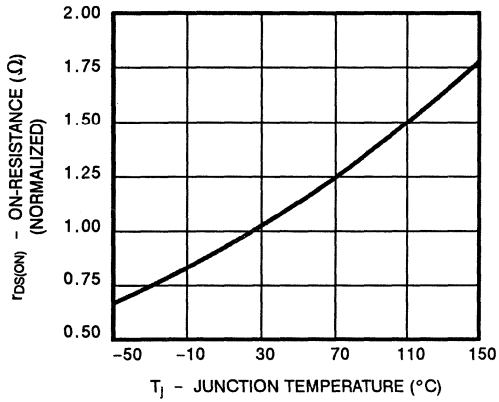
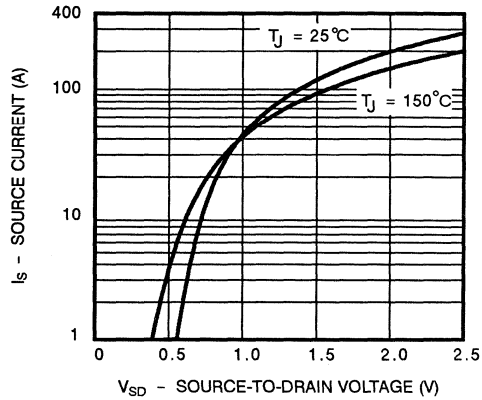


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

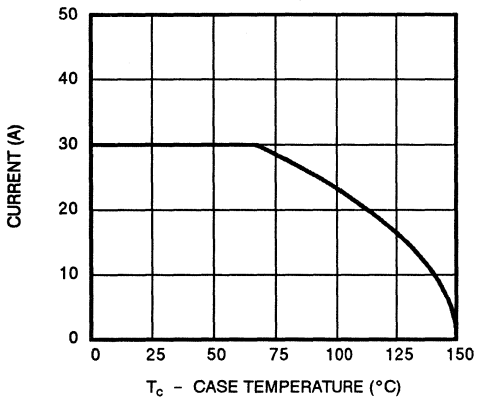
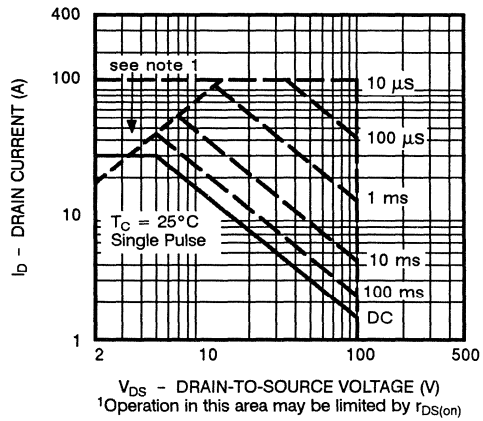
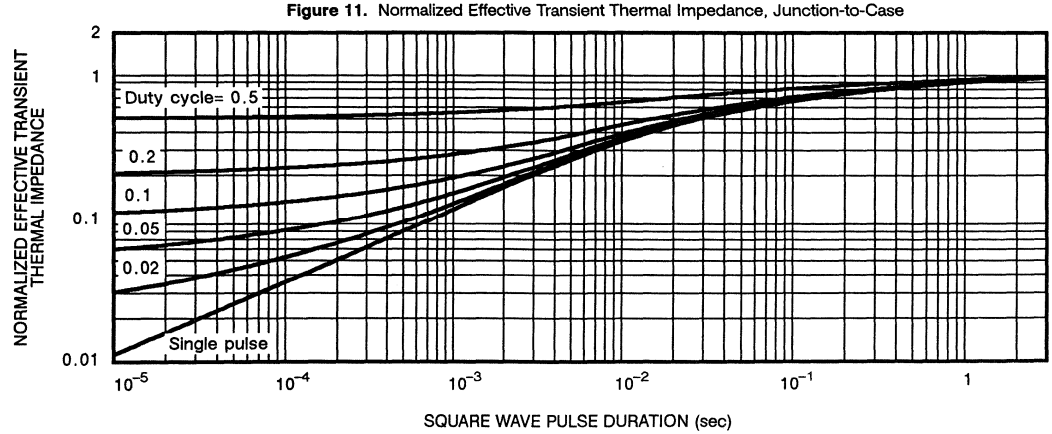


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

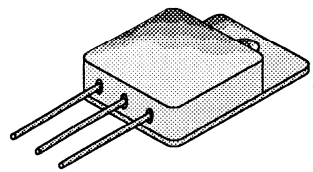


Siliconix incorporated

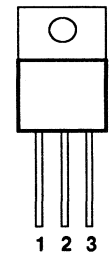
2N7076

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	0.10	28

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	28	A
	T_C = 100°C		18	
Pulsed Drain Current[1]		I_{DM}	112	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		28		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 18 A	0.080		0.100	Ω
		V_{GS} = 10 V, I_D = 18 A, T_J = 125°C	0.15		0.170	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 18 A	12	9.0	27	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700			pF
Output Capacitance	C_{oss}		850			
Reverse Transfer Capacitance	C_{rss}		300			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 28 A	63	55	115	nC
Gate-Source Charge[2]	Q_{gs}		14	10	21	
Gate-Drain Charge[2]	Q_{gd}		32	30	60	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 3.6 Ω, $I_D \simeq$ 28 A, V_{GEN} = 10 V, R_G = 2.4 Ω	15		35	ns
Rise Time[2]	t_r		100		150	
Turn-Off Delay Time[2]	$t_{d(off)}$		70		125	
Fall Time[2]	t_f		50		100	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				28	A
Pulsed Current[3]	I_{SM}				112	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.6	1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	175		650	ns
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

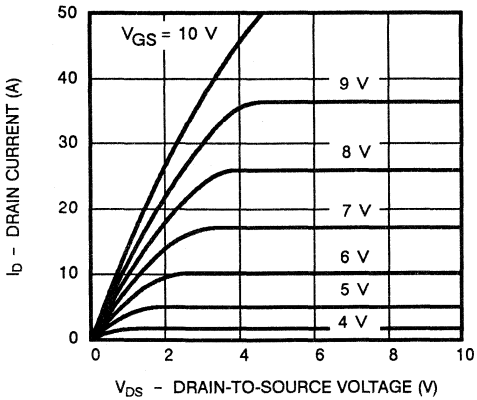


Figure 2. Transfer Characteristics

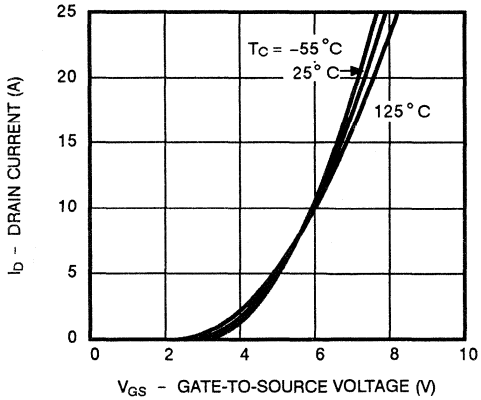


Figure 3. Transconductance

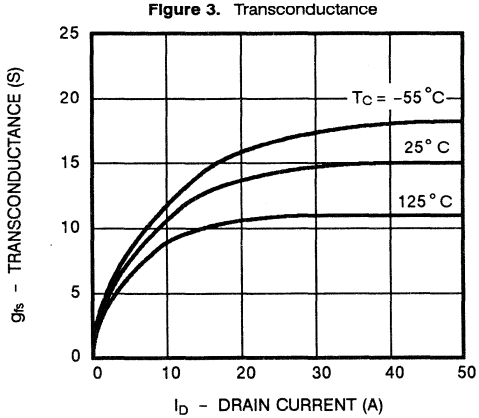


Figure 4. On-Resistance

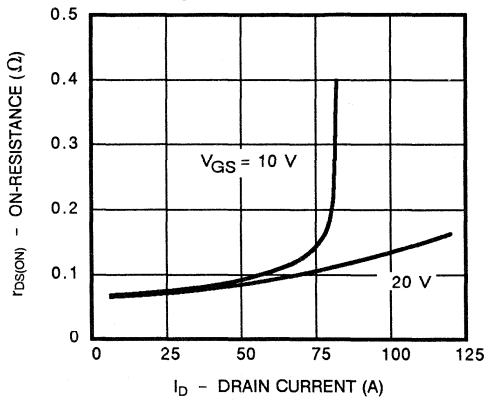


Figure 5. Capacitance

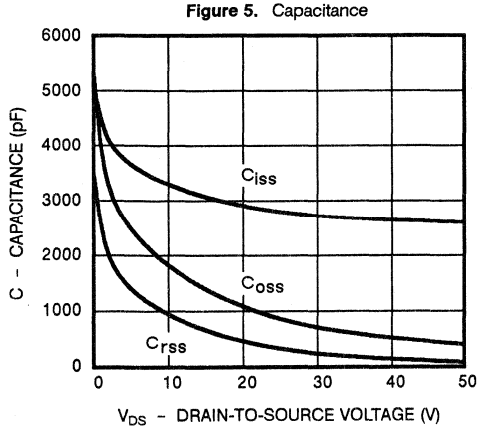
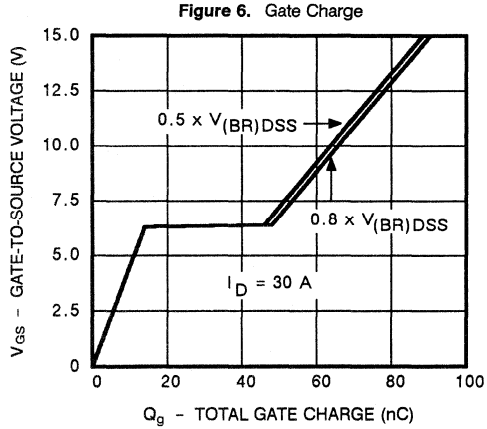


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

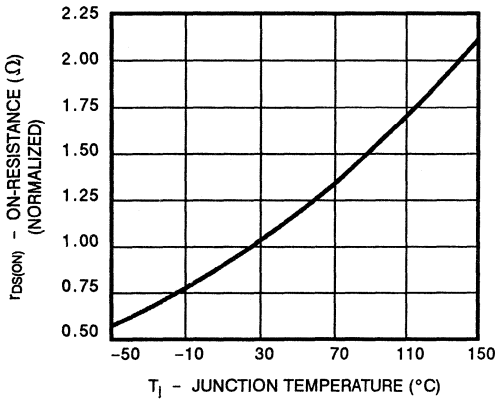
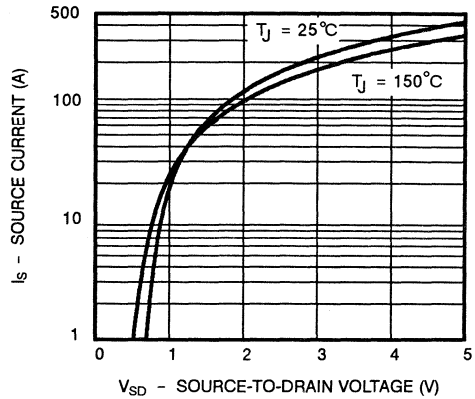


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

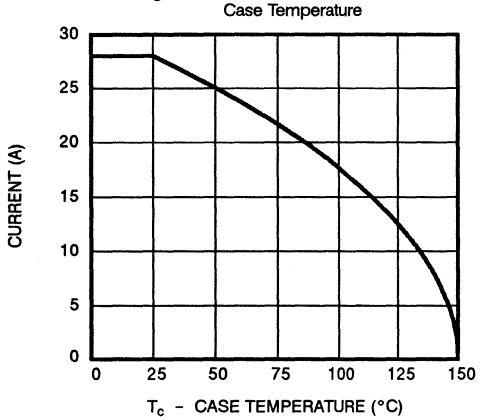
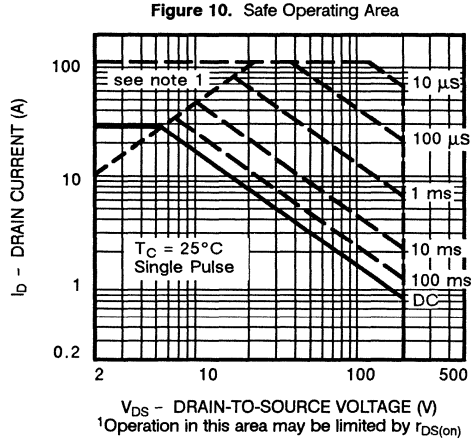
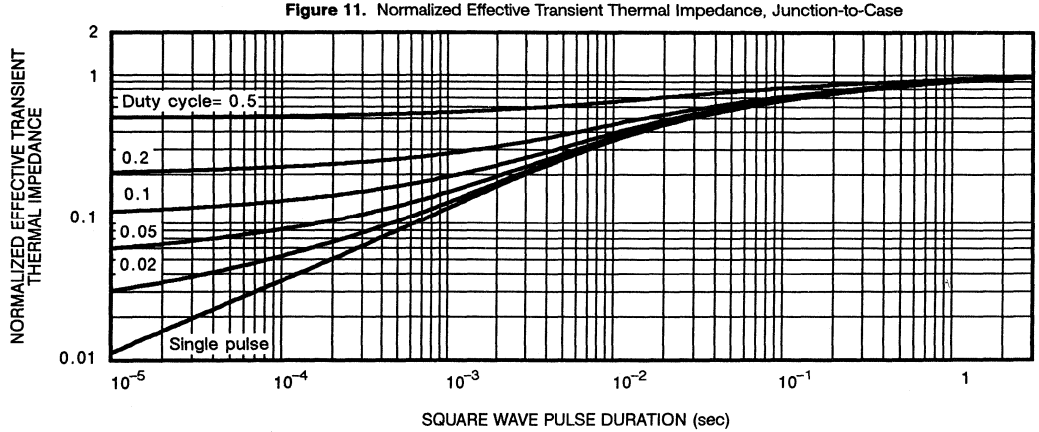


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

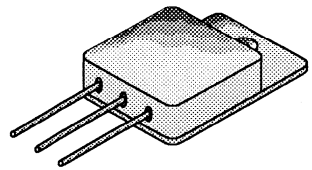


Siliconix incorporated

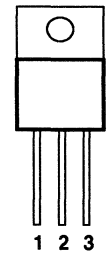
2N7077

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
400	0.30	15

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	15	A
	T_C = 100°C		9.5	
Pulsed Drain Current[1]		I_{DM}	60	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($1/16$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		400		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 320 V, V_{GS} = 0 V			25	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		15.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 9.5 A	0.23		0.30	Ω
		V_{GS} = 10 V, I_D = 9.5 A, T_J = 125°C	0.4		0.66	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 9.5 A	8.5		24	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700			pF
Output Capacitance	C_{oss}		450			
Reverse Transfer Capacitance	C_{rss}		160			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A	77	52	110	nC
Gate-Source Charge[2]	Q_{gs}		14	5.3	18	
Gate-Drain Charge[2]	Q_{gd}		39	25	65	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 200 V, R_L = 13 Ω, I_D ≃ 15 A, V_{GEN} = 10 V, R_G = 2.4 Ω	14		35	ns
Rise Time[2]	t_r		30		60	
Turn-Off Delay Time[2]	$t_{d(off)}$		54		150	
Fall Time[2]	t_f		15		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				15	A
Pulsed Current[3]	I_{SM}				60	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.85	1.7	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	350		800	ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

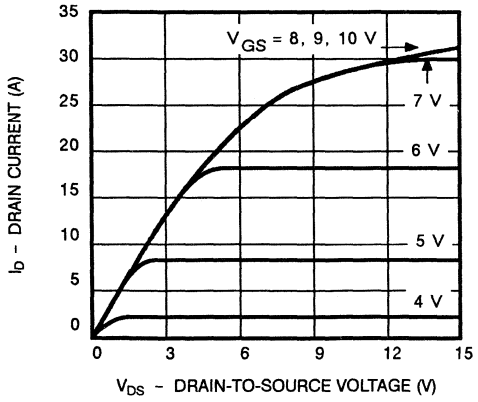


Figure 2. Transfer Characteristics

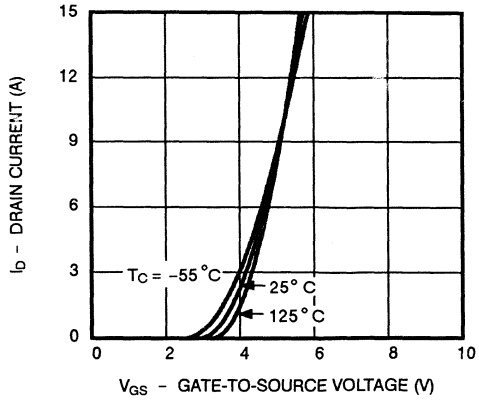


Figure 3. Transconductance

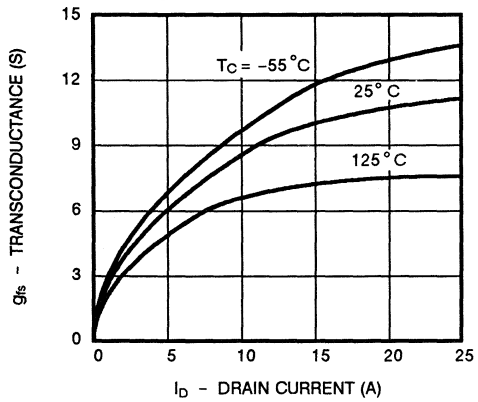


Figure 4. On-Resistance

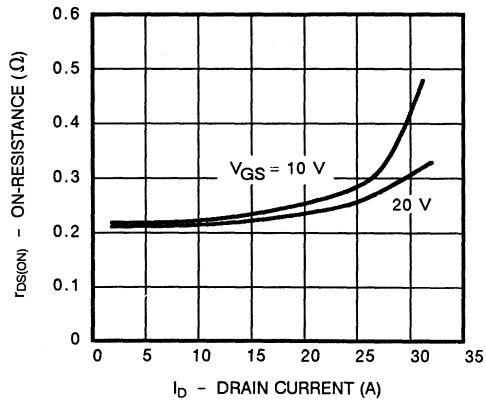


Figure 5. Capacitance

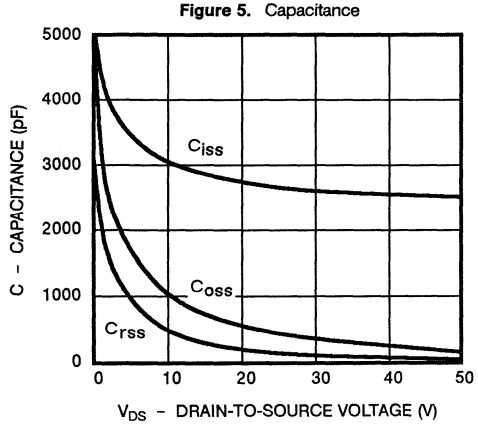
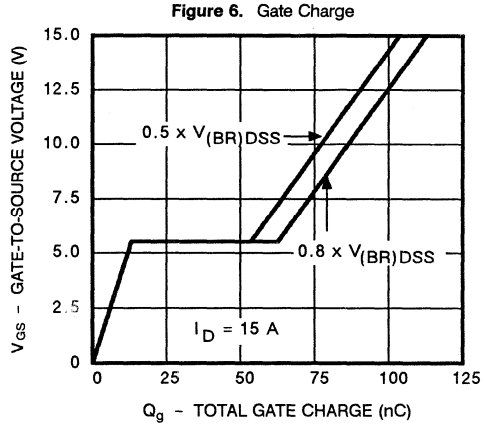


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

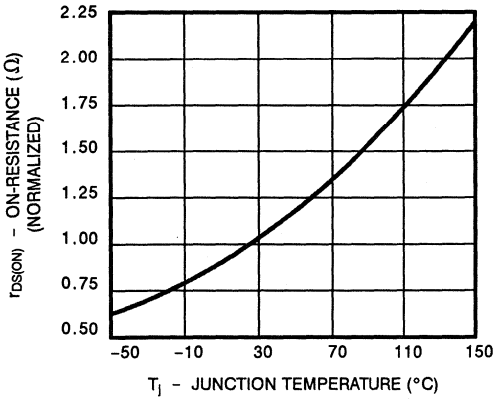
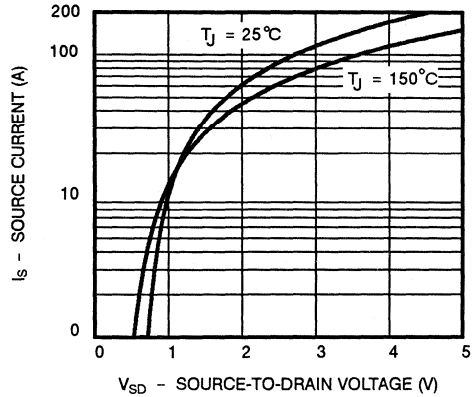


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

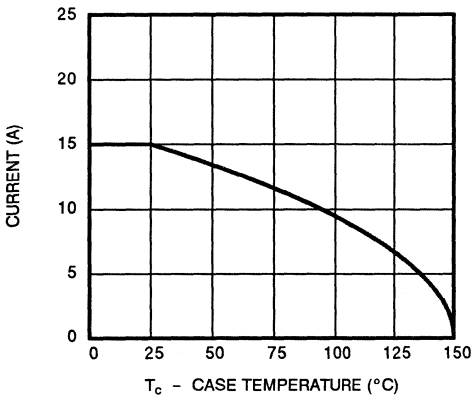
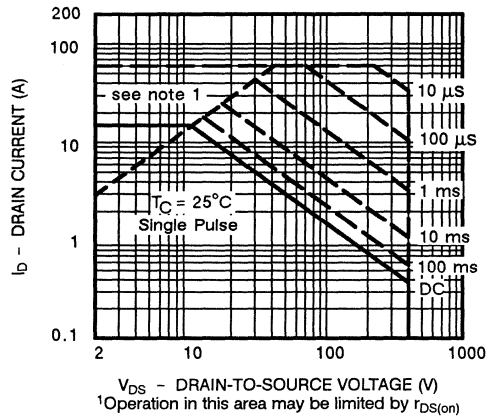
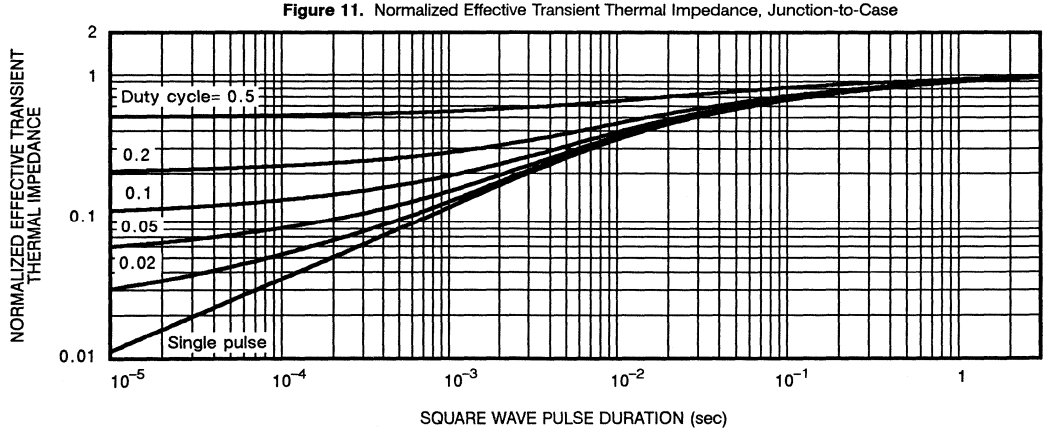


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

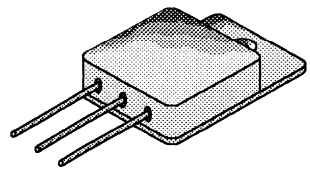


Siliconix incorporated

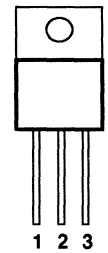
2N7078

N-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
500	0.40	13

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	13	A
	T_C = 100°C		8.0	
Pulsed Drain Current[1]		I_{DM}	50	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V			25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		13.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 8 A	0.31		0.40	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C	0.67		0.90	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	10	8.0	24	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2700			pF
Output Capacitance	C_{oss}		410			
Reverse Transfer Capacitance	C_{rss}		140			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A	75	55	120	nC
Gate-Source Charge[2]	Q_{gs}		12	5.2	19	
Gate-Drain Charge[2]	Q_{gd}		35	27	70	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 19 Ω, $I_D \simeq$ 13 A, V_{GEN} = 10 V, R_G = 2.4 Ω	13		35	ns
Rise Time[2]	t_r		26		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		55		150	
Fall Time[2]	t_f		17		70	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				13	A
Pulsed Current[3]	I_{SM}				50	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V		0.80	1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	400		1000	ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

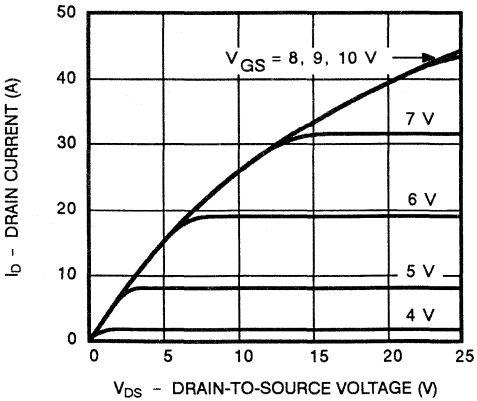


Figure 2. Transfer Characteristics

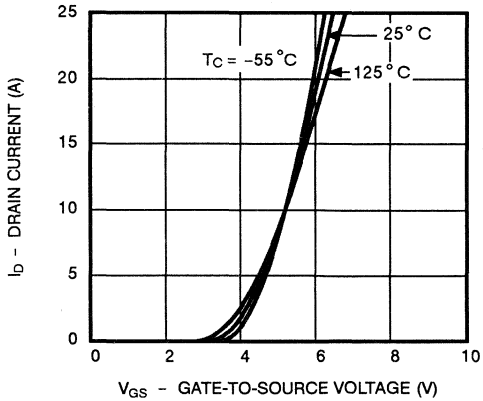


Figure 3. Transconductance

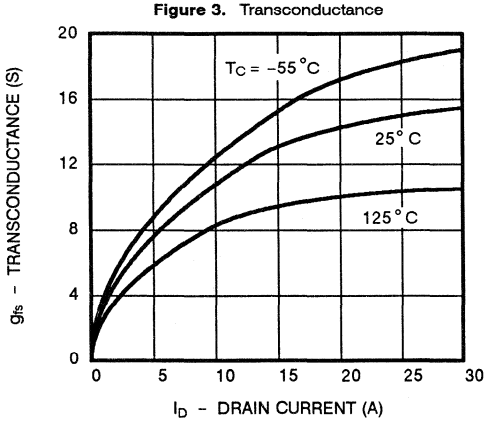


Figure 4. On-Resistance

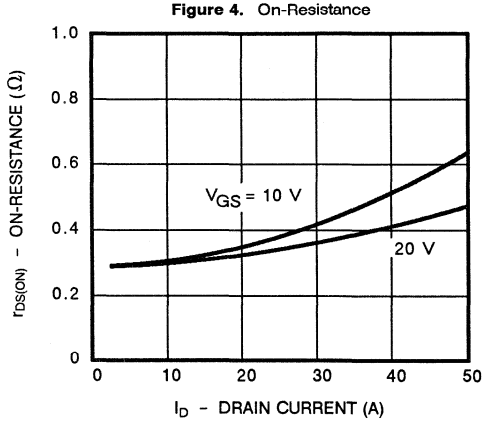


Figure 5. Capacitance

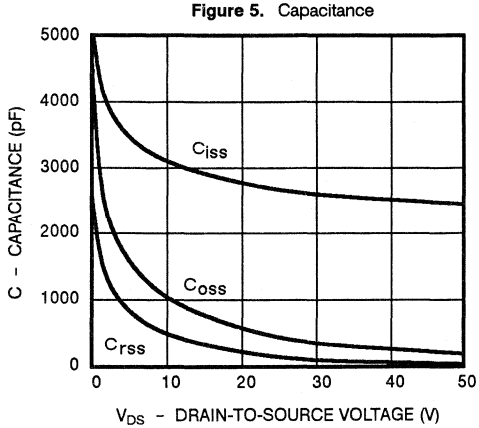
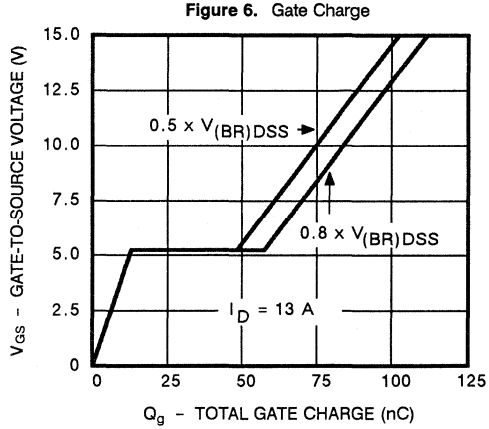


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

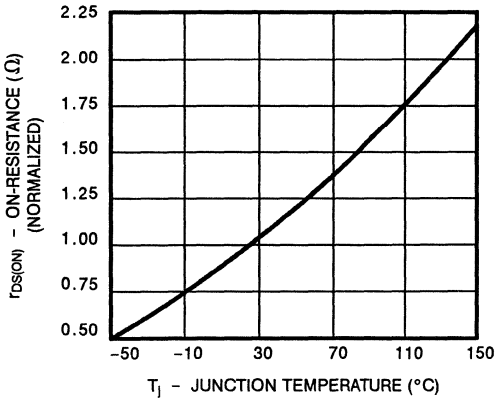
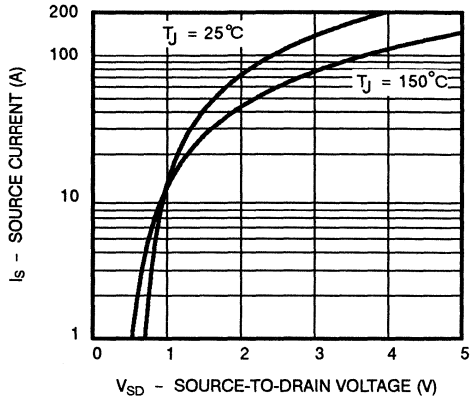


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

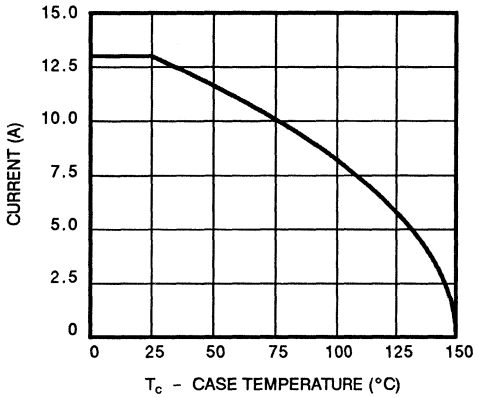
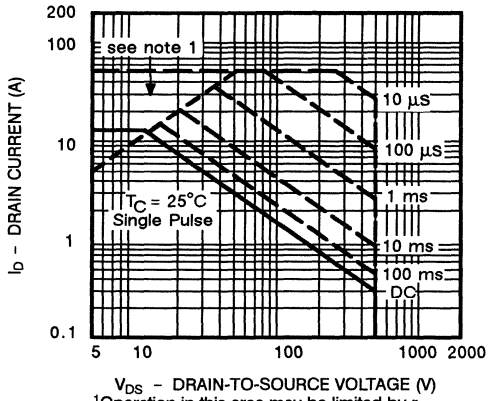
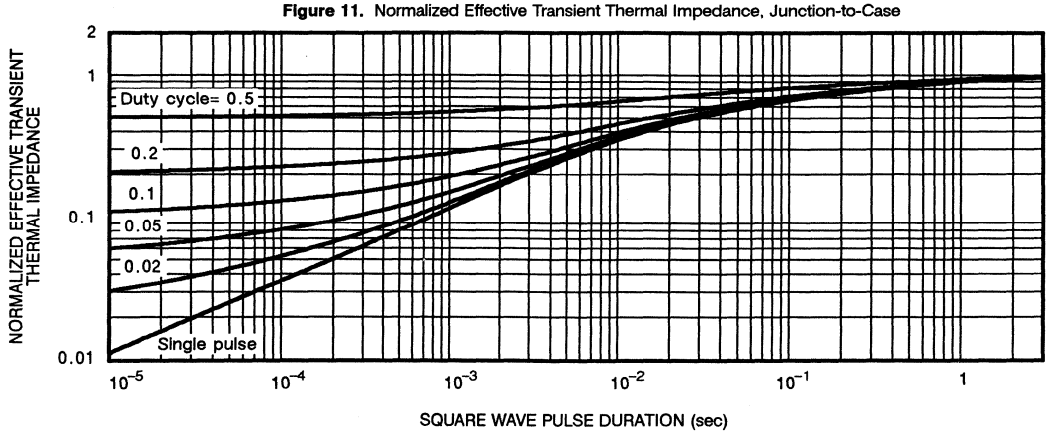


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

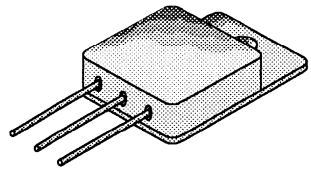


Siliconix incorporated

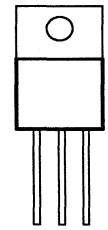
2N7079

P-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	0.210	-17

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	17	A
	T_C = 100°C		10.8	
Pulsed Drain Current		I_{DM}	68	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		17		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 8 A	0.14		0.21	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C	0.22		0.32	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 10.8 A	5.5	5.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		300			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 17 A	47	38	60	nC
Gate-Source Charge[2]	Q_{gs}		10	6.0	18	
Gate-Drain Charge[2]	Q_{gd}		27	18	36	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 2.7 Ω, $I_D \simeq$ 17 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		25		80	
Fall Time[2]	t_f		15		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				17	A
Pulsed Current[3]	I_{SM}				68	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

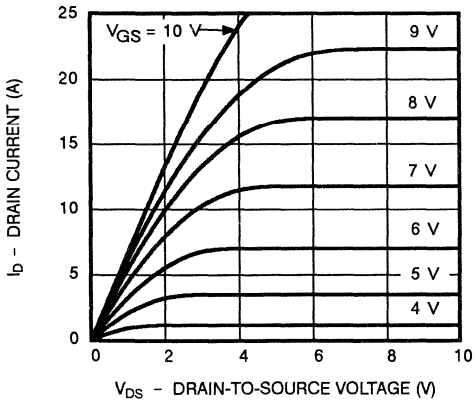


Figure 2. Transfer Characteristics

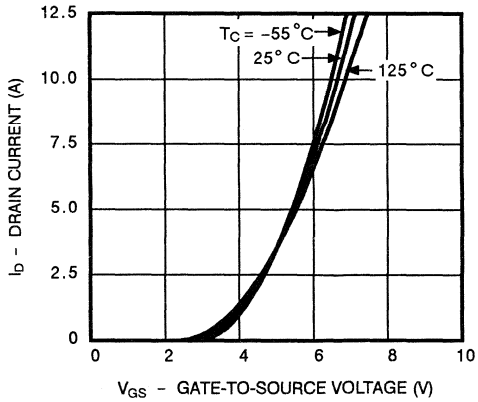


Figure 3. Transconductance

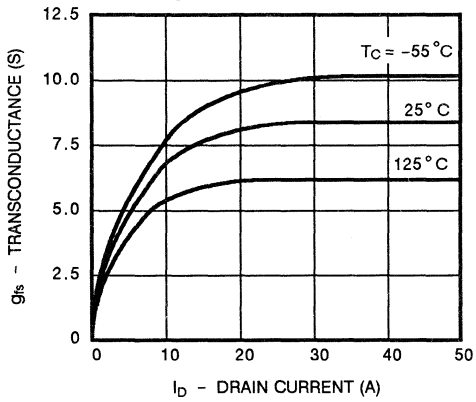


Figure 4. On-Resistance

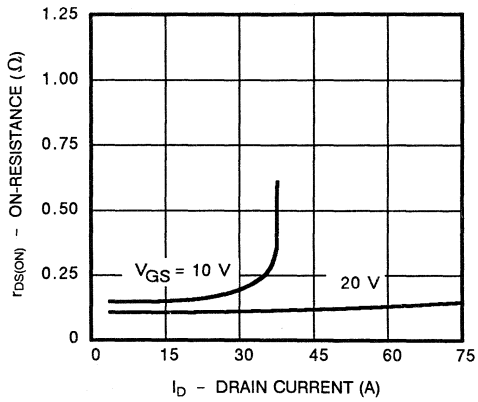


Figure 5. Capacitance

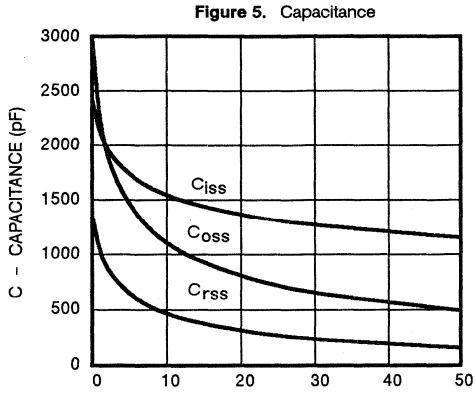
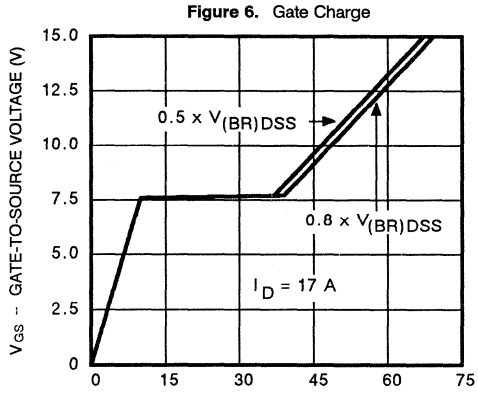


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

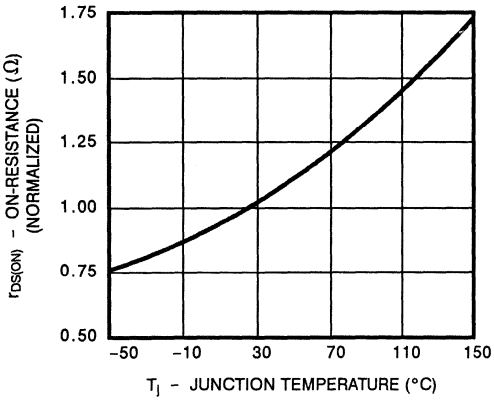
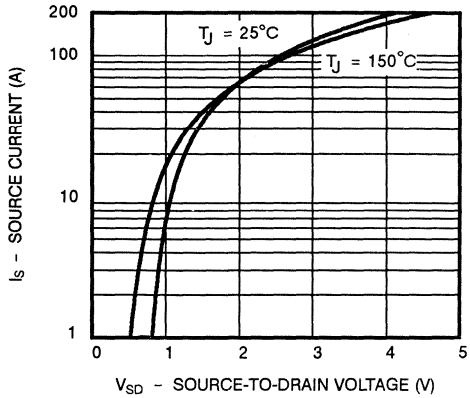


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

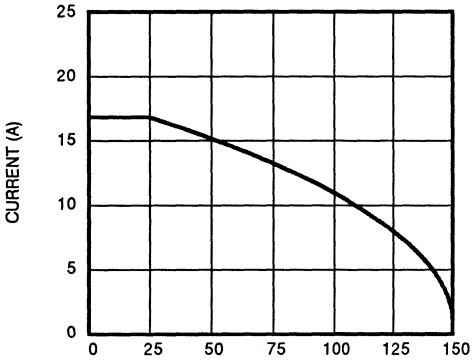
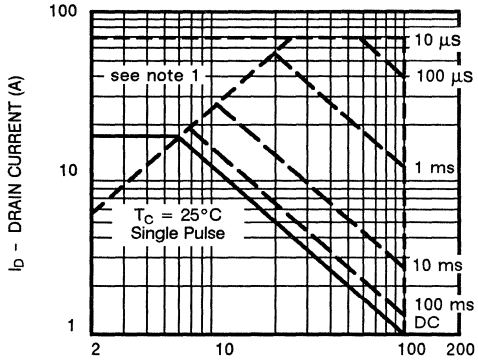
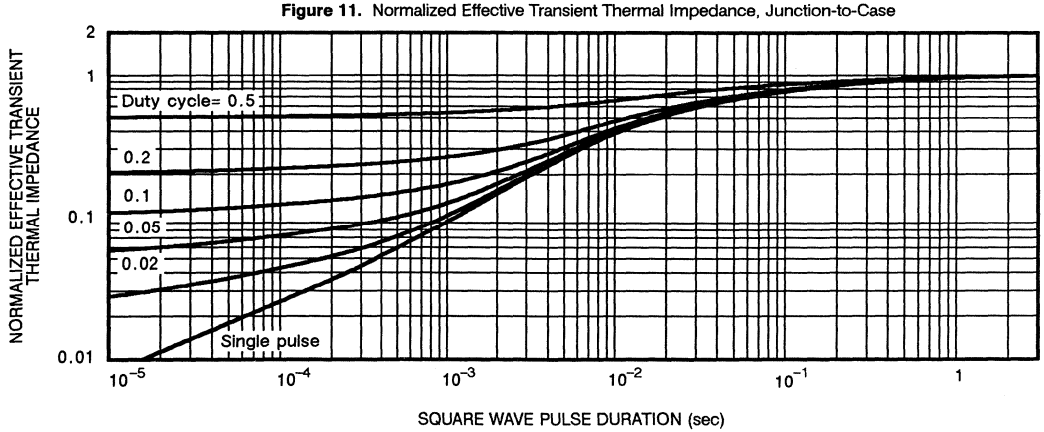


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

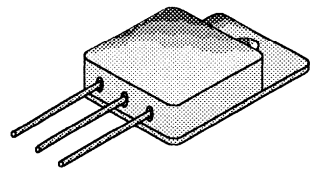


Siliconix incorporated

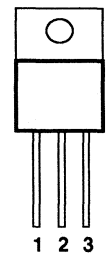
2N7080

P-Channel Enhancement Mode Transistor

TO-254AA
Hermetic Package



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.500	-9.5

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	9.5	A
	T_C = 100°C		6.1	
Pulsed Drain Current		I_{DM}	38	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.25	K/W
Junction-to-Ambient	R_{thJA}		50	
Case-to-Sink	R_{thCS}	0.2		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		9.5		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 6.1 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 6.1 A, T_J = 125°C	0.5		1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 6.1 A	4.8	4.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		450			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.5 A	55	35	75	nC
Gate-Source Charge[2]	Q_{gs}		9.0	3.0	15	
Gate-Drain Charge[2]	Q_{gd}		30	15	45	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 10.2 Ω, I_D ≃ 9.5 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		25	ns
Rise Time[2]	t_r		30		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		80	
Fall Time[2]	t_f		16		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				9.5	A
Pulsed Current[3]	I_{SM}				38	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

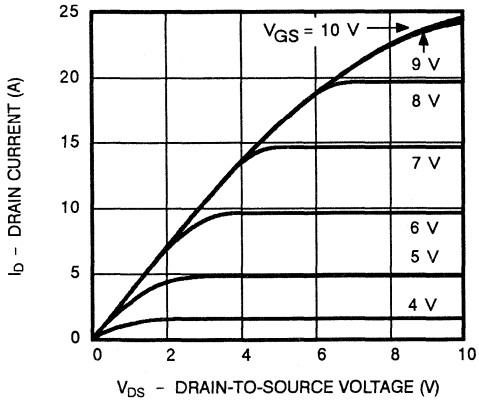


Figure 2. Transfer Characteristics

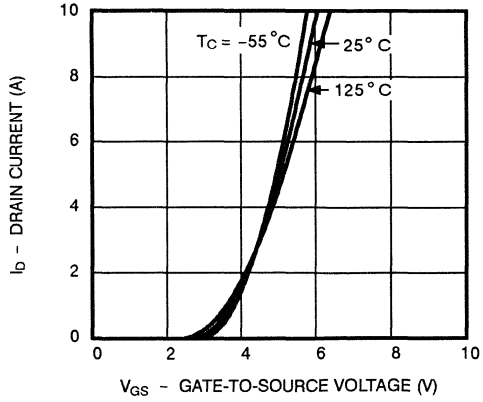


Figure 3. Transconductance

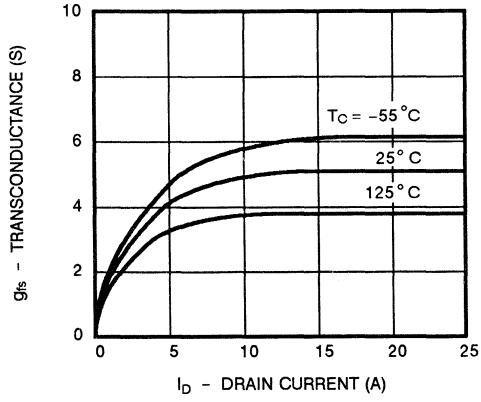


Figure 4. On-Resistance

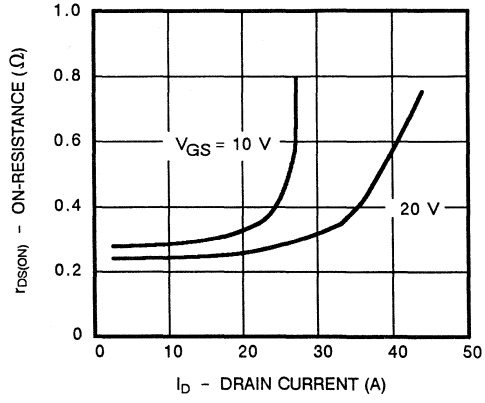


Figure 5. Capacitance

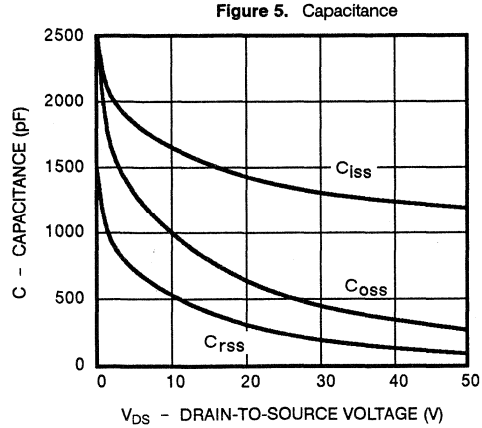
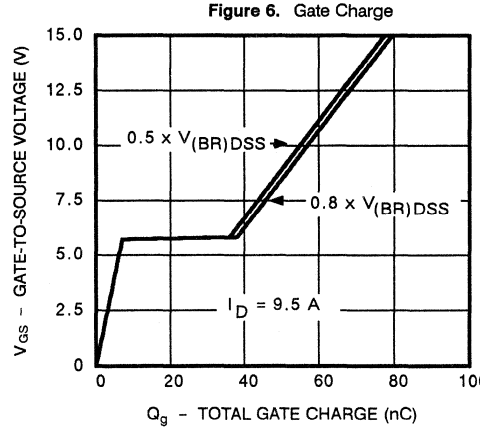


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

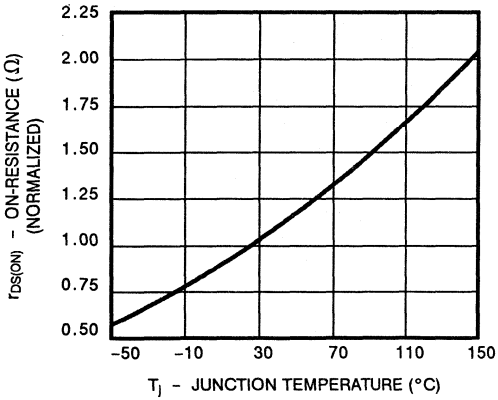
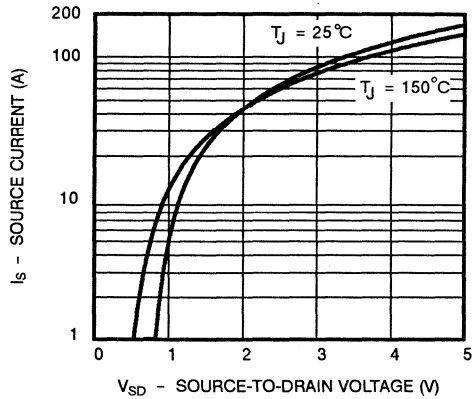


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

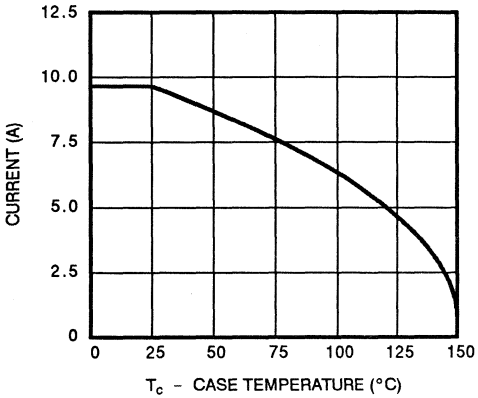
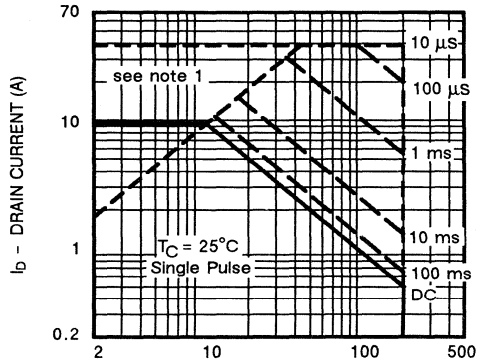
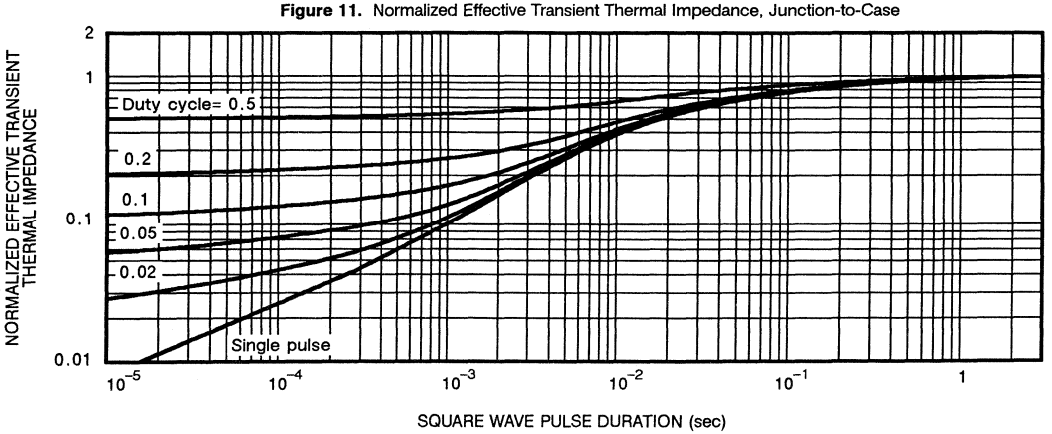


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

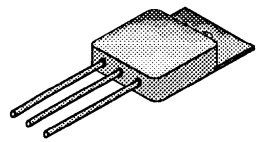


Siliconix incorporated

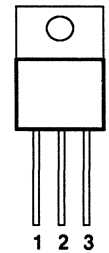
2N7081

N-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.15	12

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		7.7	
Pulsed Drain Current[1]		I_{DM}	48	
Power Dissipation	T_C = 25°C	P_D	45	W
	T_C = 100°C		18	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.8	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		12		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7.7 A	0.12		0.15	Ω
		V_{GS} = 10 V, I_D = 7.7 A, T_J = 125°C	0.22		0.27	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7.7 A	5.0	4.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	600			pF
Output Capacitance	C_{oss}		190			
Reverse Transfer Capacitance	C_{rss}		35			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A	17	12	30	nC
Gate-Source Charge[2]	Q_{gs}		6	2.5	9.0	
Gate-Drain Charge[2]	Q_{gd}		9	5.0	20	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 4.1 Ω, $I_D \simeq$ 12 A, V_{GEN} = 10 V, R_G = 7.5 Ω	7		30	ns
Rise Time[2]	t_r		45		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		30		60	
Fall Time[2]	t_f		10		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				12	A
Pulsed Current[3]	I_{SM}				48	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	100		300	ns
Reverse Recovery Charge	Q_{rr}		0.7			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

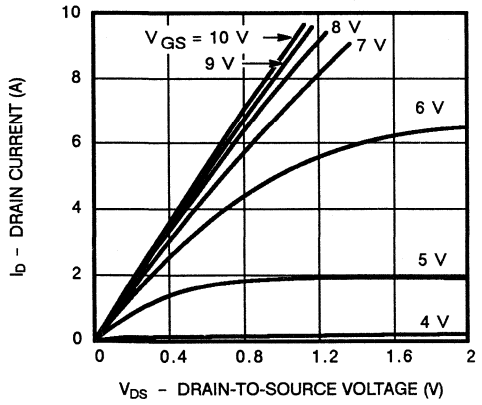


Figure 2. Transfer Characteristics

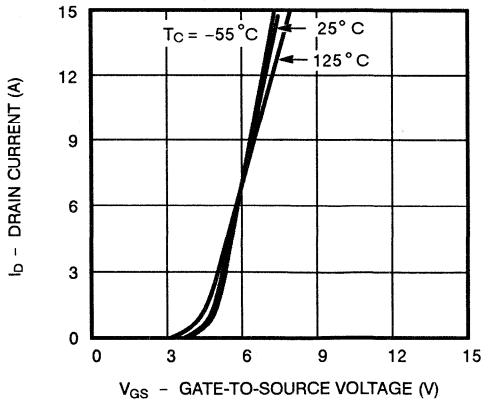


Figure 3. Transconductance

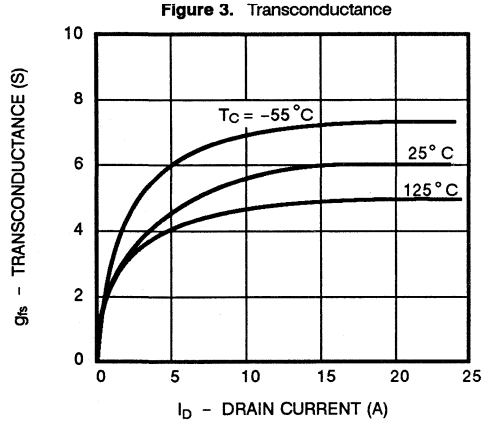


Figure 4. On-Resistance

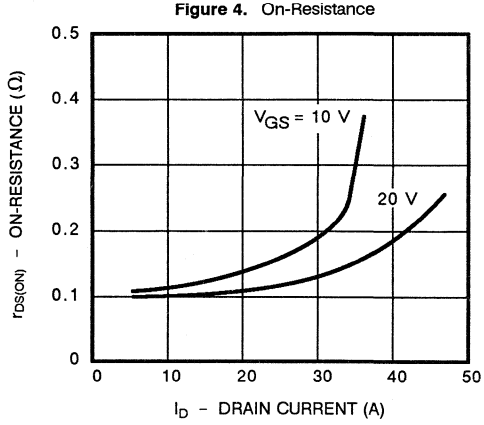


Figure 5. Capacitance

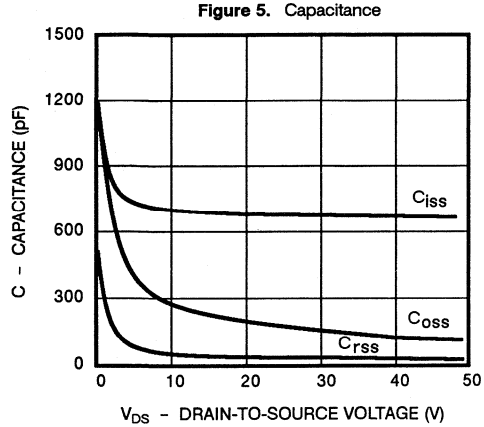
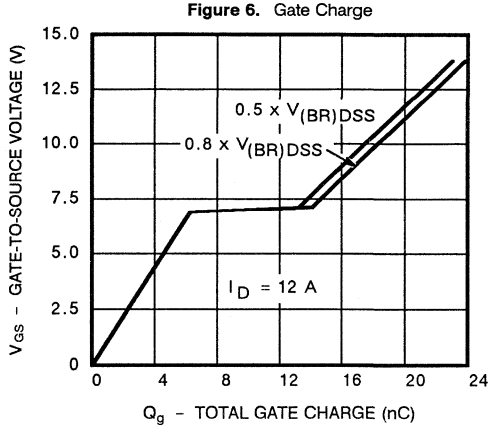


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

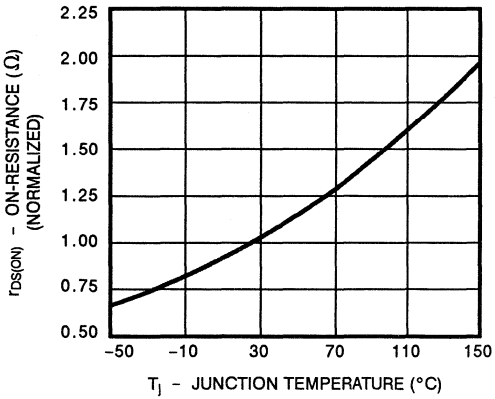
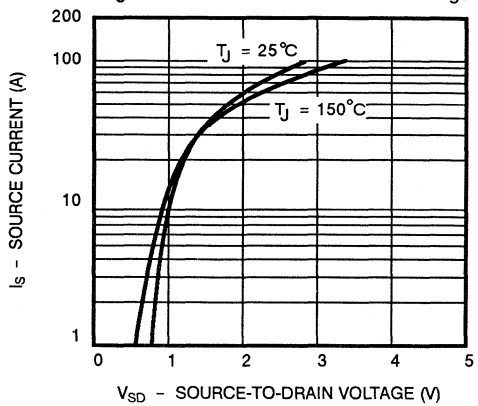


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

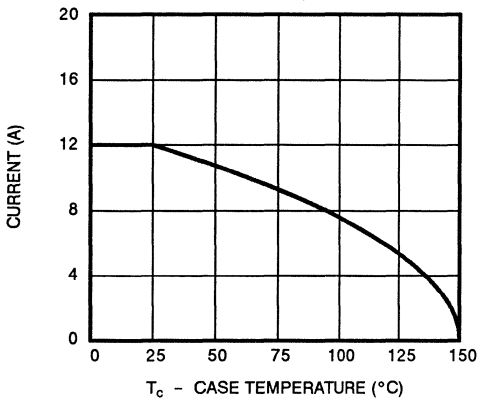
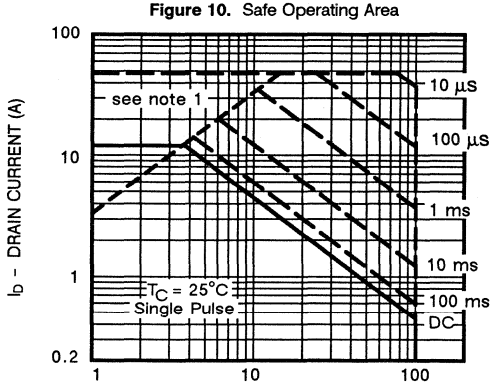
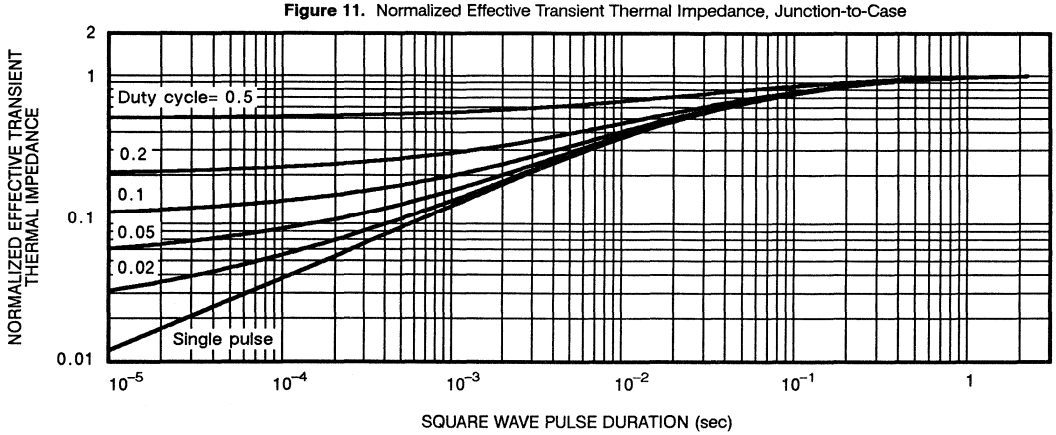


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

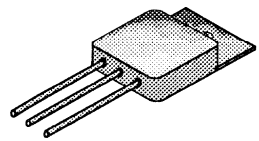


Siliconix incorporated

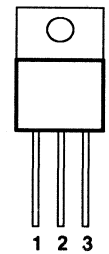
2N7082

N-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	0.30	9.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	9.0	A
	T_C = 100°C		5.5	
Pulsed Drain Current[1]		I_{DM}	36	
Power Dissipation	T_C = 25°C	P_D	50	W
	T_C = 100°C		20	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.5	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		9.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5.5 A	0.25		0.30	Ω
		V_{GS} = 10 V, I_D = 5.5 A, T_J = 125°C	0.50		0.60	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5.5 A	3.8	3.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	780			pF
Output Capacitance	C_{oss}		220			
Reverse Transfer Capacitance	C_{rss}		70			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9 A	23	14	39	nC
Gate-Source Charge[2]	Q_{gs}		5	2.2	7.0	
Gate-Drain Charge[2]	Q_{gd}		13	8.0	20	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 11 Ω, $I_D \simeq$ 9 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				9.0	A
Pulsed Current[3]	I_{SM}				36	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150		500	ns
Reverse Recovery Charge	Q_{rr}		0.8			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

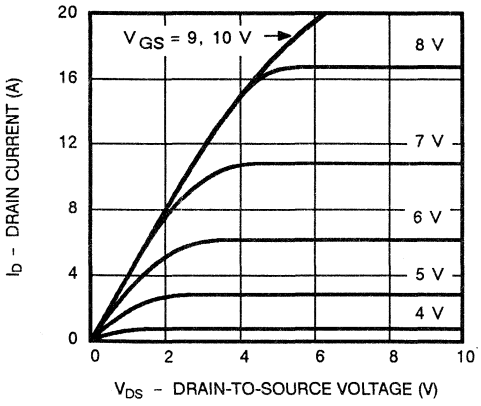


Figure 2. Transfer Characteristics

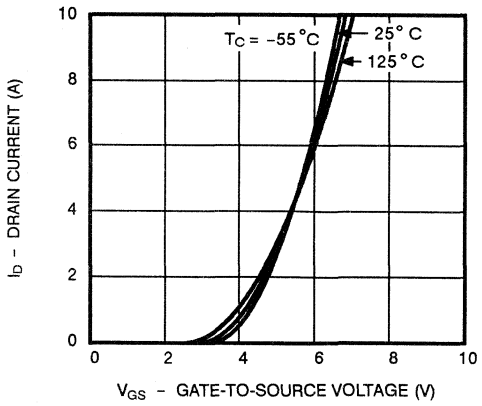


Figure 3. Transconductance

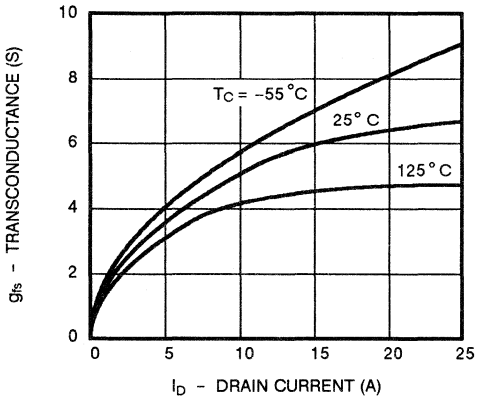


Figure 4. On-Resistance

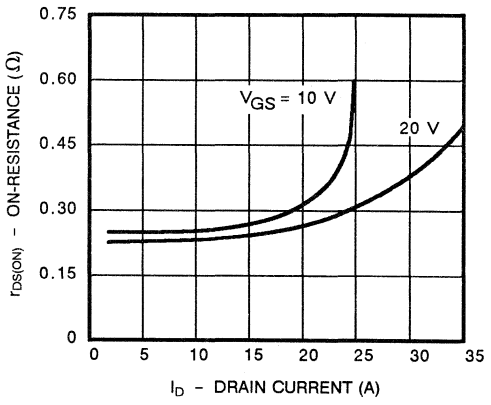


Figure 5. Capacitance

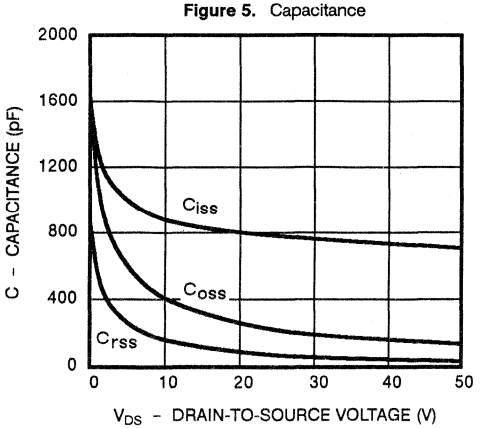
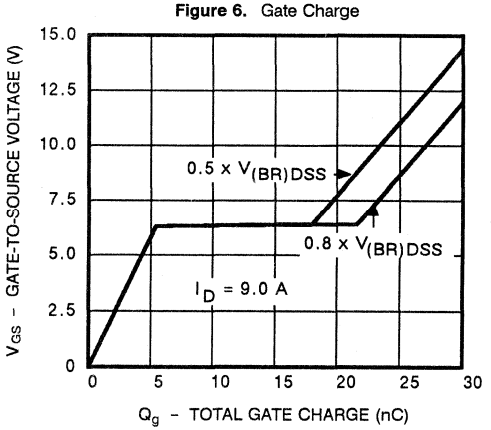


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

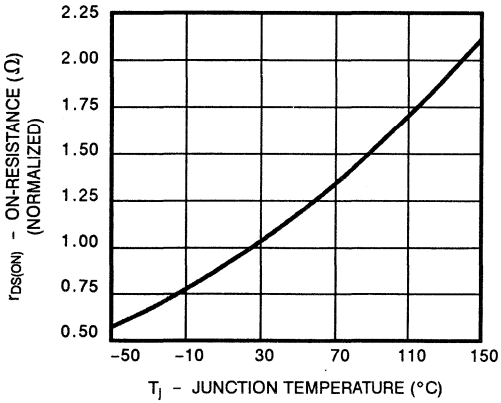
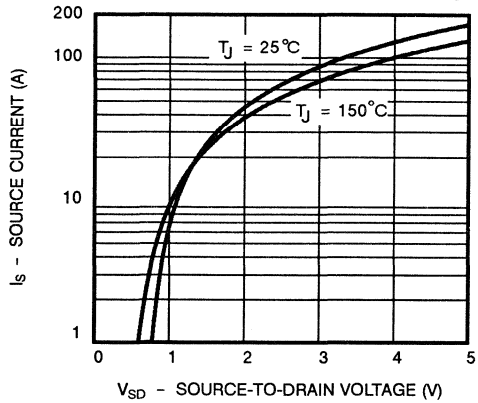


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

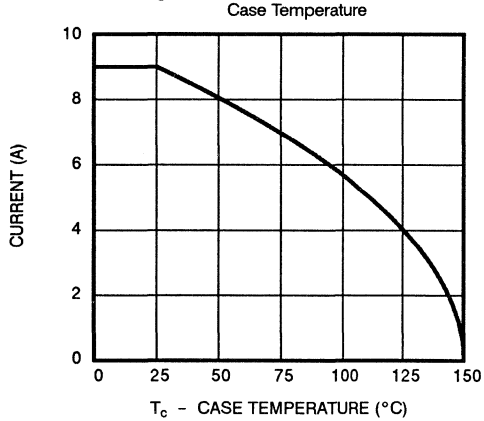


Figure 10. Safe Operating Area

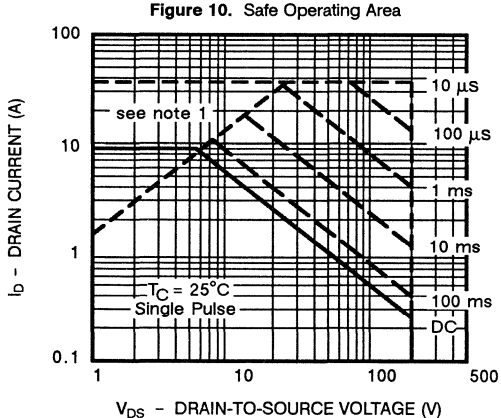
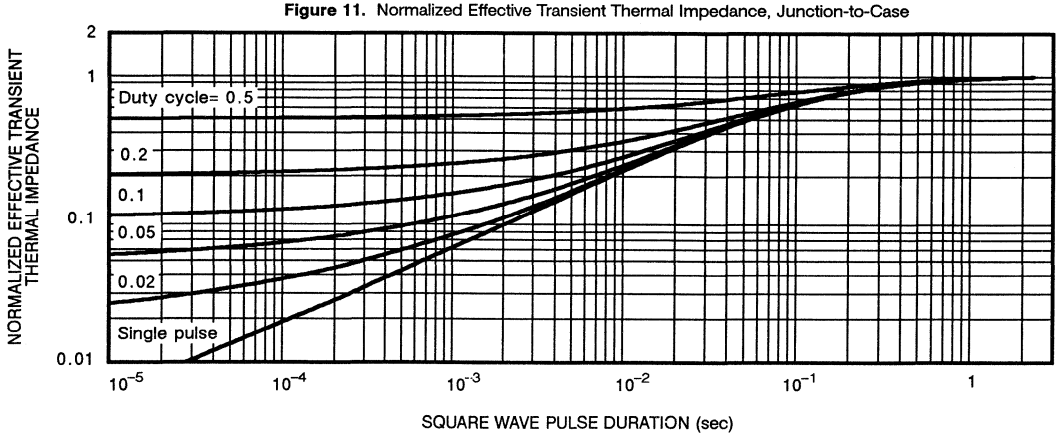


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

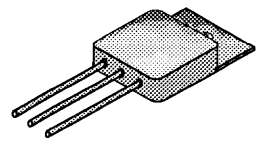


Siliconix incorporated

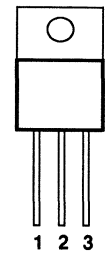
2N7085

N-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.075	20

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		12	
Pulsed Drain Current[1]		I_{DM}	80	
Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		23	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.1	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12 A	0.06		0.075	Ω
		V_{GS} = 10 V, I_D = 12 A, T_J = 125°C	0.11		0.14	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 12 A	8.0	5.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1400			pF
Output Capacitance	C_{oss}		480			
Reverse Transfer Capacitance	C_{rss}		110			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	35	15	50	nC
Gate-Source Charge[2]	Q_{gs}		10	6.0	20	
Gate-Drain Charge[2]	Q_{gd}		15	8.0	25	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 2.5 Ω, I_D ≃ 20 A, V_{GEN} = 10 V, R_G = 4.7 Ω	13		30	ns
Rise Time[2]	t_r		85		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		80	
Fall Time[2]	t_f		75		95	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				80	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150		400	ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

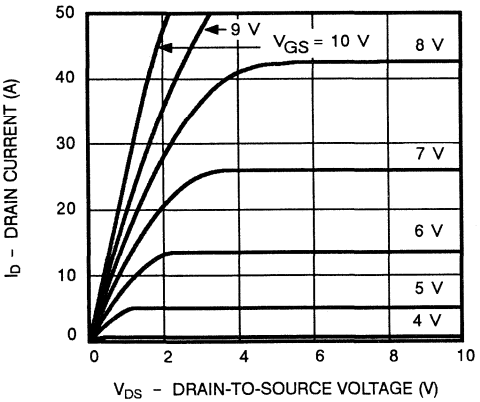


Figure 2. Transfer Characteristics

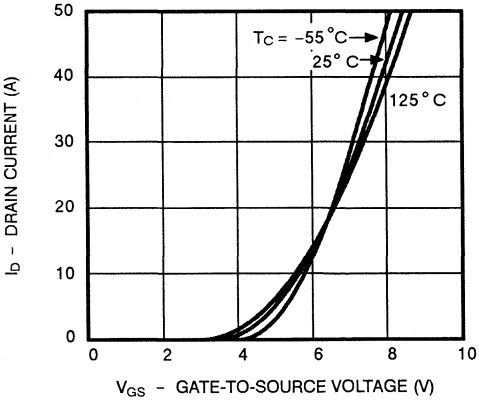


Figure 3. Transconductance

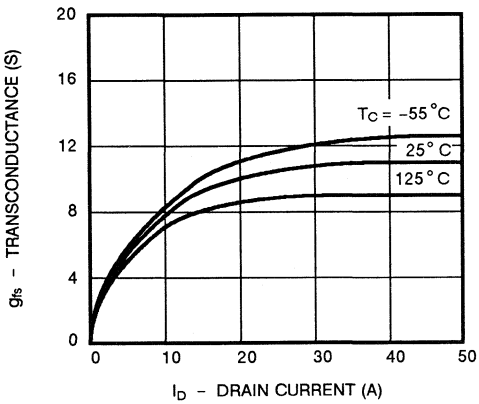


Figure 4. On-Resistance

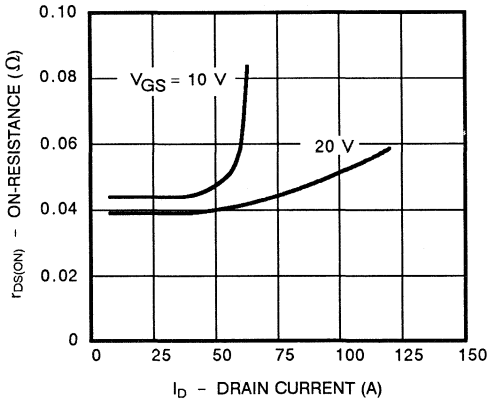


Figure 5. Capacitance

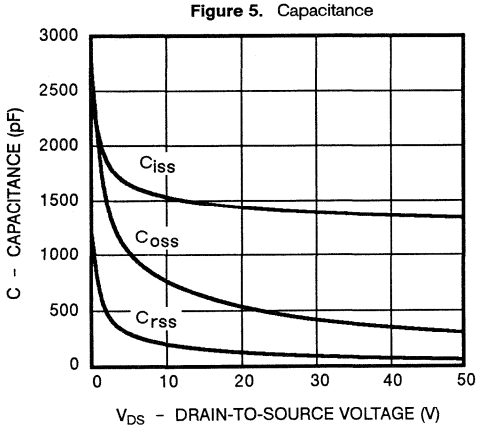
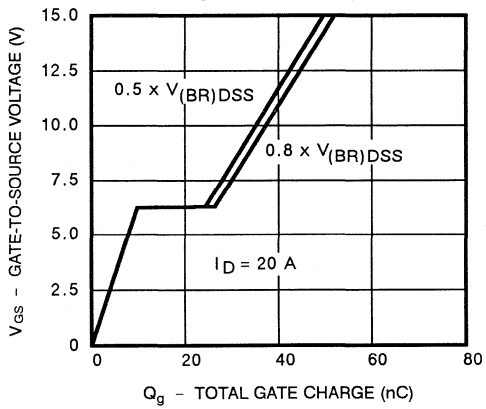


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

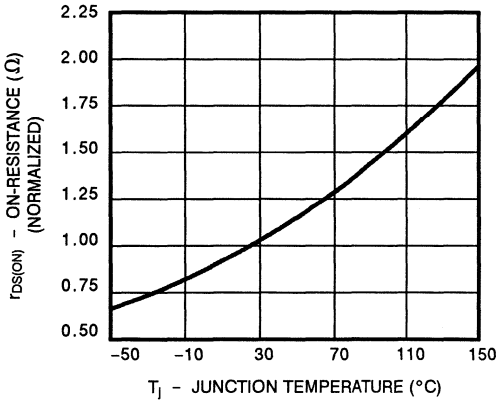
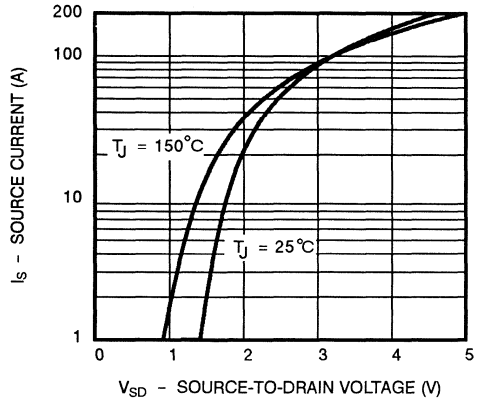


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

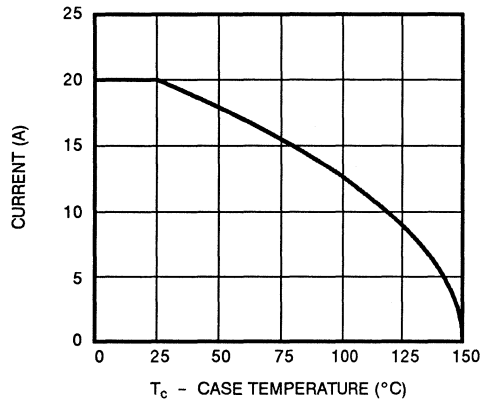
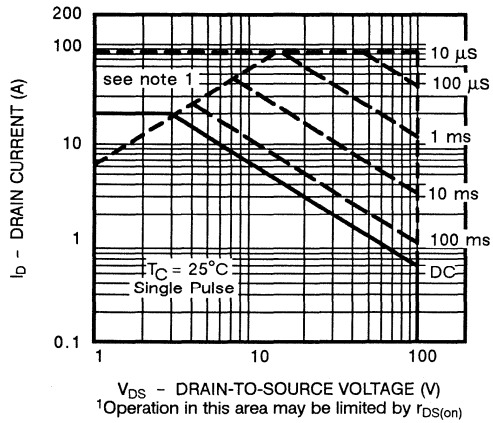
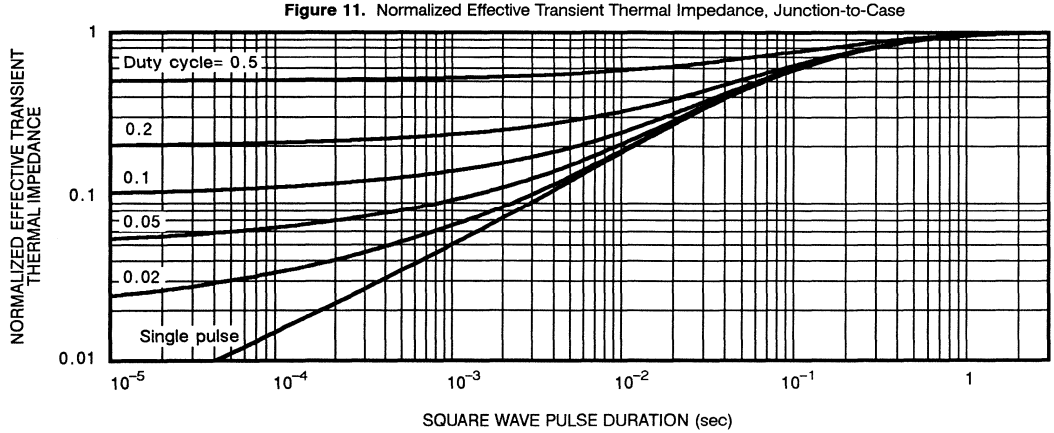


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

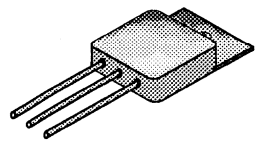


Siliconix incorporated

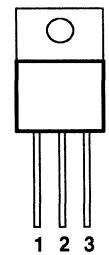
2N7086

N-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	0.16	14

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		8.5	
Pulsed Drain Current[1]		I_{DM}	56	
Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		23	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($1/16$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.1	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		14		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 8.5 A	0.14		0.16	Ω
		V_{GS} = 10 V, I_D = 8.5 A, T_J = 125°C	0.25		0.30	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 8.5 A		5.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1550			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		220			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A	44	30	77	nC
Gate-Source Charge[2]	Q_{gs}		10	4.6	15	
Gate-Drain Charge[2]	Q_{gd}		26	13	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 7.1 Ω, $I_D \simeq$ 14 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		60		100	
Turn-Off Delay Time[2]	$t_{d(off)}$		30		80	
Fall Time[2]	t_f		40		95	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				14	A
Pulsed Current[3]	I_{SM}				56	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150		650	ns
Reverse Recovery Charge	Q_{rr}		0.5			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

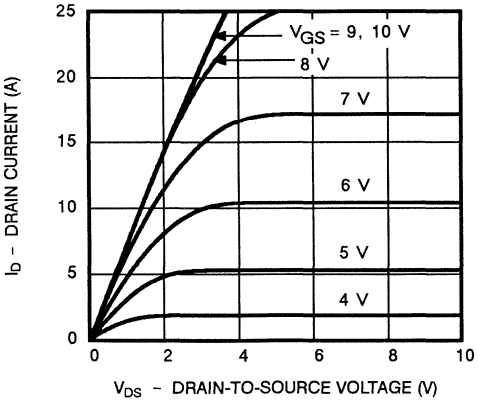


Figure 2. Transfer Characteristics

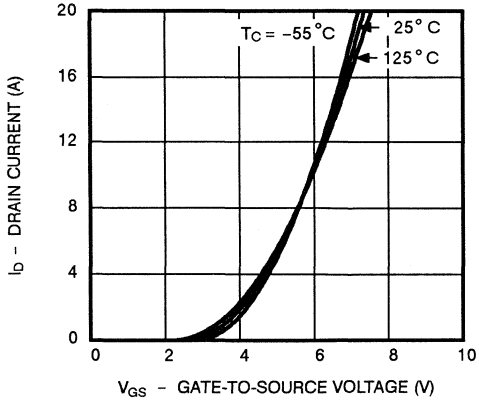


Figure 3. Transconductance

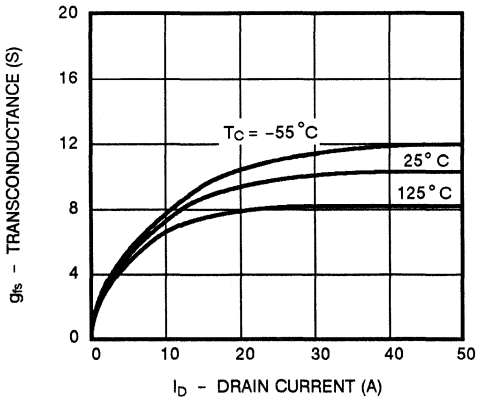


Figure 4. On-Resistance

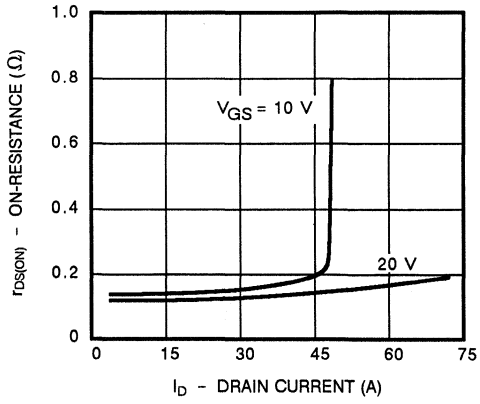


Figure 5. Capacitance

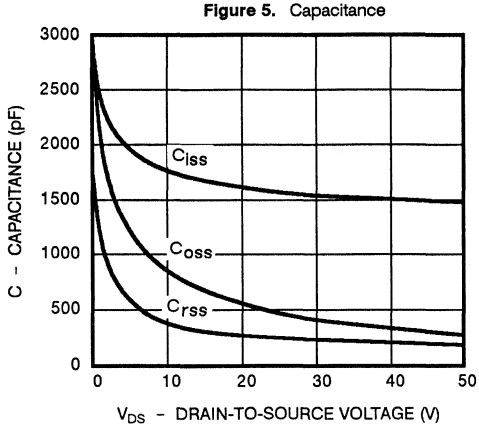
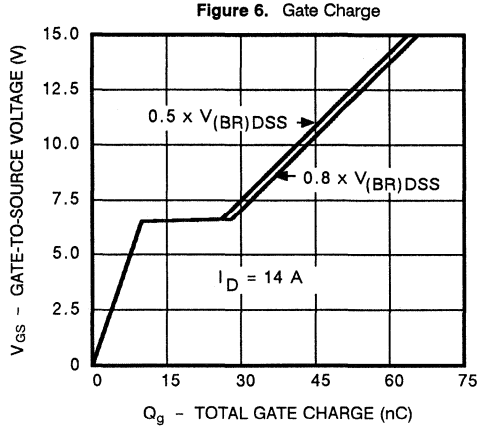


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

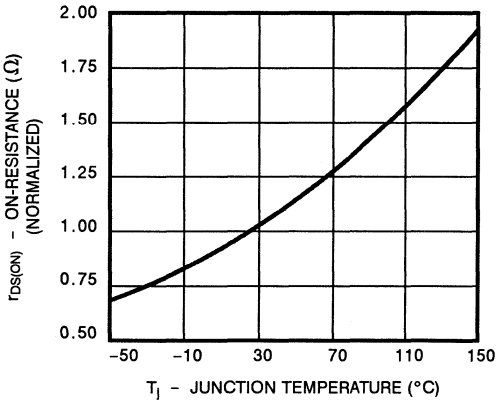
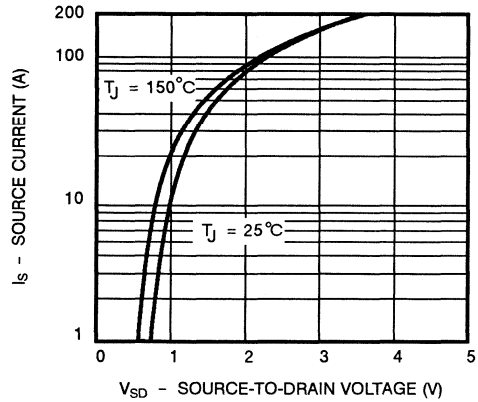


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

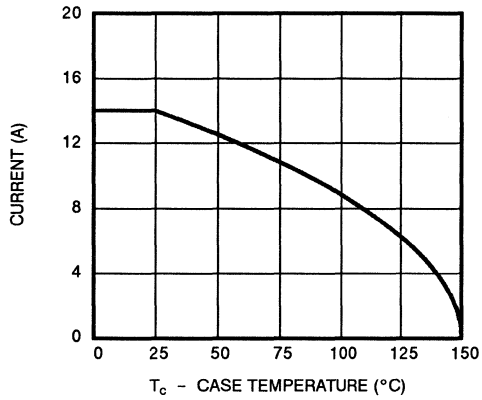
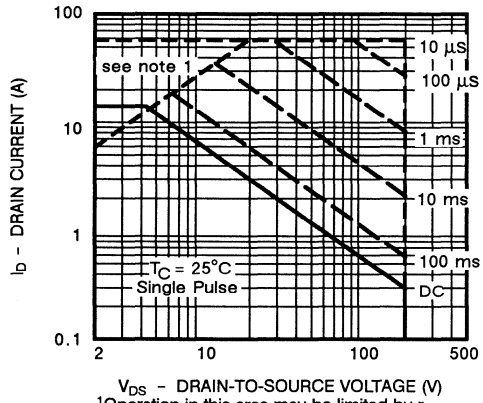
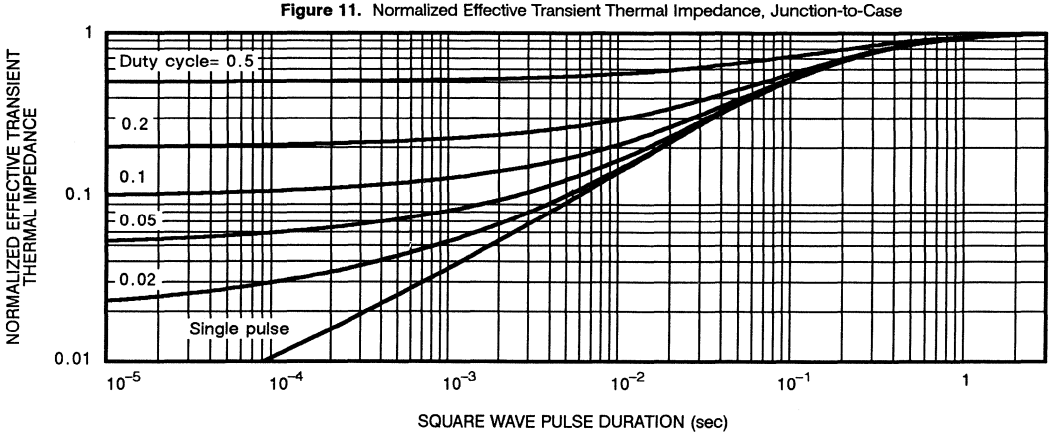


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

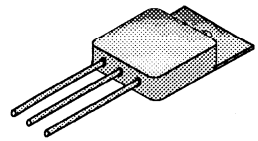


Siliconix incorporated

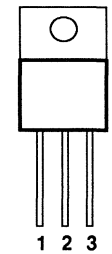
2N7089

P-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-100	0.30	-10.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	10.0	A
	T_C = 100°C		6.7	
Pulsed Drain Current[2]		I_{DM}	40	
Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		24	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		10.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 6.7 A	0.25		0.30	Ω
		V_{GS} = 10 V, I_D = 6.7 A, T_J = 125°C	0.40		0.53	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 6.7A	3.0	2.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	625			pF
Output Capacitance	C_{oss}		280			
Reverse Transfer Capacitance	C_{rss}		105			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A	24	13	40	nC
Gate-Source Charge[2]	Q_{gs}		3.4	1.5	6.0	
Gate-Drain Charge[2]	Q_{gd}		13.5	6.7	20	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 5.0 Ω, $I_D \simeq$ 10 A, V_{GEN} = 10 V, R_G = 7.5 Ω	9		60	ns
Rise Time[2]	t_r		50		140	
Turn-Off Delay Time[2]	$t_{d(off)}$		60		140	
Fall Time[2]	t_f		38		140	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				10.0	A
Pulsed Current[3]	I_{SM}				40	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	110		250	ns
Reverse Recovery Charge	Q_{rr}		0.4			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

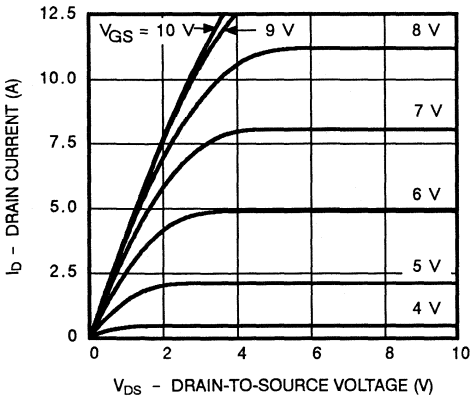


Figure 2. Transfer Characteristics

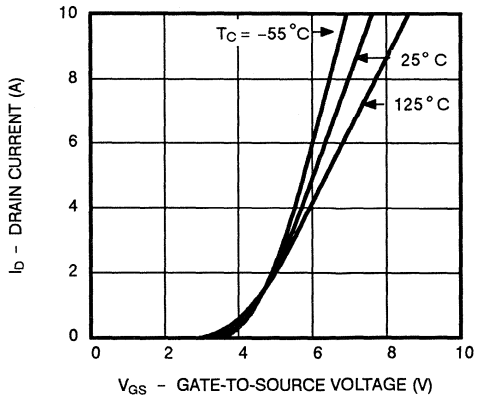


Figure 3. Transconductance

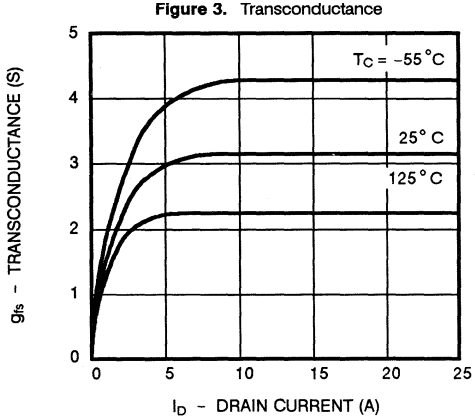


Figure 4. On-Resistance

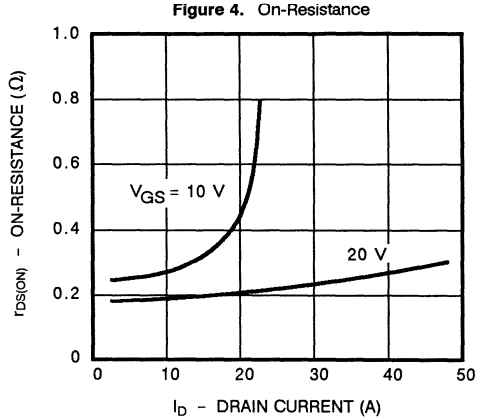


Figure 5. Capacitance

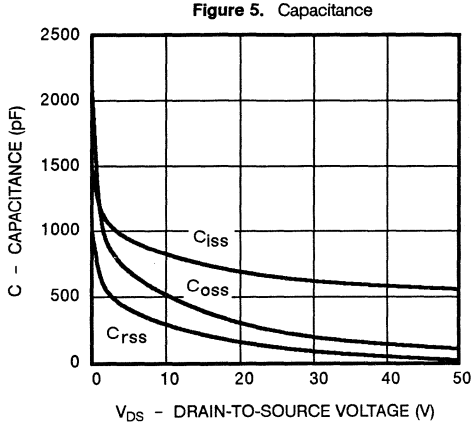
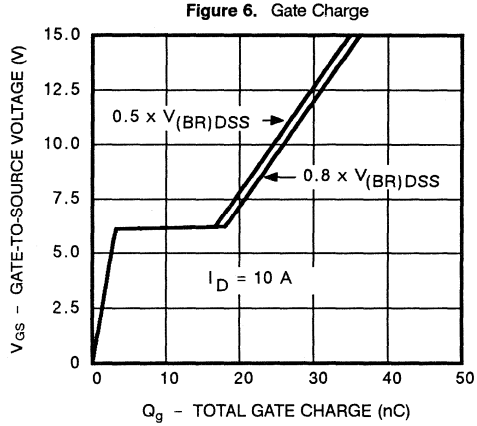


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

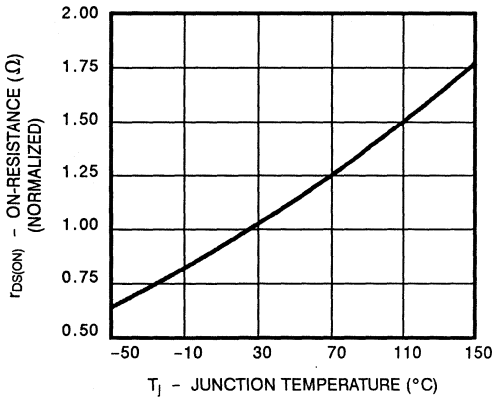
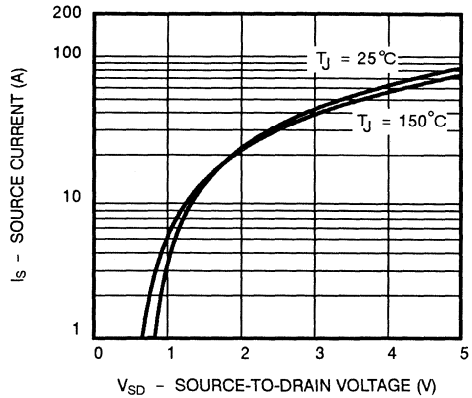


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

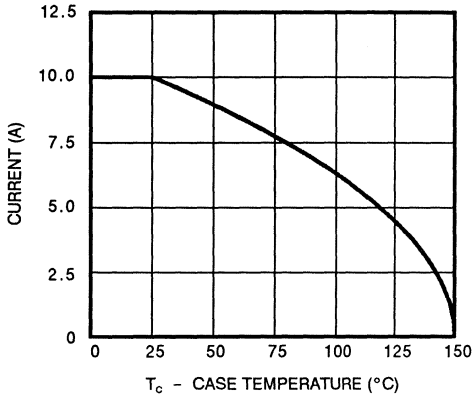
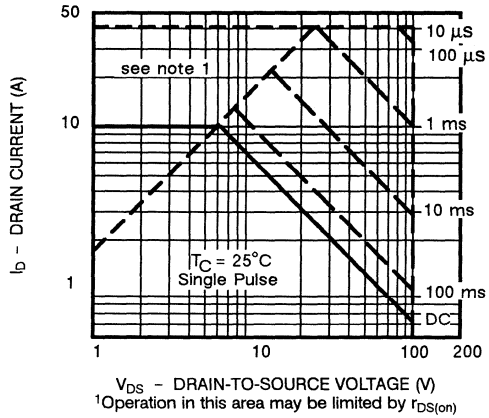
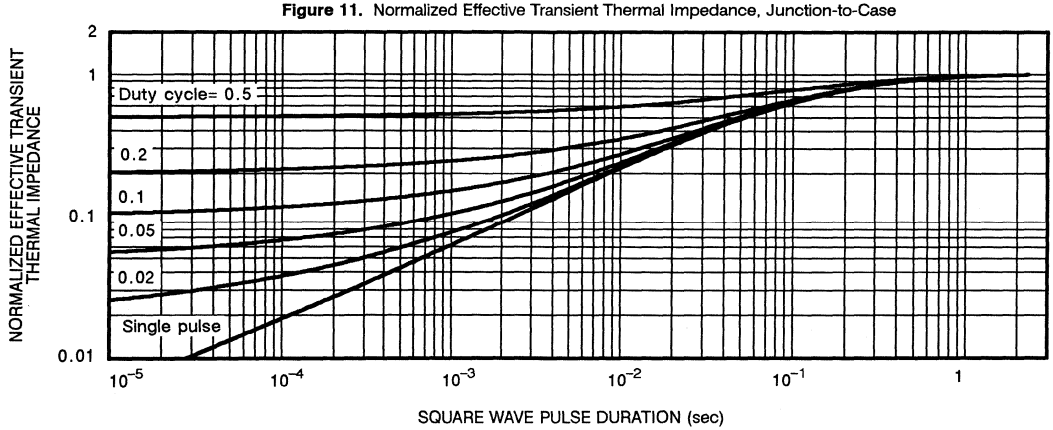


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

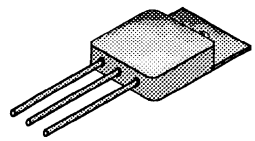


Siliconix incorporated

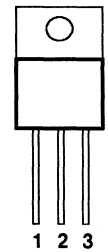
2N7090

P-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.80	-5.7

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	5.7	A
	T_C = 100°C		3.6	
Pulsed Drain Current[2]		I_{DM}	23	
Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		25	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		5.7		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 3.6 A	0.5		0.80	Ω
		V_{GS} = 10 V, I_D = 3.6 A, T_J = 125°C	1.0		1.6	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 3.6 A	2.7	2.2		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	510			pF
Output Capacitance	C_{oss}		180			
Reverse Transfer Capacitance	C_{rss}		75			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.7 A	13	27	35	nC
Gate-Source Charge[2]	Q_{gs}		1.5	3.4	6.0	
Gate-Drain Charge[2]	Q_{gd}		7	15	25	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 17 Ω, I_D ≃ 5.7 A, V_{GEN} = 10 V, R_G = 7.5 Ω	9.0		50	ns
Rise Time[2]	t_r		33		100	
Turn-Off Delay Time[2]	$t_{d(off)}$		80		100	
Fall Time[2]	t_f		50		80	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				5.7	A
Pulsed Current[3]	I_{SM}				23	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160		400	ns
Reverse Recovery Charge	Q_{rr}		1.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

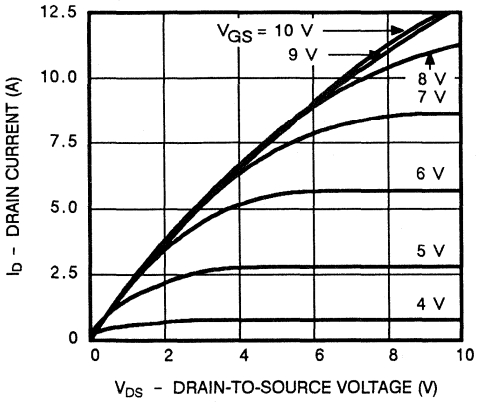


Figure 2. Transfer Characteristics

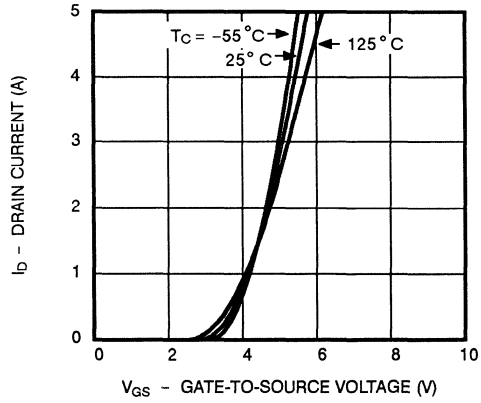


Figure 3. Transconductance

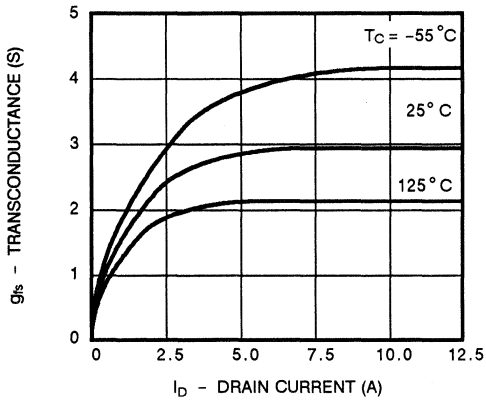


Figure 4. On-Resistance

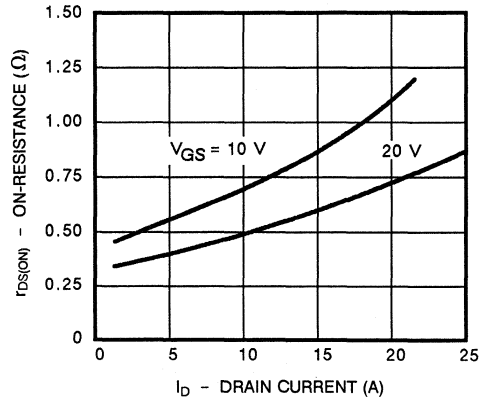


Figure 5. Capacitance

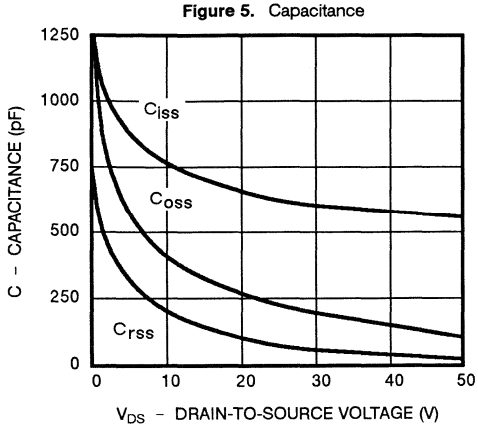
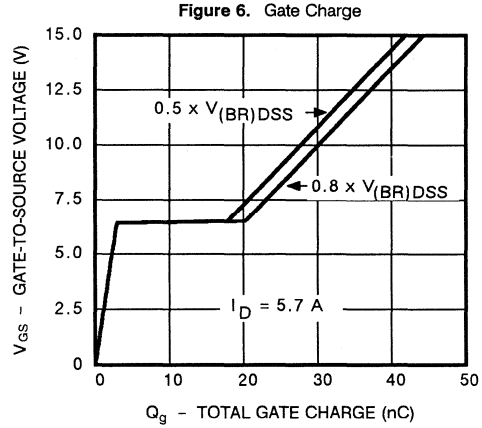


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

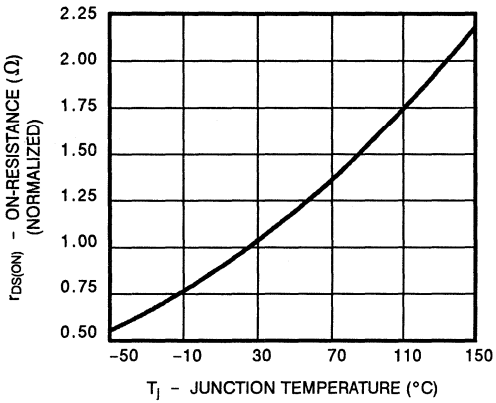
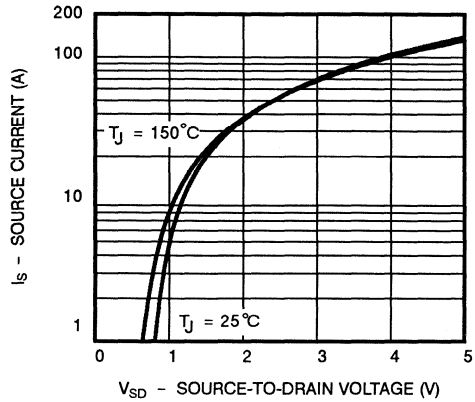


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

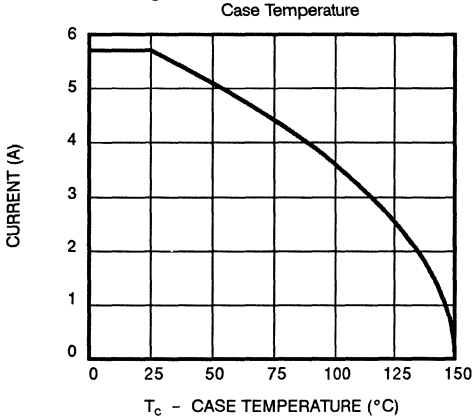
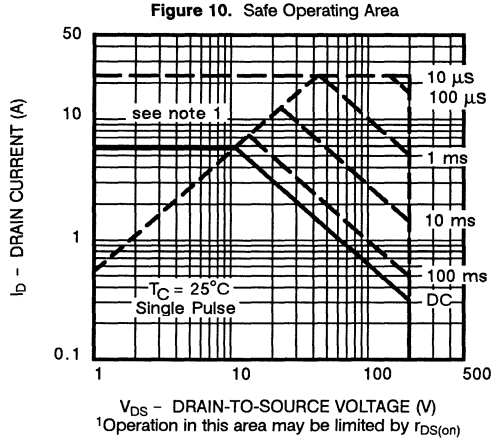
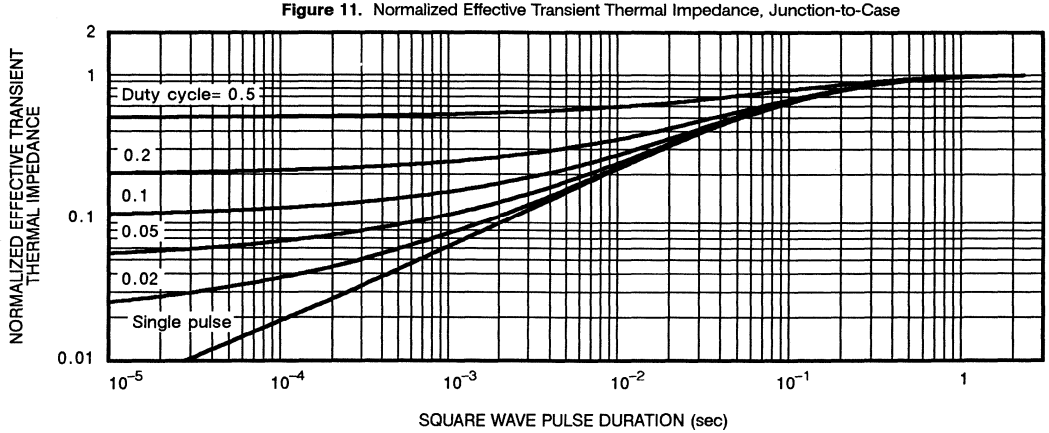


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

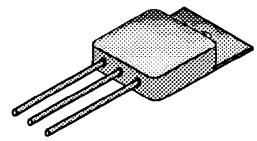


Siliconix incorporated

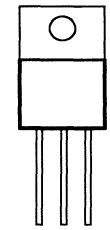
2N7091

P-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
−100	0.20	−14

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		8.7	
Pulsed Drain Current[2]		I_{DM}	56	
Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		27	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.8	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11) .

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		14		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 8.7 A	0.15		0.20	Ω
		V_{GS} = 10 V, I_D = 8.7 A, T_J = 125°C	0.23		0.32	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 8.7 A		5.0		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		310			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A	50	32	62	nC
Gate-Source Charge[2]	Q_{gs}		10	5.0	15	
Gate-Drain Charge[2]	Q_{gd}		27	19	35	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 3.5 Ω, $I_D \simeq$ 14 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		50		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		40		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				14	A
Pulsed Current[3]	I_{SM}				56	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	150			ns
Reverse Recovery Charge	Q_{rr}		0.3			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

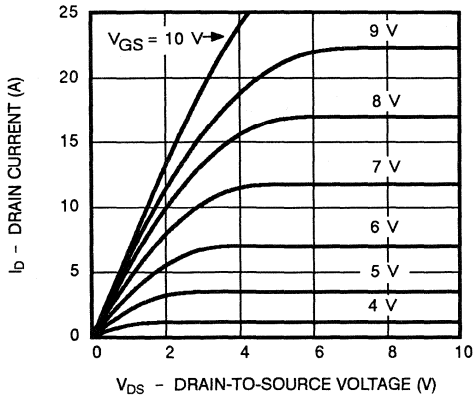


Figure 2. Transfer Characteristics

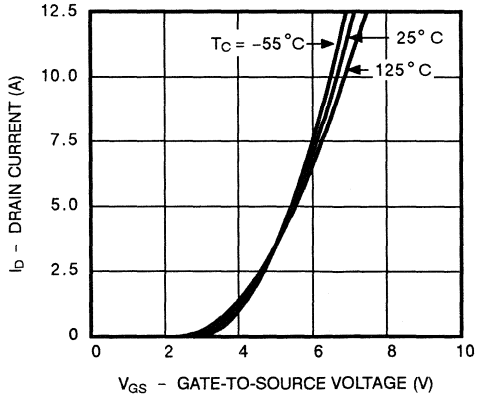


Figure 3. Transconductance

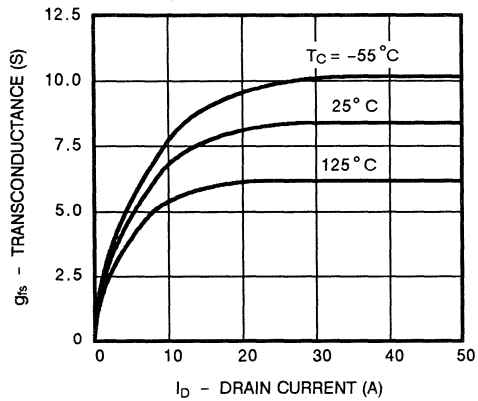


Figure 4. On-Resistance

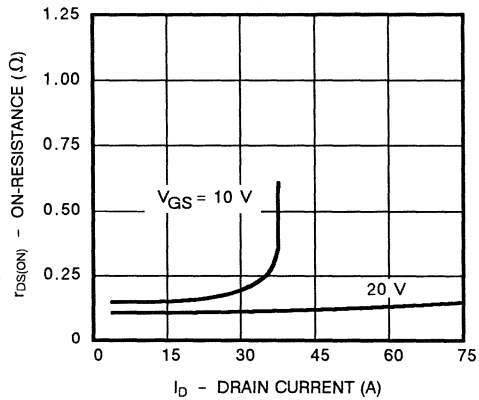


Figure 5. Capacitance

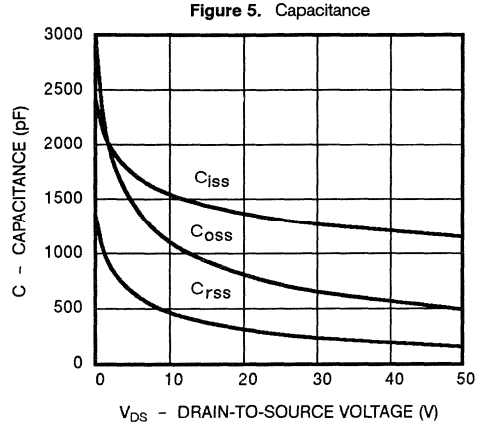
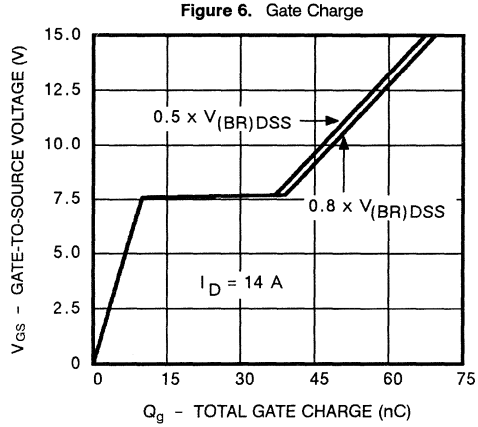


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

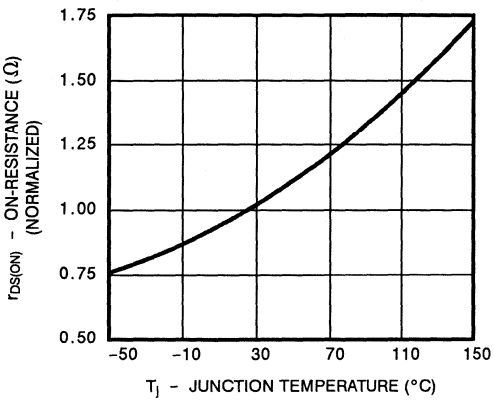
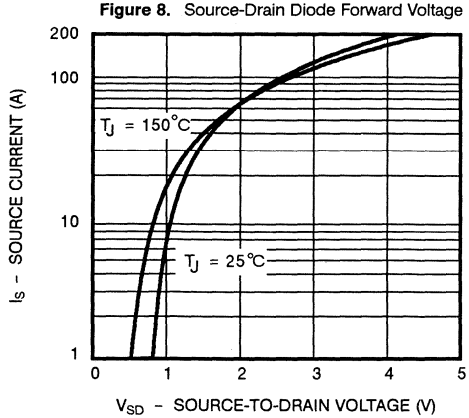


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

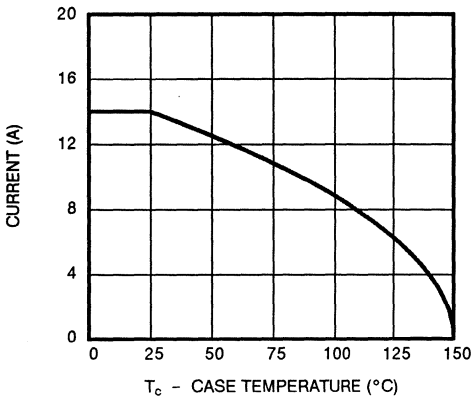
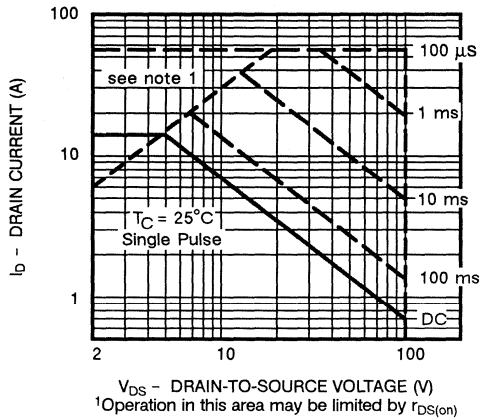
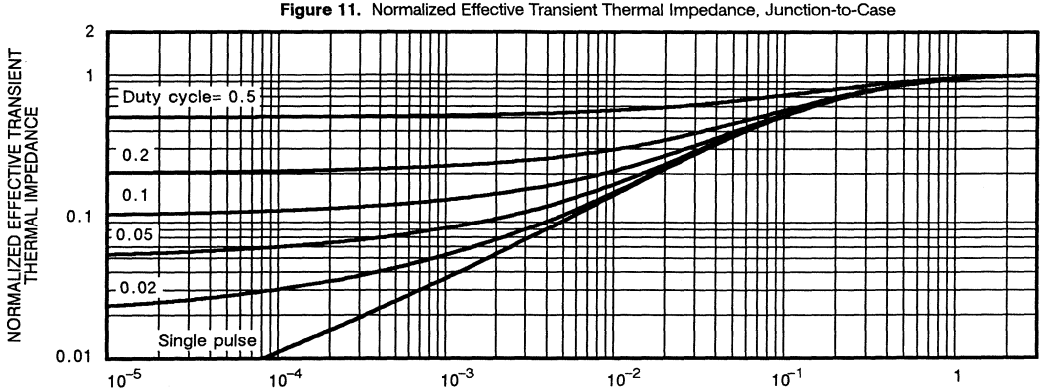


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

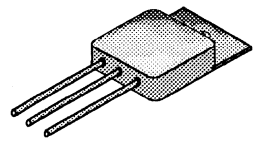


Siliconix incorporated

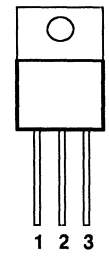
2N7092

P-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-8.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.1	
Pulsed Drain Current[2]		I_{DM}	32	
Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		27	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.8	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		8.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5.1 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 5.1 A, T_J = 125°C	0.56		1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5.1 A	5.0	4.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8 A	55	30	90	nC
Gate-Source Charge[2]	Q_{gs}		10	5.0	15	
Gate-Drain Charge[2]	Q_{gd}		30	10	50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 12.5 Ω, $I_D \simeq$ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		45		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		40		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				8.0	A
Pulsed Current[3]	I_{SM}				32	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

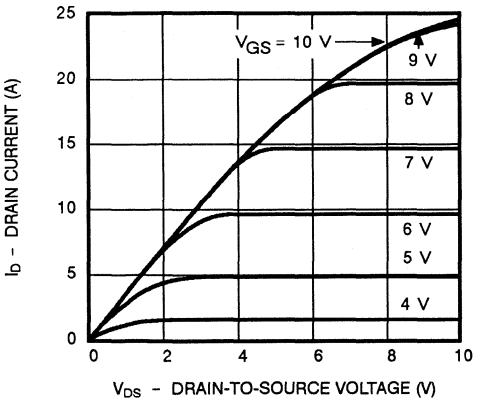


Figure 2. Transfer Characteristics

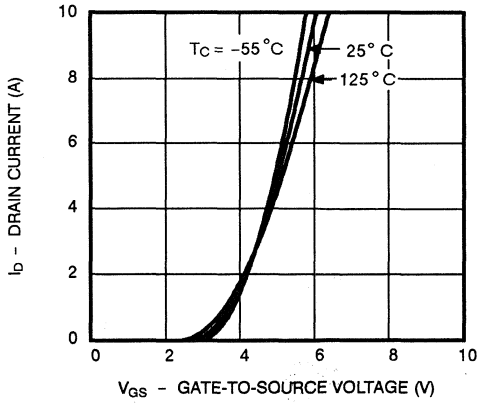


Figure 3. Transconductance

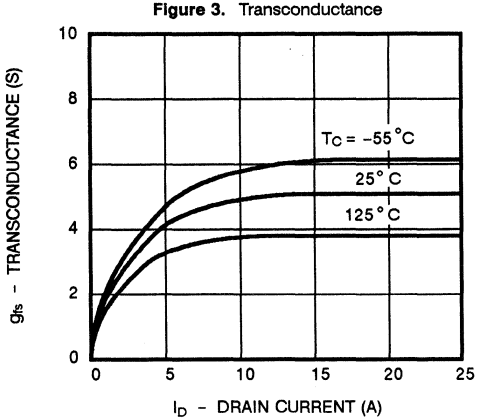


Figure 4. On-Resistance

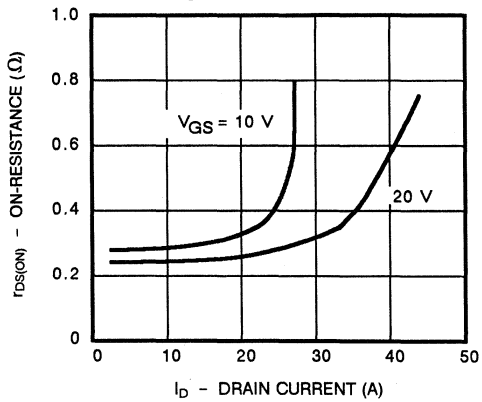


Figure 5. Capacitance

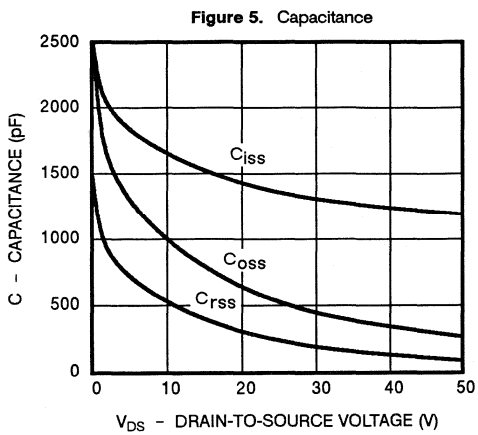
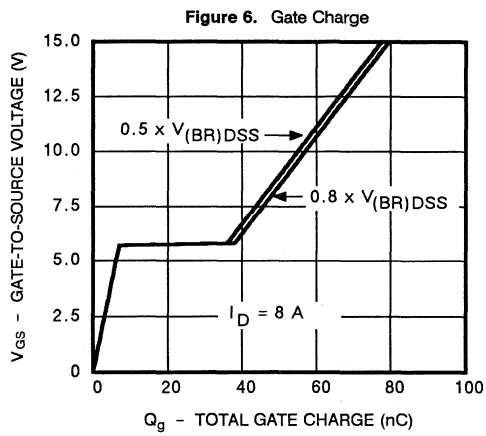


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

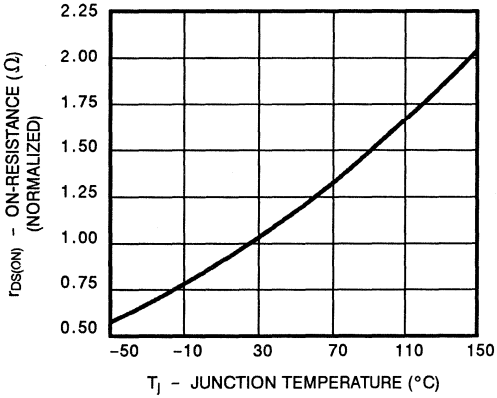
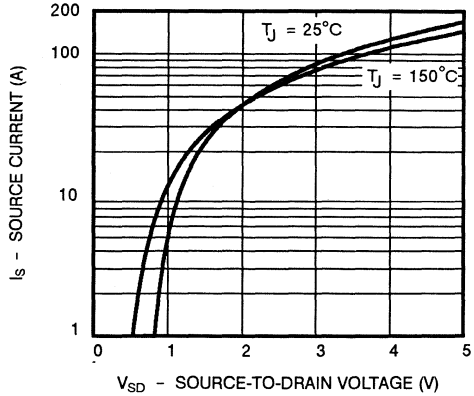


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

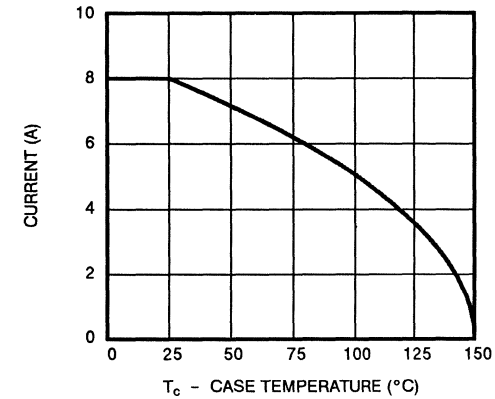
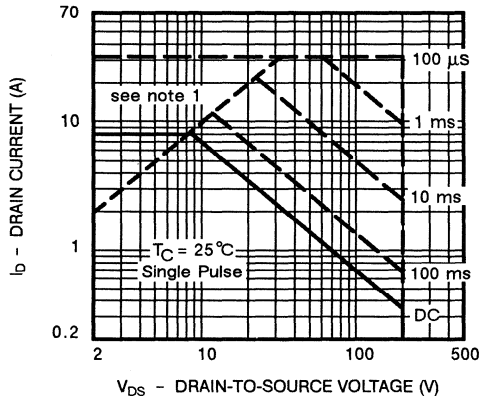
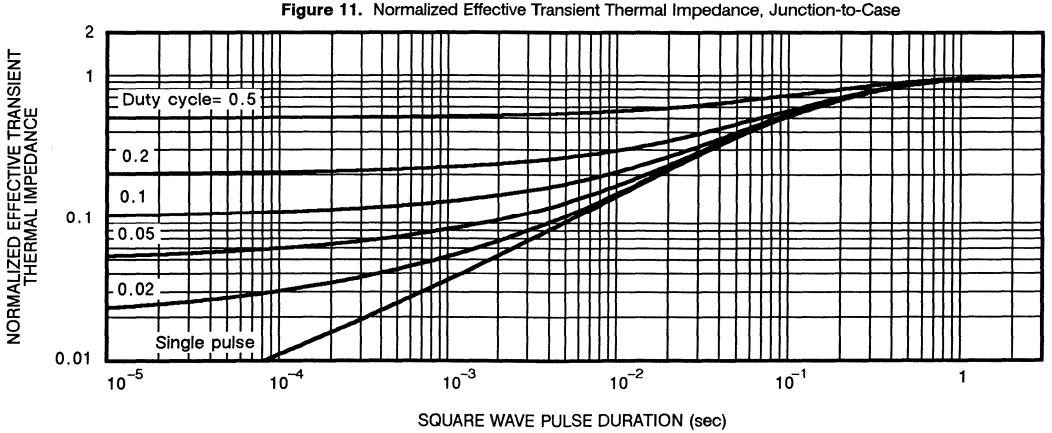


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

D469A
Quad High-Current Power Driver

FEATURES

- Wide Voltage Range
- High Current Drive
- Fast Rise and Fall Times
- Low Power Consumption
- Single Power Supply
- Low Output Impedance
- TTL/CMOS Inputs
- ESD Protection

APPLICATIONS

- Motor Drives
- Power Supplies
- dc/dc Converters

END PRODUCTS

- Computers
- Printers
- Avionics
- Industrial Controllers
- Robotics
- Central Office Equipment

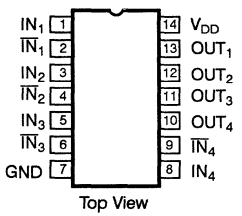
DESCRIPTION

The D469A is a quad monolithic high current and high speed driver designed to interface logic level signals to power MOSFETs, at voltages up to 15 V, in motor controls and other power control applications. This 4-channel power driver can source or sink up to 1.5 A.

The D469A is available in 14-pin side braze, 14-pin plastic dip and 20-pin PLCC packages. Performance grades include the military, A suffix (–55 to 125°C), and industrial, D suffix (–40 to 85°C) temperature ranges.

PIN CONFIGURATION

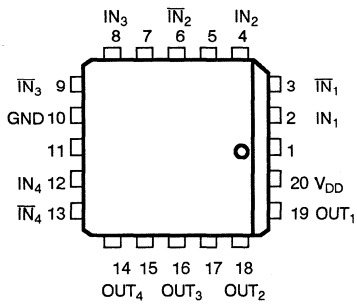
Dual-In-Line Package



Top View

Order Numbers:
Side Braze: D469AAP
Plastic: D469ADJ

PLCC Package



Top View

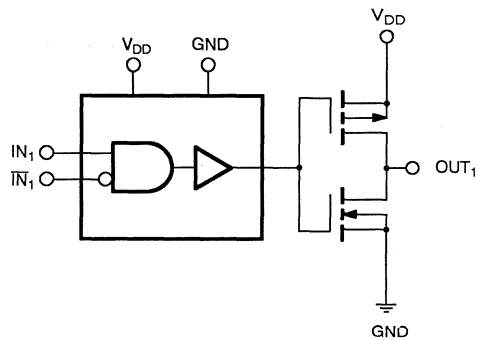
Order Number:
Plastic: D469ADN

Truth Table

IN_X	$\overline{IN}_X$	OUT_X
0	0	LO
0	1	LO
1	0	HI
1	1	LO

FUNCTIONAL BLOCK DIAGRAM

Single Channel



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Siliconix incorporated

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias ..... −55 to 125°C

Storage Temperature ..... −65 to 150°C

Voltage on Any Pin with Respect to Ground ..... −0.3 to V_{DD} +0.3 V

Supply Voltage, V_{DD} ..... −0.3 to 18 V

Peak Output Current ..... ±1.5 A

	AK Suffix	DJ Suffix
Operating Temperature	−55 to 125°C	−40 to 85°C
Junction Temperature	150°C	150°C
Power Dissipation	1000 mW	750 mW
Derating	10 mW/°C above 50°C	6 mW/°C above 25°C
Θ_{JA}	100°C/W (No Airflow)	167°C/W (No Airflow)

SPECIFICATIONS[a]

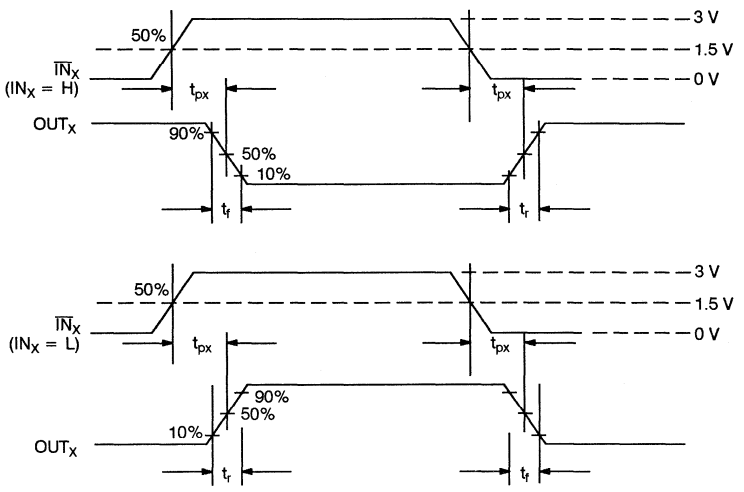
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V_{DD} = 15 V, T_A = Operating Temperature Range	TYP[d]	MIN[b]	MAX[b]	UNIT
INPUT						
Input Voltage HIGH	V_{INH}			2.4		V
Input Voltage LOW	V_{INL}				0.8	
Input Current with Input Voltage HIGH	I_{INH}	$V_{IN} = V_{DD}$	0.001		10	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V	−0.001	−10		
OUTPUT						
Output Voltage HIGH	V_{OUTH}	I_{OUT} = −100 mA One Output at a Time	14.44	13		V
		I_{OUT} = −10 mA	14.95	14.8		
Output Voltage LOW	V_{OUTL}	I_{OUT} = 100 mA One Output at a Time	0.33		1	
		I_{OUT} = 10 mA	0.033		0.1	
Output Source Current	I_{OS+}		1.5			A
Output Sink Current	I_{OS-}		−1.5			
Output Resistance	R_{OUT}	I_{OUT} = +10 mA	3.5			Ω
		I_{OUT} = −10 mA	5.5			
DYNAMIC						
Propagation Delay	t_{px}	C_L = 1000 pF	30		80	ns
Rise Time	t_r		10			
Fall Time	t_f		10			
Input Capacitance	C_{In}		5			pF

SPECIFICATIONS[a]

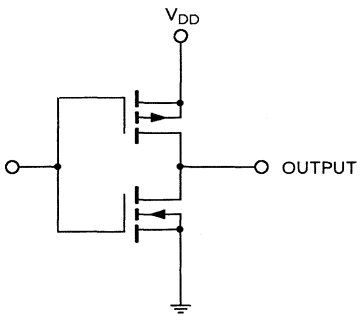
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V_{DD} = 15 V, T_A = Operating Temperature Range	TYP[d]	MIN[b]	MAX[b]	UNIT
SUPPLY						
Supply Current	I_{DD}	IN_X = $\overline{IN}_X$ = 0 V, V_{DD} = 15.75 V	1.4		7	mA
		IN_X = $\overline{IN}_X$ = 3 V, V_{DD} = 15.75 V	14		30	
		f = 100 kHz, V_{DD} = 15.75 V, C_L = 1000 pF, One Output at a Time	7			

[a]Refer to PROCESS OPTION FLOWCHART in the Siliconix data book for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY at T_A = 25°C, not guaranteed nor subject to production testing.

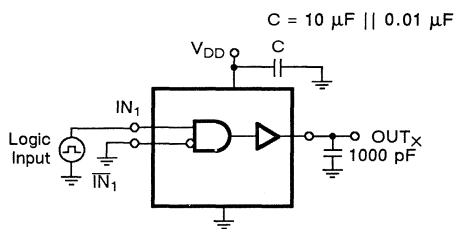
AC TESTING CONDITIONS



OUTPUT STRUCTURE



SWITCHING TIME TEST CIRCUIT*

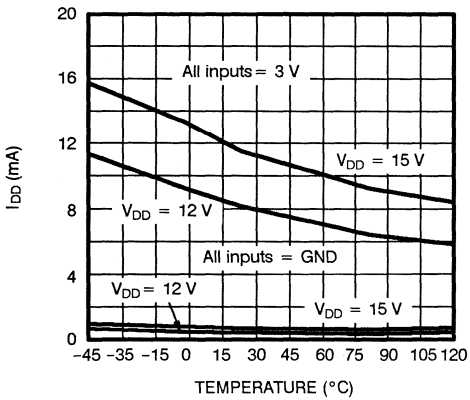


*Test repeated for inverting input

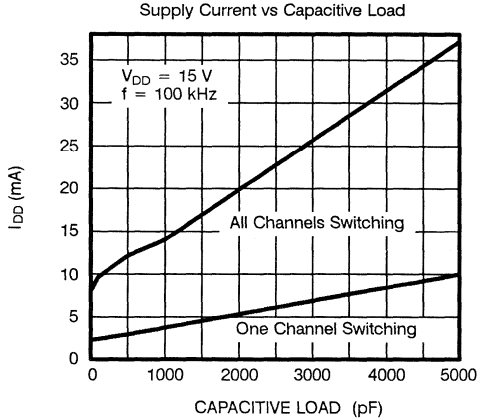
5

TYPICAL CHARACTERISTICS

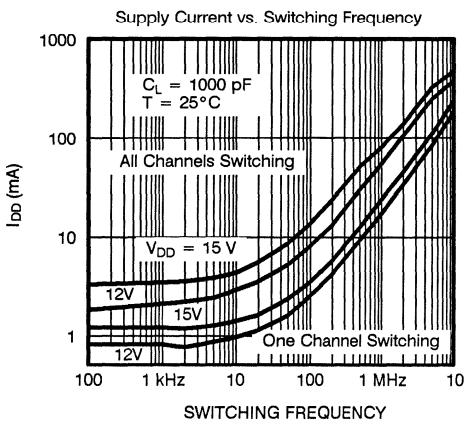
Supply Current vs Temperature



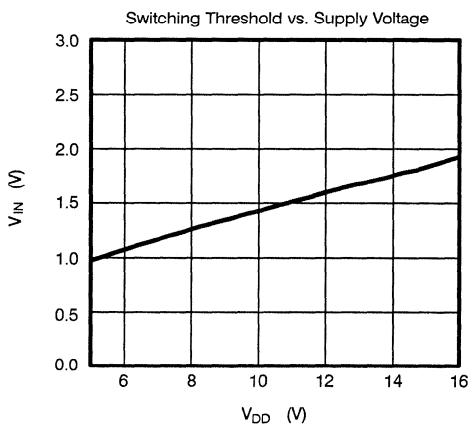
Supply Current vs Capacitive Load



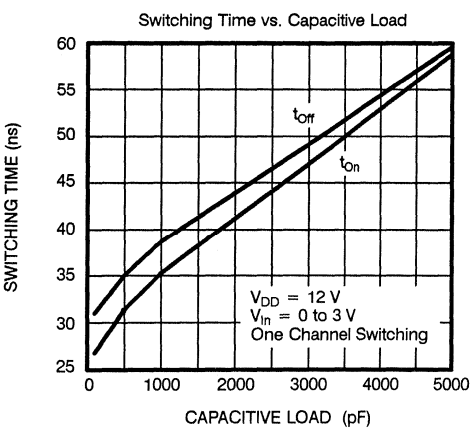
Supply Current vs. Switching Frequency



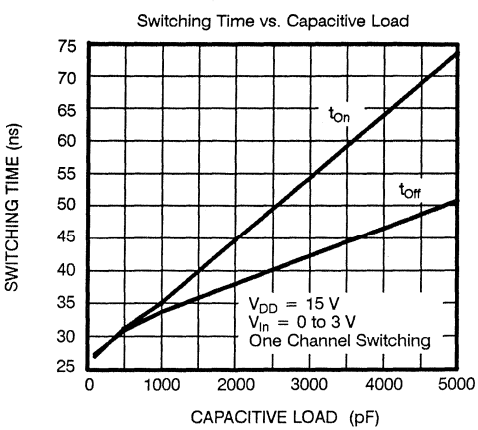
Switching Threshold vs. Supply Voltage



Switching Time vs. Capacitive Load



Switching Time vs. Capacitive Load



Si9100/Si9101
3-W High-Voltage Switchmode Regulators

FEATURES

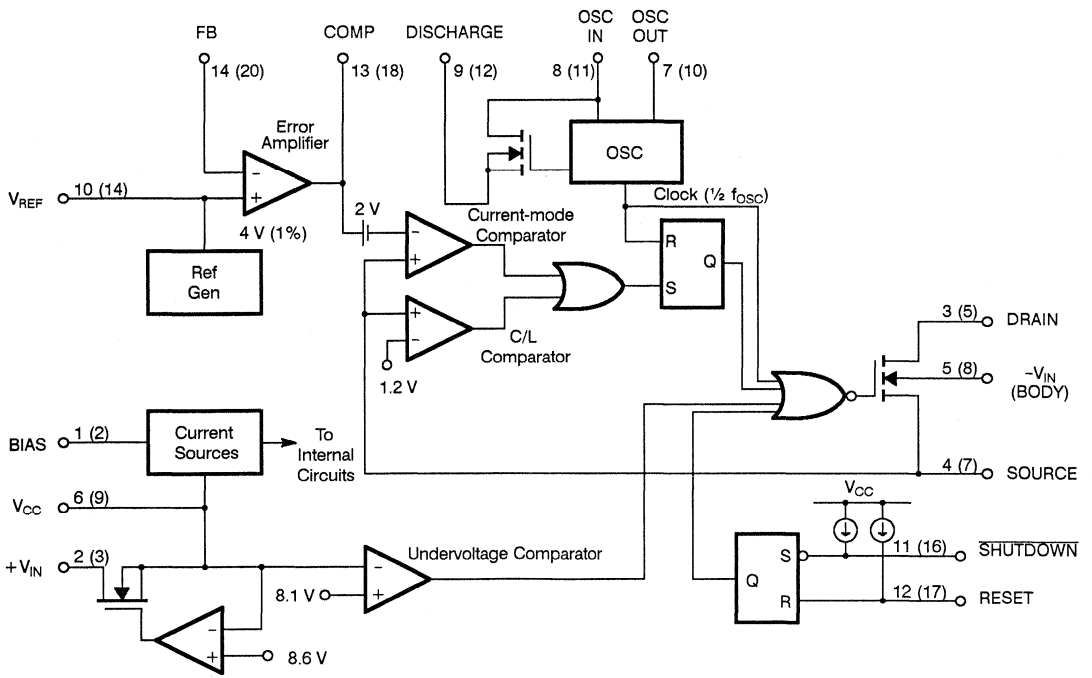
- 10 to 70 V Input Range
- Current-mode Control
- On chip 150 V, 5 Ω MOSFET Switch
- Reference Selection
  Si9100 – ±1%
  Si9101 – ±10%
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

DESCRIPTION

The Si9100/Si9101 high-voltage switchmode regulators are monolithic BiC/DMOS integrated circuits which contain most of the components necessary to implement high-efficiency dc-to-dc converters up to 3 watts. They can either be operated from a low-voltage dc supply, or directly from a 10- to 70-V unregulated dc power source. The Si9100/Si9101 may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward), or by using a level shift circuit can generate a +5 V or a -5 V non-isolated output from a -48 V source.

The Si9100/Si9101 is available in 14-pin plastic, CerDIP and PLCC 20-pin packages, and is specified over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 70 V

V_{DS} ..... 150 V

I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2.5 A

I_D (rms) ..... 350 mA

Logic Inputs (RESET, SHUTDOWN, OSC IN) ..... -0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V

HV Preregulator Input Current (continuous) ..... 3 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)*
14-Pin Ceramic DIP (K Suffix)** ..... 1000 mW
14-Pin Plastic DIP (J Suffix)*** ..... 750 mW
20-Pin PLCC (N Suffix)**** ..... 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Ceramic DIP ..... 100°C/W
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 10 mW/°C above 50°C
***Derate 6 mW/°C above 25°C
****Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 13.5 V

$+V_{IN}$ ..... 10 V to 70 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to 7 V

Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85,125°C 3 = -40,-55°C		LIMITS A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
REFERENCE									
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	1	4.0	3.92	4.08	3.92	4.08	V
Output Impedance[c]	Z_{OUT}		1	30	15	45	15	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	1	100	70	130	70	130	µA
Temperature Stability[c]	T_{REF}		2,3	0.1		0.25		0.25	mV/°C
OSCILLATOR									
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e	1	100	80	120	80	120	kHz
		R_{OSC} = 150 k, See Note e	1	200	160	240	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	10		15		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500		500	ppm/°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ		1 = 25°C 2 = 85,125°C 3 = -40,-55°C		LIMITS A SUFFIX -55 to 125°C		LIMITS D SUFFIX -40 to 85°C		UNIT
				TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
ERROR AMPLIFIER										
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Si9100 Si9101	1 1	4.00 4.00	3.96 3.60	4.04 4.40	3.96 3.60	4.04 4.40	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V		1	25		500		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$, (OSC Disabled)		1	±15		±40		±40	mV
Open Loop Voltage Gain[c]	A_{VOL}			1	80	60		60		dB
Unity Gain Bandwidth[c]	BW			1	1					MHz
Dynamic Output Impedance[c]	Z_{OUT}			1	1000		2000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)		1	-2.0		-1.4		-1.4	mA
		Sink (V_{FB} = 4.5 V)		1	0.15	0.12		0.12		
Power Supply Rejection	PSRR	OSC IN = $-V_{IN}$, (OSC Disabled)		1	70	50		50		dB
CURRENT LIMIT										
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V		1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output[c]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1		1	100		200		200	ns
PREREGULATOR/STARTUP										
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA		1			70		70	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 9.4 V		1			10		10	µA
Preregulator Startup Current	I_{START}	Pulse Width ≤ 300 µs V_{CC} = V_{UVLO}		1	15	8		8		mA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA		1	8.6	7.8	9.4	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description		1	8.1	7.0	8.9	7.0	8.9	
V_{REG} -V_{UVLO}	V_{DELTA}			1	0.6	0.3		0.3		
SUPPLY										
Supply Current	I_{CC}			1	0.6	0.45	1.0	0.45	1.0	mA
Bias Current	I_{BIAS}			1	15	10	20	10	20	µA
LOGIC										
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2		1	50		100		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3		1		50		50		

5

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85,125°C 3 = -40,-55°C		LIMITS A SUFFIX -55 to 125°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
LOGIC (Cont'd)									
RESET Pulse Width	t_{RW}	See Figure 3	1		50		50		ns
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	t_{LW}	See Figure 3	1		25		25		ns
Input LOW Voltage	V_{IL}		1			2.0		2.0	V
Input HIGH Voltage	V_{IH}		1		8.0		8.0		V
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		-35		µA
MOSFET SWITCH									
Breakdown Voltage	$V_{(BR)DSS}$	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V I_{DRAIN} = 100 µA	2,3	180	150		150		V
Drain-Source ON Resistance[f]	$r_{DS(ON)}$	V_{SOURCE} = 0 V I_{DRAIN} = 100 mA	1	3		5		5	Ω
Drain OFF Leakage Current	I_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V V_{DRAIN} = 100 V	1			10		10	µA
Drain Capacitance	C_{DS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V	1	35					pF

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = ≤ 5 pF
[f]Temperature coefficient of $r_{DS(ON)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

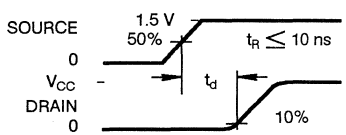


Figure 1

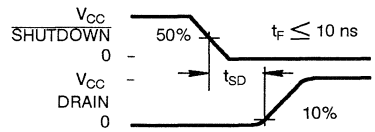


Figure 2

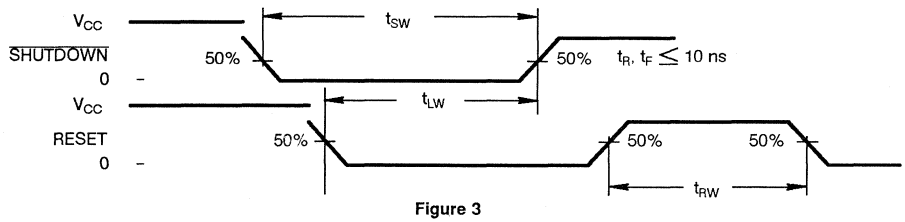


Figure 3

TYPICAL CHARACTERSITICS

Figure 4. $+V_{IN}$ vs. $+I_{IN}$ at Startup

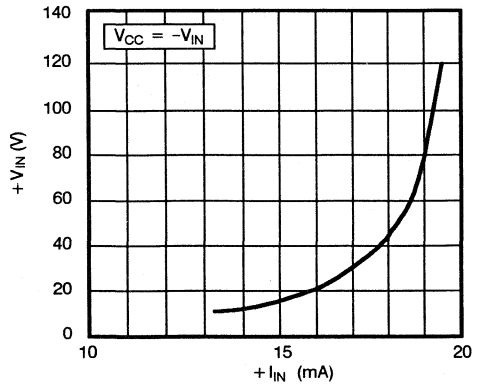
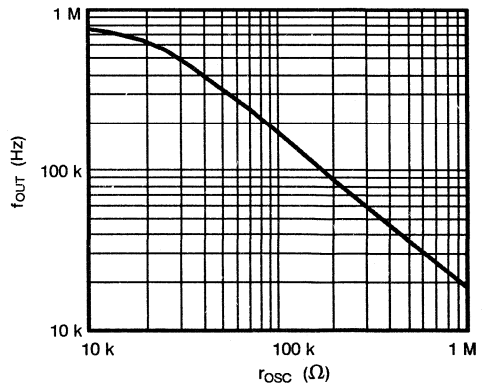
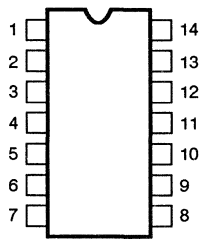


Figure 5. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package

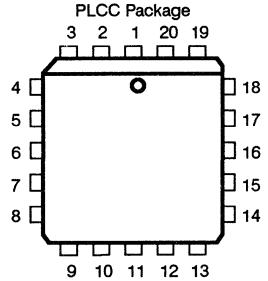


Top View

Order Numbers:

CerDIP:
Si9100AK
Plastic:
Si9100DJ, SI9101DJ

PLCC Package



Top View

Order Number:

Si9100DN, SI9101DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical preregulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9100, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. During the reference trimming procedure the error amplifier is connected for unity gain in order to compensate for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

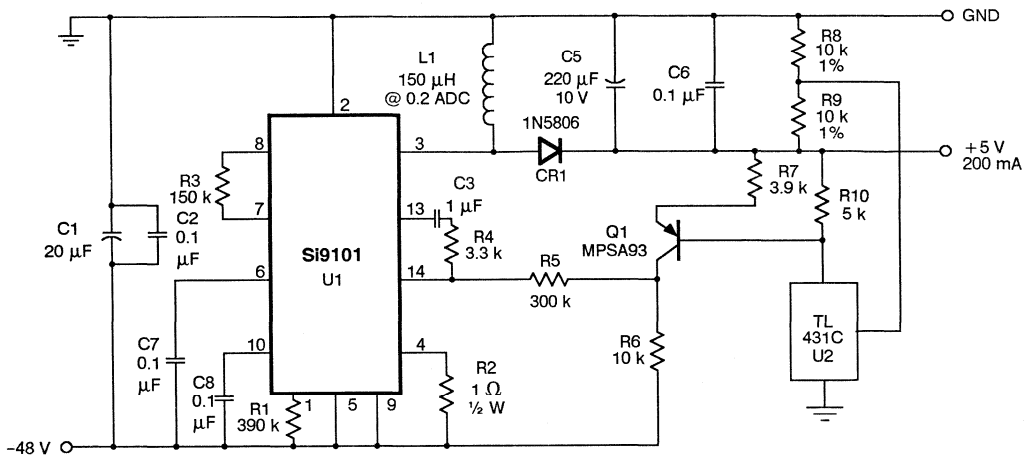
Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

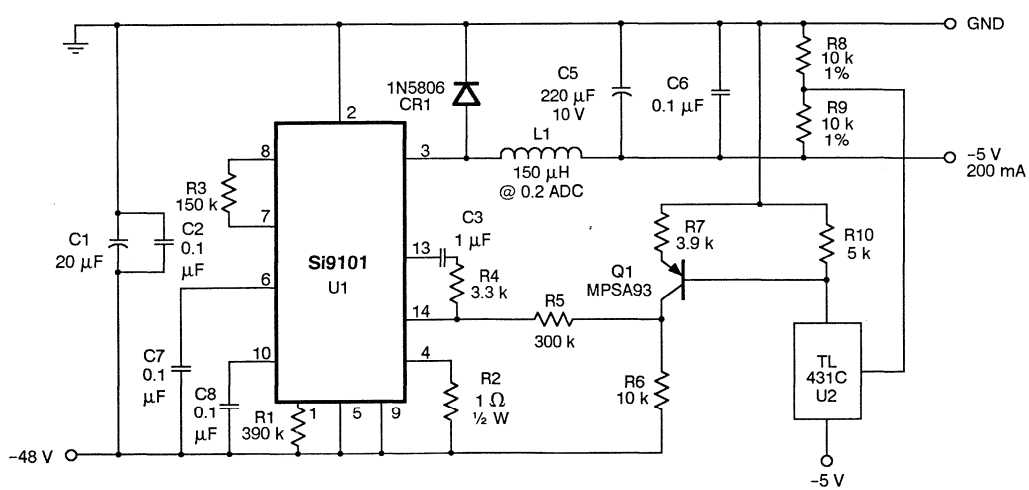
OUTPUT SWITCH

The output switch is a 5 Ω, 150 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

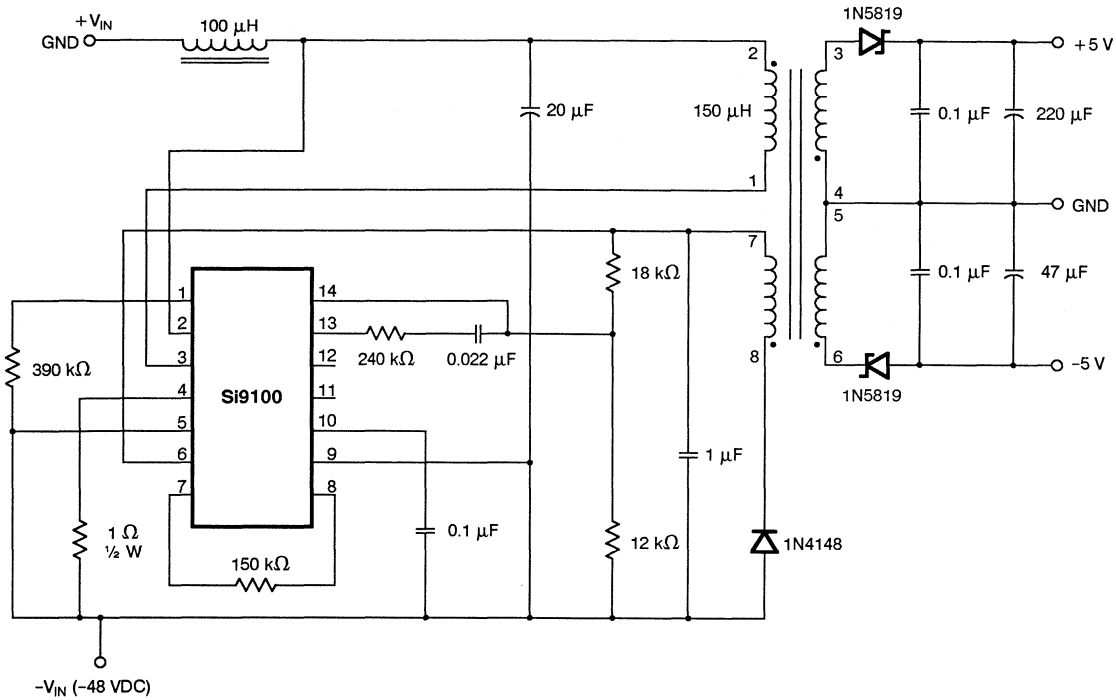
Buck-boost
Non-isolated 1-W Supply



Non-isolated 1-W Supply (Buck)



One-watt Flyback Converter for Telecommunications Power Supplies*



* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN87-1 and AN87-2.

Si9102

3-W High-Voltage Switchmode Regulator

FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- On chip 200 V, 7 Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)

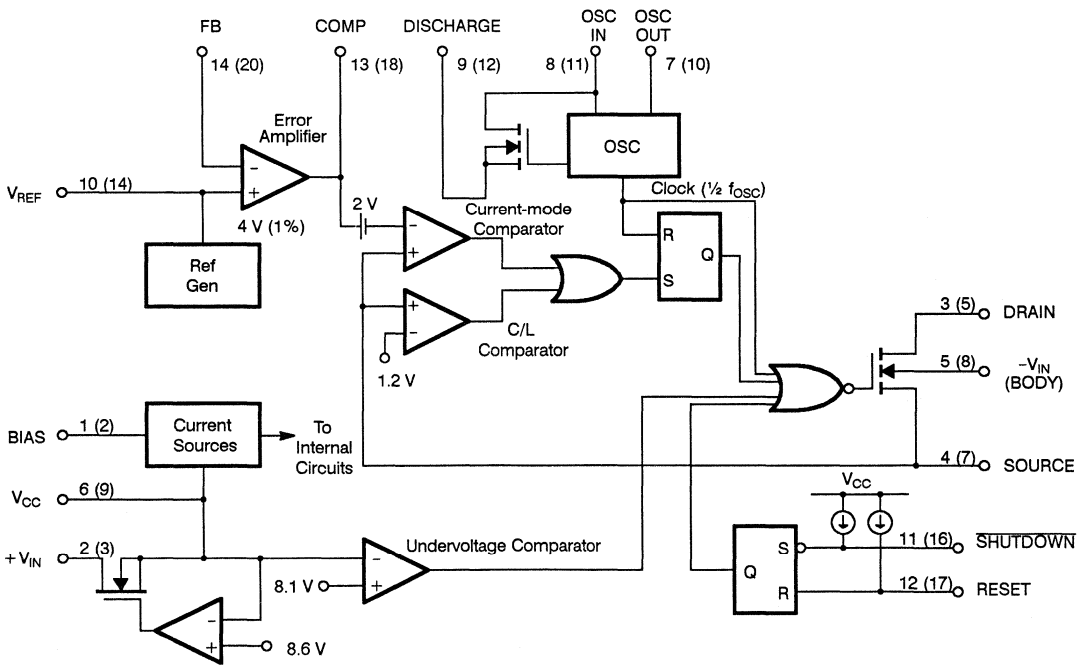
DESCRIPTION

The Si9102 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9102 is available in 14-pin plastic and 20-pin PLCC packages, and is specified over the D suffix (–40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... -0.3 V to V_{CC} + 0.3 V
Linear Inputs
(FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Preregulator Input Current (continuous) ..... 3 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)*
14-Pin Plastic DIP (J Suffix)** ..... 750 mW
20-Pin PLCC (N Suffix)*** ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 6 mW/°C above 25°C
***Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85 3 = -40C TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
REFERENCE							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	1 2,3	4.0	3.92 3.86	4.08 4.14	V
Output Impedance[c]	Z_{OUT}		1	30	15	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	1	100	70	130	µA
Temperature Stability[c]	T_{REF}		2,3	0.1		0.25	mV/°C
OSCILLATOR							
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e	1	100	80	120	kHz
		R_{OSC} = 150 k, See Note e	1	200	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	10		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500	ppm/°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85 3 = -40 TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
ERROR AMPLIFIER							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = - V_{IN} (OSC Disabled)	1	4.00	3.96	4.04	V
Input BIAS Current	I_{FB}	OSC IN = - V_{IN}, V_{FB} = 4 V	1	25		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = - V_{IN} (OSC Disabled)	1	±15		±40	mV
Open Loop Voltage Gain[c]	A_{VOL}		1	80	60		dB
Unity Gain Bandwidth[c]	BW		1	1	0.7		MHz
Dynamic Output Impedance[c]	Z_{OUT}		1	1000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	1	-2.0		-1.4	mA
		Sink (V_{FB} = 4.5 V)	1	0.15	0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	1	70	50		dB
CURRENT LIMIT							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	1	1.2	1.0	1.4	V
Delay to Output[c]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	1	100		200	ns
PREREGULATOR/STARTUP							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	1			120	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10	µA
Preregulator Startup Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	1	15	8		mA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA	1	8.6	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	1	8.1	7.0	8.9	
V_{REG} - V_{UVLO}	V_{DELTA}		1	0.6	0.3		
SUPPLY							
Supply Current	I_{CC}		1	0.6	0.45	1.0	mA
Bias Current	I_{BIAS}		1	15	10	20	µA
LOGIC							
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = -V_{IN}, See Figure 2	1	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	1		50		

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Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85 3 = -40 TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
LOGIC (Cont'd)							
RESET Pulse Width	t_{RW}	See Figure 3	1		50		ns
Latching Pulse Width SHUTDOWN and RESET LOW	t_{LW}	See Figure 3	1		25		ns
Input LOW Voltage	V_{IL}		1			2.0	V
Input HIGH Voltage	V_{IH}		1		8.0		V
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		µA
MOSFET SWITCH							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	2,3	220	200		V
Drain-Source ON Resistance[f]	$r_{DS(ON)}$	I_{DRAIN} = 100 mA	1			7	Ω
Drain OFF Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	1	5		10	µA
Drain Capacitance	C_{DS}		1	35			pF

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = $\leq$ 5 pF
[f]Temperature coefficient of $r_{DS(ON)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

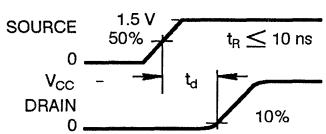


Figure 1

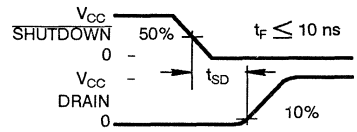


Figure 2

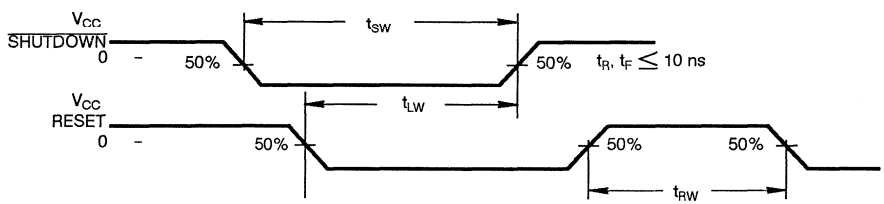


Figure 3

TYPICAL CHARACTERSITICS

Figure 4. $+V_{IN}$ vs. $+I_{IN}$ at Startup

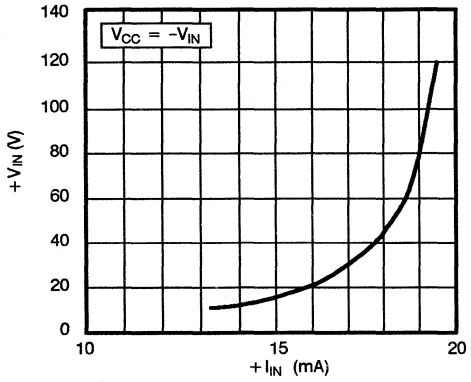
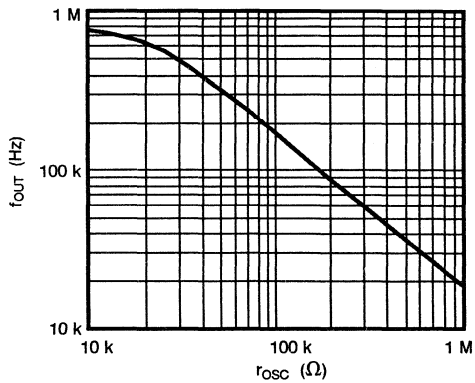
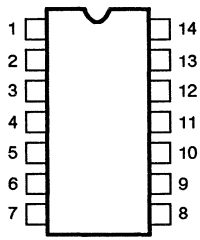


Figure 5. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package

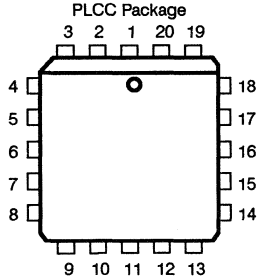


Top View

Order Numbers:

Plastic: Si9102DJ

PLCC Package



Top View

Order Number:

Plastic: Si9102DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical preregulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9102, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

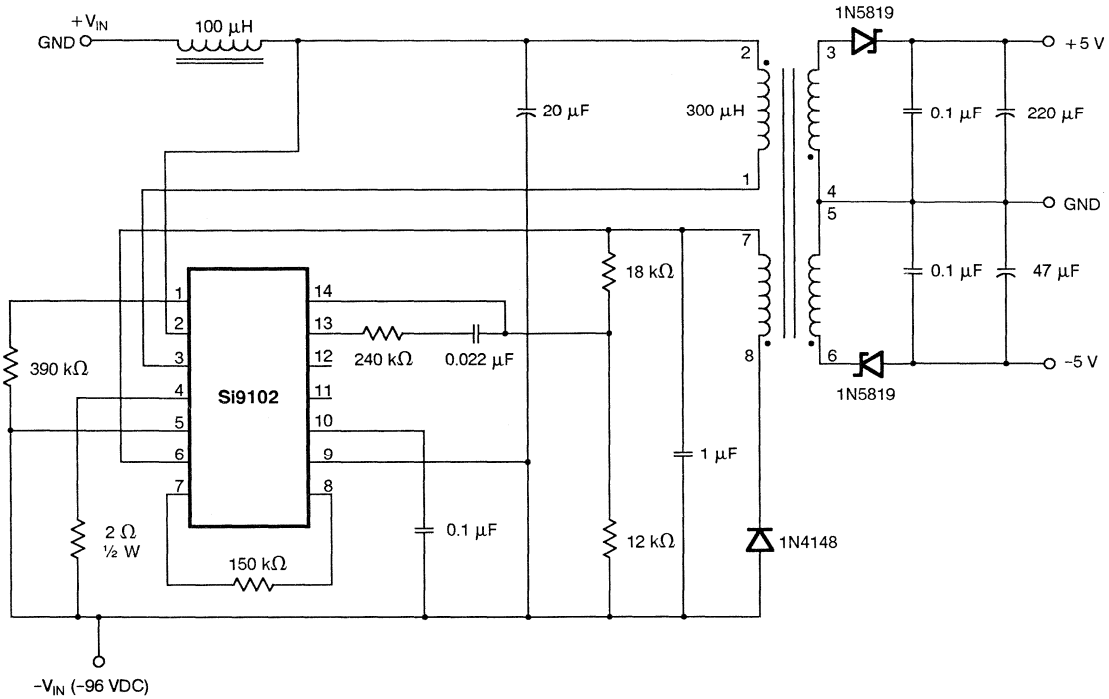
OUTPUT SWITCH

The output switch is a 7 Ω, 200 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

NOTE: Pin numbers refer to 14-pin DIP.

APPLICATIONS

Flyback Converter for Double Battery Telecommunications Power Supplies



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Si9105

1-W High-Voltage Switchmode Regulator

FEATURES

- CCITT Compatible
- Current-mode Control
- Low Power Consumption (less than 5 mW)
- 10 to 120 V Input Range
- 200 V, 250 mA MOSFET
- Internal Start-up Circuit
- Current-mode Control
- $\overline{\text{SHUTDOWN}}$ and RESET

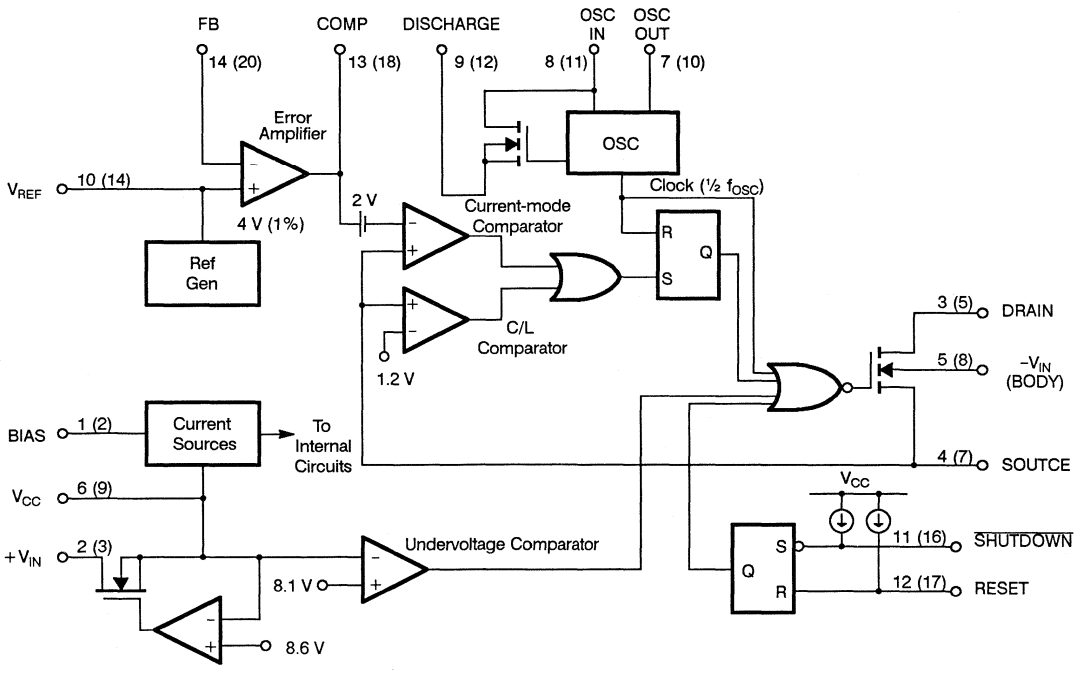
DESCRIPTION

The Si9105 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5 mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ±5 V).

The Si9105 is available in 14-pin plastic and 20-pin PLCC packages, and is specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) ..... -0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Preregulator Input Current (continuous) ..... 5 mA**
Note 1: 300 µs pulse, 2% duty cycle
Storage Temperature (D Suffix) ..... -65 to 125°C
Operating Temperature (D Suffix) ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)*
14-Pin Plastic DIP (J Suffix)*** ..... 750 mW
20-Pin PLCC (N Suffix)**** ..... 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Continuous current may be limited by the maximum input voltage and the package power dissipation.
***Derate 6 mW/°C above 25°C
****Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} - 3 V
Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ R_{OSC} = 910 kΩ	1 = 25°C 2 = 85°C 3 = -40°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	
REFERENCE							
Output Voltage	V_R	OSC IN = - V_{IN} (OSC Disabled) R_L = 10 MΩ	1	4.00	3.92	4.08	V
Output Impedance[c]	Z_{OUT}	OSC IN = - V_{IN}	1	30	15	45	kΩ
Short Circuit Current	I_{SREF}	OSC IN = - V_{IN}, V_{REF} = $-V_{IN}$	1	100	70	130	µA
Temperature Stability[c]	T_{REF}	OSC IN = - V_{IN}	2,3	0.1		0.25	mV/°C
OSCILLATOR							
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		MHz
Initial Accuracy	f_{OSC}	See Note e	1	40	32	48	kHz
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	10		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500	ppm/°C
ERROR AMPLIFIER							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = - V_{IN} (OSC Disabled)	1	4	3.96	4.04	V
Input BIAS Current	I_{FB}	OSC IN = - V_{IN}, V_{FB} = 4 V	1	25		500	nA
Open Loop Voltage Gain[c]	A_{VOL}	OSC IN = - V_{IN} (OSC Disabled)	1	80	60		dB

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ R_{OSC} = 910 kΩ	1 = 25°C 2 = 85°C 3 = -40°C TEMP		LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
ERROR AMPLIFIER							
Unity Gain Bandwidth[c]	BW	OSC IN = $-V_{IN}$	1	0.8	0.5		MHz
Dynamic Output Impedance[c]	Z_{OUT}		1	1			kΩ
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	1	-1.2		-0.32	mA
		Sink (V_{FB} = 4.5 V)	1	0.08	0.05		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	1	70			dB
CURRENT LIMIT							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	1	1.0	0.8	1.2	V
Delay to Output[c]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	1	200		300	ns
PREREGULATOR/STARTUP							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	1			120	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10	µA
Preregulator Startup Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	1	15	8		mA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA	1	8.3	7.5	9.1	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	1	7.8	7.0	8.6	
V_{REG} - V_{UVLO}	V_{DELTA}		1	0.5	0.25		
SUPPLY							
Supply Current	I_{CC}		1	0.35		0.5	mA
Bias Current	I_{BIAS}		1	7.5			µA
LOGIC							
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	1	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	1		50		
RESET Pulse Width	t_{RW}		1		50		
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	t_{LW}		1		25		
Input LOW Voltage	V_{IL}		1			2.0	V
Input HIGH Voltage	V_{IH}		1		8.0		
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		

5

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ R_{OSC} = 910 kΩ	1 = 25°C 2 = 85°C 3 = -40°C TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
MOSFET SWITCH							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	2,3	220	200		V
Drain-Source ON Resistance[f]	$r_{DS(ON)}$	I_{DRAIN} = 100 mA	1	4		5	Ω
Drain OFF Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	1			10	µA
Drain Capacitance	C_{DS}		1	35			pF

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = ≙ 5 pF
[f]Temperature coefficient of $r_{DS(ON)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

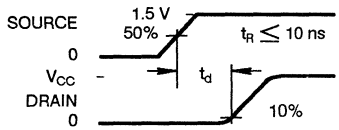


Figure 1

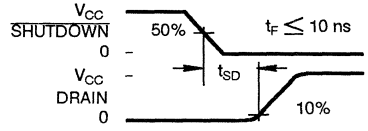


Figure 2

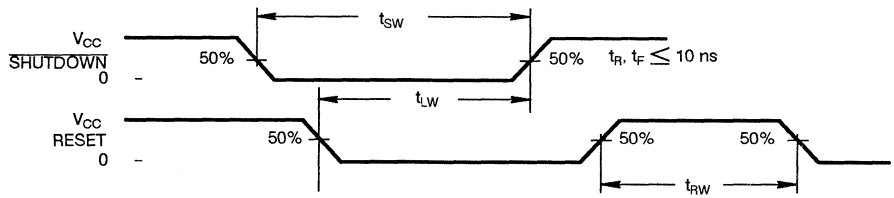
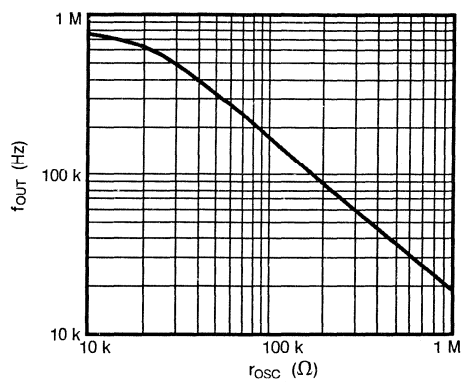


Figure 3

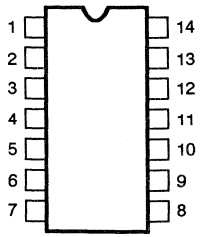
TYPICAL CHARACTERSITICS

Figure 4. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package

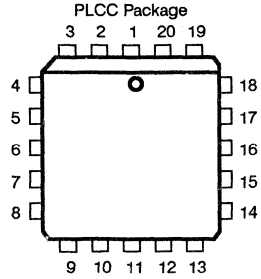


Top View

Order Numbers:

Plastic: Si9105DJ

PLCC Package



Top View

Order Number:

Plastic: Si9105DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9105 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.3 V. If V_{CC} is not forced to exceed the 8.3 V threshold, then V_{CC} will be regulated to a nominal value of 8.3 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 7.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

BIAS

To properly set the bias for the Si9105, a 820 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 7.5 µA.

REFERENCE SECTION

The reference section of the Si9105 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9105 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, whose 1 kΩ dynamic output impedance enables it to be used with feedback compensation (unlike transconductance amplifiers). A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

DETAILED DESCRIPTION

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 4 for graph of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to a maximum of 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ pin to provide variable shutdown time.

OUTPUT SWITCH

The output switch is a 5 Ω, 200 V lateral DMOS transistor. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9105 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

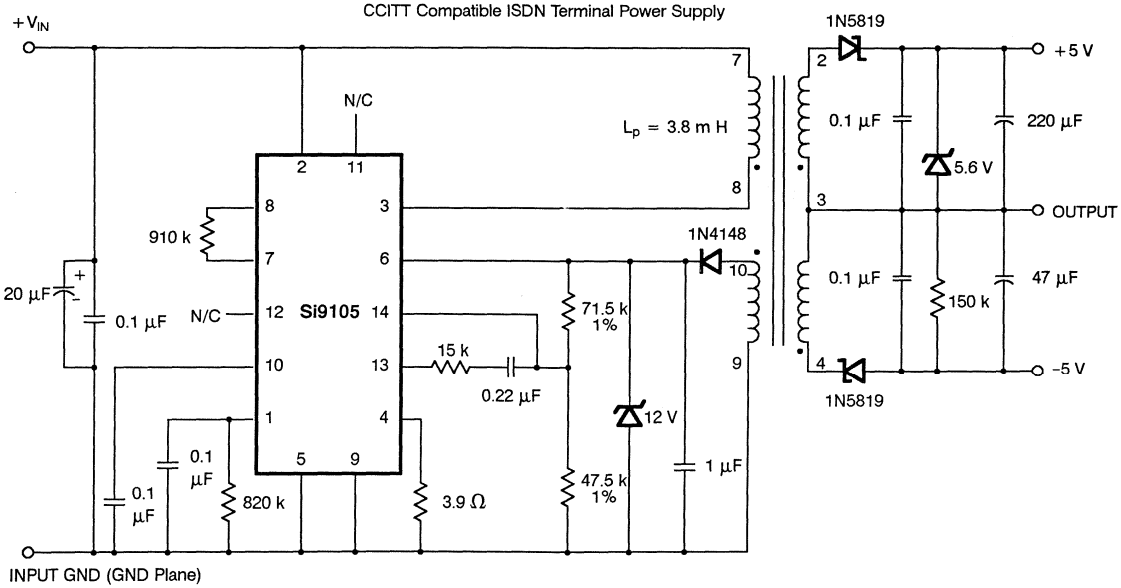
Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↓	L	OFF (Latched) (No Change)

NOTE: Pin numbers refer to 14-pin Dip.

APPLICATIONS

CCITT Compatible ISDN Terminal Power Supply



Si9110/Si9111
High-Voltage Switchmode Controllers

FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- High-speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)
- Reference Selection
  Si9110 – ±1%
  Si9111 – ±10%
- $\overline{\text{SHUTDOWN}}$ and RESET

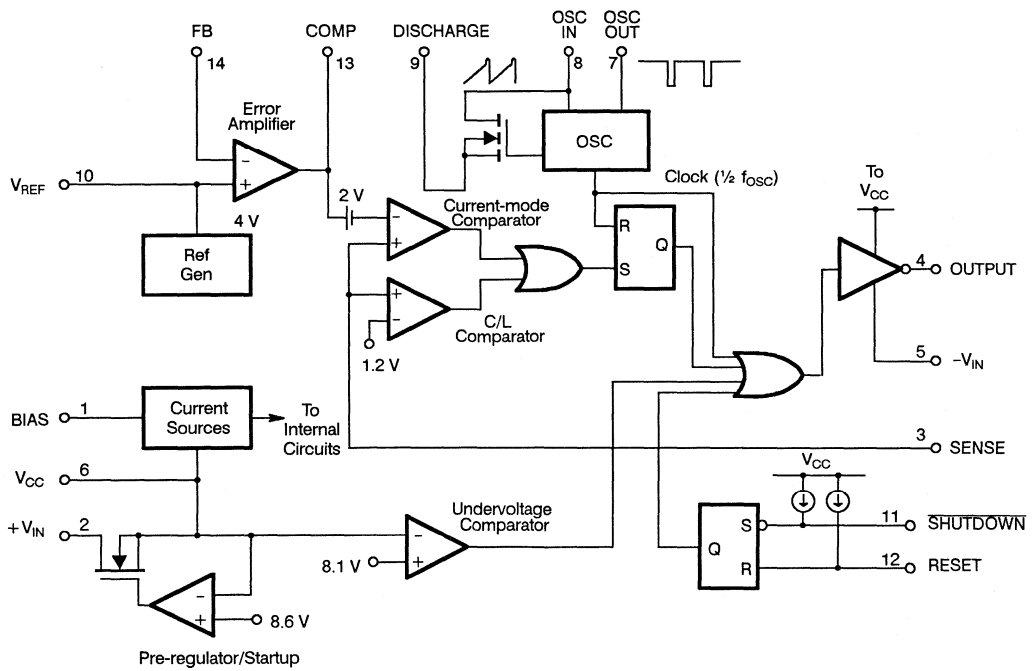
DESCRIPTION

The Si9110/9111 are BiC/DMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110 or Si9111 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9110 and Si9111 are available in 14-pin plastic, SOIC and CerDIP packages, and are specified over the military, A suffix (–55 to 125°C) and industrial, D suffix (–40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 120 V

Logic Inputs (RESET, SHUTDOWN, OSC IN, OSC OUT) ..... -0.3 V to $V_{CC} + 0.3$ V

Linear Inputs (FEEDBACK, SENSE, BIAS, V_{REF}) ..... -0.3 V to $V_{CC} + 0.3$ V

HV Preregulator Input Current (continuous) ..... 5 mA

Storage Temperature (A, D Suffix) ..... -65 to 150°C

Operating Temperature (A Suffix) ..... -55 to 125°C

(D Suffix) ..... -40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)*

14-Pin Ceramic DIP (K Suffix)** ..... 1000 mW

14-Pin Plastic DIP (J Suffix)*** ..... 750 mW

14-Pin SOIC (Y Suffix)**** ..... 900 mW

Thermal Impedance (Θ_{JA})

14-Pin Ceramic DIP ..... 100°C/W

14-Pin Plastic DIP ..... 167°C/W

14-Pin SOIC ..... 140°C/W

*Device mounted with all leads soldered or welded to PC board.

**Derate 10 mW/°C above 50°C

***Derate 6 mW/°C above 25°C

****Derate 7.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 13.5 V

$+V_{IN}$ ..... 10 V to 120 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to $V_{CC} - 3$ V

Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified: DISCHARGE = $-V_{IN}$ = 0 V; V_{CC} = 10 V, $+V_{IN}$ = 48 V; R_{BIAS} = 390 kΩ; R_{OSC} = 330 kΩ		1 = 25°C, 2 = 85,125°C, 3 = −40,−55°C: TEMP	TYP[d]	LIMITS A SUFFIX −55 to 125°C: MIN[b]	MAX[b]	LIMITS D SUFFIX −40 to 85°C: MIN[b]	MAX[b]	UNIT
REFERENCE										
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled)	Si9110	1	4.0	3.92	4.08	3.92	4.08	V
			Si9111	1		3.60	4.40	3.60	4.40	
		R_L = 10 MΩ	Si9110	2,3[c]		3.82	4.16	3.86	4.14	
			Si9111	2,3[c]		3.50	4.48	3.52	4.46	
Output Impedance[c]	Z_{OUT}			1	30	15	45	15	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		1	100	70	130	70	130	µA
Temperature Stability[c]	T_{REF}			2,3	0.11		0.25		0.25	mV/°C
OSCILLATOR										
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0		1	3	1		1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e		1	100	80	120	80	120	kHz
		R_{OSC} = 150 k, See Note e		1	200	160	240	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) − f(9.5 V) / f(9.5 V)		1	10		15		15	%
Temperature Coefficient[c]	T_{OSC}			2,3	200		500		500	ppm/°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ		1 = 25°C 2 = 85,125°C 3 = -40,-55°C TEMP	TYP[d]	LIMITS A SUFFIX -55 to 125°C MIN[b]	MAX[b]	D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
ERROR AMPLIFIER										
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Si9110	1	4.00	3.96	4.04	3.96	4.04	V
			Si9111	1	4.00	3.60	4.40	3.60	4.40	
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V		1	25		500		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)		1	±15		±40		±40	mV
Open Loop Voltage Gain[c]	A_{VOL}			1	80	60		60		dB
Unity Gain Bandwidth[c]	BW			1	1.3	1		1		MHz
Dynamic Output Impedance[c]	Z_{OUT}			1	1000		2000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)		1	-2.0		-1.4		-1.4	mA
		Sink (V_{FB} = 4.5 V)		1	0.15	0.12		0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V		1	70	50		50		dB
CURRENT LIMIT										
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V		1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1		1	100		150		150	ns
PREREGULATOR/STARTUP										
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA		1		120		120		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V		1			10		10	µA
Preregulator Startup Current	I_{START}	Pulse Width ≤ 300 µs V_{CC} = V_{ULVO}		1	15	8		8		mA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA		1	8.6	7.8	9.4	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}			1	8.1	7.0	8.9	7.0	8.9	
V_{REG} -V_{UVLO}	V_{DELTA}			1	0.6	0.3		0.3		
SUPPLY										
Supply Current	I_{CC}	C_{LOAD} < 75 pF (Pin 4)		1	0.6	0.45	1.0	0.45	1.0	mA
Bias Current	I_{BIAS}			1	15	10	20	10	20	µA
LOGIC										
$\overline{\text{SHUTDOWN}}$ Delay[c]	t_{SD}	C_L = 500 pF, V_{SENSE} -V_{IN} See Figure 2		1	50		100		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[c]	t_{SW}	See Figure 3		1		50		50		
RESET Pulse Width[c]	t_{RW}			1		50		50		

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Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85,125°C 3 = -40,-55°C		LIMITS A SUFFIX -55 to 125°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
LOGIC (Cont'd)									
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW[c]	t_{LW}	See Figure 3	1		25		25		ns
Input LOW Voltage	V_{IL}		1			2.0		2.0	V
Input HIGH Voltage	V_{IH}		1		8		8		
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		-35		
OUTPUT									
Output HIGH Voltage	V_{OH}	I_{OUT} = -10 mA	1 2,3		9.7 9.5		9.7 9.5		V
Output LOW Voltage	V_{OL}	I_{OUT} = 10 mA	1 2,3			0.30 0.50		0.30 0.50	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA Source or Sink	1 2,3	20 25		30 50		30 35	Ω
Rise Time	t_r	C_L = 500 pF	1	40		75		75	ns
Fall Time	t_f		1	40		75		75	

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = $\preceq$ 5 pF

TIMING WAVEFORMS

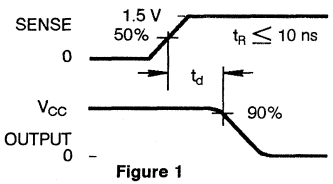


Figure 1

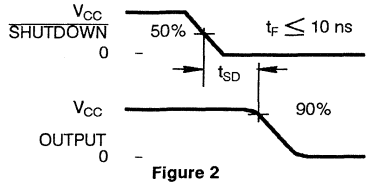


Figure 2

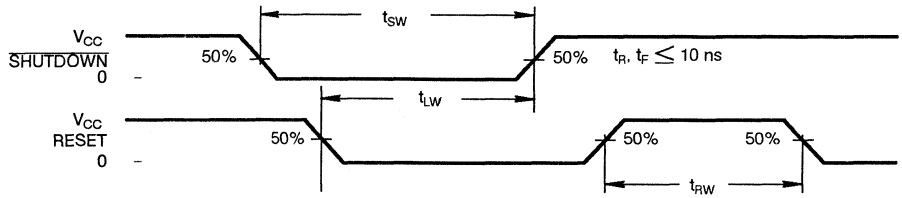


Figure 3

TYPICAL CHARACTERISTICS

Figure 4. $+V_{IN}$ vs. $+I_{IN}$ at Startup

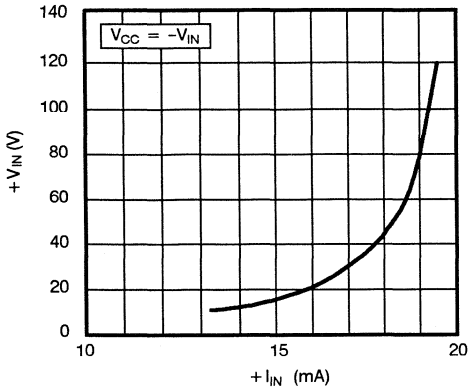
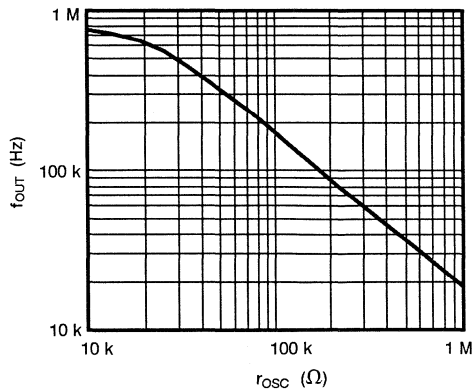
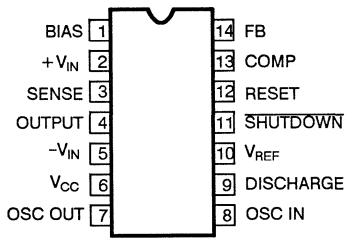


Figure 5. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package

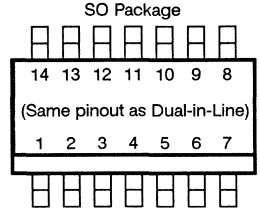


Top View

Order Numbers:

CerDIP: Si9110AK
Plastic: Si9110DJ, Si9111DJ

SO Package



Top View

Order Numbers:
Si9110DY, Si9111DY

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9110/Si9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical preregulator current at BiC/DMOS as a function of input voltage.

BIAS

To properly set the bias for the Si9110/Si9111, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

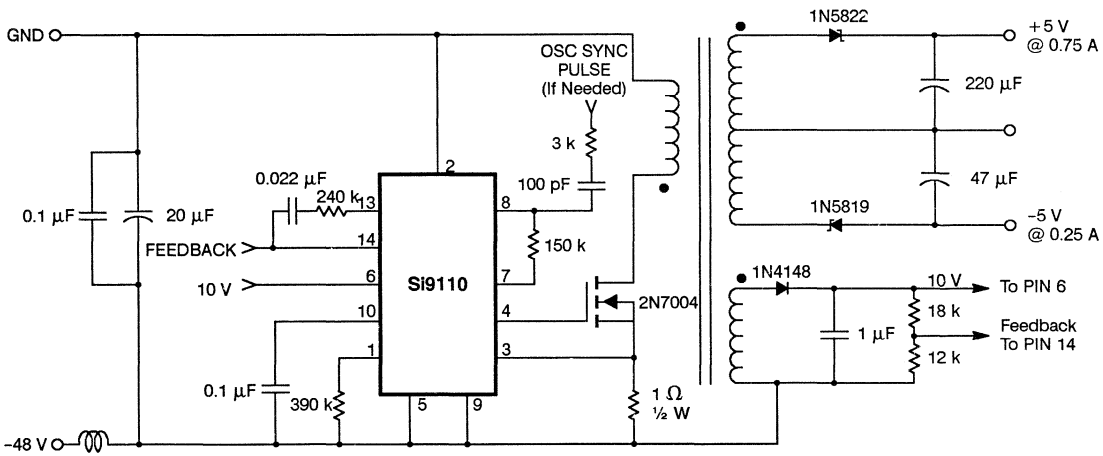
$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↓	L	OFF (Latched) (No Change)

OUTPUT DRIVER

The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469A. The D469A can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

APPLICATIONS

5-watt Power Supply for Telecom Applications



5

Si9112
High-Voltage Switchmode Controller

FEATURES

- 9 to 80 V Input Range
- Current-mode Control
- High-speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

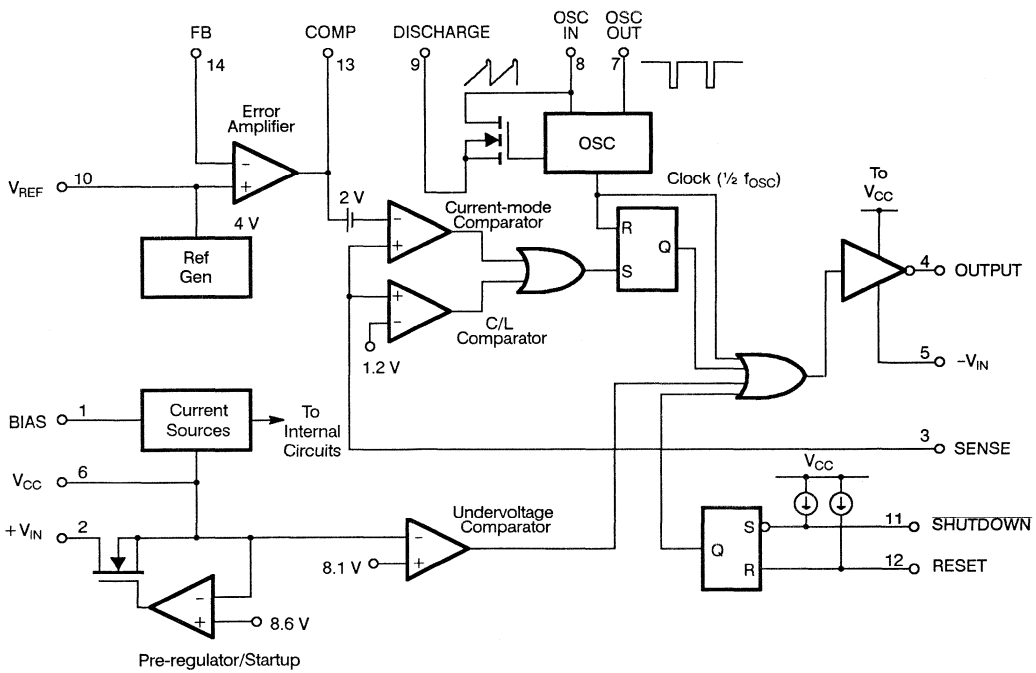
DESCRIPTION

The Si9112 is a BiC/DMOS integrated circuit designed for use in high-efficiency switchmode power converters. A high-voltage DMOS input allows this controller to work over a wide range of input voltages (9- to 80-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A CMOS output driver provides high-speed switching of MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9112 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9112 is available in 14-pin plastic DIP, and SO packages, and is specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 80 V
Logic Inputs
(RESET, SHUTDOWN, OSC IN) ..... -0.3 V to V_{CC} + 0.3 V
Linear Inputs
(FEEDBACK, SENSE) ..... -0.3 V to V_{CC} to 0.3 V
HV Preregulator Input Current (continuous) ..... 25 mA
(Power Dissipation Limited)
Storage Temperature (D Suffix) ..... -65 to 150°C
Operating Temperature (D Suffix) ..... -40 to 85°C

Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)*
14-Pin Plastic DIP (J Suffix)** ..... 750 mW
14-Pin SOIC (Y Suffix)*** ..... 900 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
14-Pin SOIC ..... 140°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 6 mW/°C above 25°C
***Derate 7.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9 V to 13.5 V
$+V_{IN}$ ..... 9 V to 80 V
f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} - 3 V
Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85°C 3 = -40°C	LIMITS D SUFFIX -40 to 85°C			UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	
REFERENCE							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	1 2,3[c]	4.0	3.88 3.82	4.12 4.14	V
Output Impedance[c]	Z_{OUT}		1	30	15	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	1	100	70	130	µA
Temperature Stability[c]	T_{REF}		2,3	0.1		0.25	mV/°C
OSCILLATOR							
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e	1	100	80	120	kHz
		R_{OSC} = 150 k, See Note e	1	200	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	9		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500	ppm/°C
ERROR AMPLIFIER							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	1	4.00	3.92	4.08	V
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	1	±15		±40	mV
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	1	25		500	nA
Open Loop Voltage Gain[c]	A_{VOL}	OSC IN = $-V_{IN}$	1	80	60		dB

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85°C 3 = -40°C TEMP		LIMITS D SUFFIX -40 to 85°C MIN[b]	 MAX[b]	UNIT
ERROR AMPLIFIER (Cont'd)							
Unity Gain Bandwidth[c]	BW	OSC IN = $-V_{IN}$ (OSC Disabled)	1	1.5	1		MHz
Dynamic Output Impedance[c]	Z_{OUT}	Error Amp Configured for 60 dB gain	1	1000		2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	1	-2.0		-1.4	mA
		Sink V_{FB} = 4.5 V	1	0.15	0.12		
Power Supply Rejection[c]	PSRR	9 V ≤ V_{CC} ≤ 13.5 V	1	70	50		dB
CURRENT LIMIT							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	1	1.2	1.0	1.4	V
Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1	1	100		150	ns
PREREGULATOR/STARTUP							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	1		80		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10	µA
Preregulator Dropout Voltage	V_{CC}	$+V_{IN}$ = 10 V, R_{LOAD} = 4 k at Pin 6	1		V_{UVLO} +0.1		V
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA	1	8.7	8.0	9.4	
Undervoltage Lockout	V_{UVLO}	See Detailed Description	1	8.1	7.2	8.9	
V_{REG} -V_{UVLO}	V_{DELTA}		1	0.6	0.3		
SUPPLY							
Supply Current	I_{CC}	C_L ≤ 75 pF (Pin 4)	1	0.6		1.0	mA
Bias Current	I_{BIAS}		1	15			µA
LOGIC							
$\overline{\text{SHUTDOWN}}$ Delay[c]	t_{SD}	C_L = 500 pF V_{SENSE} = $-V_{IN}$, See Figure 2	1	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[c]	t_{SW}	See Figure 3	1		50		
RESET Pulse Width[c]	t_{RW}		1		50		
Latching Pulse Width SHUTDOWN and RESET LOW[c]	t_{LW}		1		25		
Input LOW Voltage	V_{IL}		1			2.0	V
Input HIGH Voltage	V_{IH}		1		7.0		
Input Current Input Voltage HIGH	I_{IH}	V_{LOGIC} = V_{CC}	1	1		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	25	-35		

5

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85°C 3 = -40°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	
OUTPUT							
Output HIGH Voltage	V_{OH}	I_{OUT} = -10 mA	1 2,3		8.7 8.5		V
Output LOW Voltage	V_{OL}	I_{OUT} = 10 mA	1 2,3			0.3 0.5	
Output Resistance[c]	R_{OUT}	I_{OUT} = 10 mA Source or Sink	1 2,3	20 25		30 35	Ω
Rise Time[c]	t_r	C_L = 500 pF	1	40		75	ns
Fall Time[c]	t_f		1	40		75	

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = $\preceq$ 5 pF

TIMING WAVEFORMS

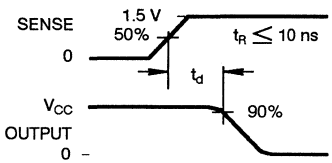


Figure 1

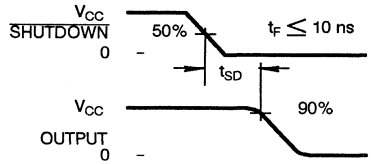


Figure 2

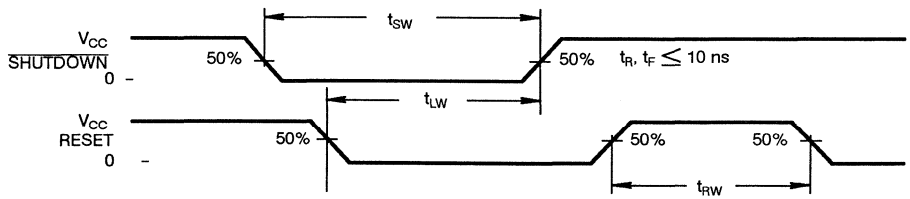


Figure 3

TYPICAL CHARACTERISTICS

Figure 4. $+V_{IN}$ vs. $+I_{IN}$ at Startup

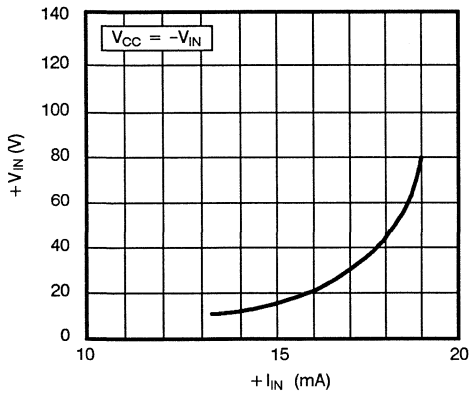
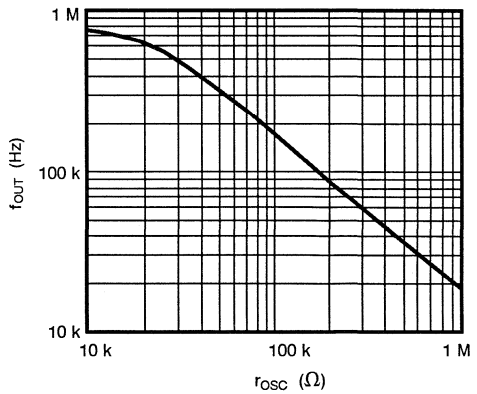
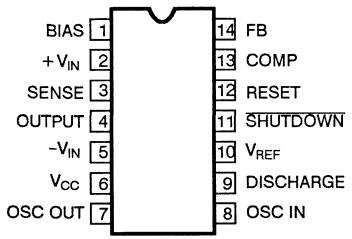


Figure 5. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

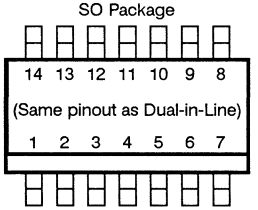
Dual-In-Line Package



Top View

Order Number:
Plastic: Si9112DJ

SO Package



Top View

Order Number:
Si9112DY

5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9112 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The charging current is disabled when V_{CC} exceeds 8.7 V. If V_{CC} is not forced to exceed the 8.7 V threshold, then V_{CC} will be regulated to a nominal value of 8.7 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the UV lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the preregulator circuit is disabled.

BIAS

To properly set the bias for the Si9112, a 270 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9112 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9112 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±2% of 4 V. This automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier. The emitter follower output has a typical dynamic output impedance of 1000 Ω, and is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNC pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

OUTPUT DRIVER

The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, and SMP25N06. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

NOTE: For applications information refer to AN88-3

Si9120
Universal Input Switchmode Controller

FEATURES

- 50 to 450 V Input Range
- Current-mode Control
- 125 mA Output Drive
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

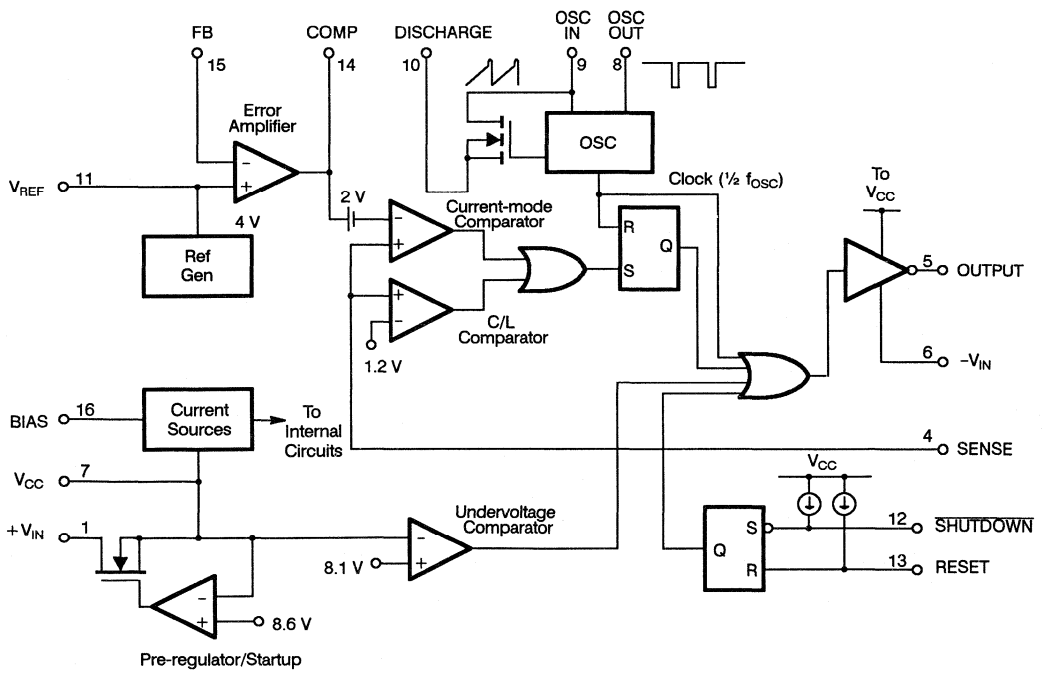
DESCRIPTION

The Si9120 is a BiC/DMOS integrated circuit designed for use in low-power, high-efficiency offline power supplies. High-voltage DMOS inputs allow the controller to work over a wide range of input voltages (50- to 450-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce quiescent current to less than 1.5 mA.

A CMOS output driver provides high-speed switching for MOSFET devices with gate charge, Q_g, up to 25 nC, enough to supply 30 W of output power at 100 kHz. These devices, when combined with an output MOSFET and transformer, can be used to implement single-ended power converter topologies (i.e., flyback and forward).

The Si9120 is available in a 16-pin plastic DIP package, and is specified over the industrial, D suffix (−40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 450 V
Logic Inputs (RESET
SHUTDOWN, OSC IN, OSC OUT) ..... -0.3 V to V_{CC} + 0.3 V
Linear Input
(FEEDBACK, SENSE, BIAS, V_{REF}) ..... -0.3 V to 7 V
HV Preregulator Input Current (continuous) ..... 5 mA*
Continuous Output Current (Source or Sink) ..... 125 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)**
16-Pin Plastic DIP (J Suffix)*** ..... 750 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic DIP ..... 167°C/W

*Continuous current may be limited by the applications maximum input voltage and the package power dissipation.
**Device mounted with all leads soldered or welded to PC board.
***Derate 6 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 50 V to 450 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} - 3 V
Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85°C 3 = -40°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	
REFERENCE							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	1 2,3	4.0	3.88 3.82	4.12 4.14	V
Output Impedance[c]	Z_{OUT}		1	30	15	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	1	100	70	130	µA
Temperature Stability[c]	T_{REF}		2,3	0.1		0.25	mV/°C
OSCILLATOR							
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e	1	100	80	120	kHz
		R_{OSC} = 150 k, See Note e	1	200	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	10		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500	ppm/°C
ERROR AMPLIFIER							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	1		3.92	4.08	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	1	25		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$	1	±15		±40	mV
Open Loop Voltage Gain[c]	A_{VOL}	OSC IN = $-V_{IN}$	1	80	60		dB

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	LIMITS 1 = 25°C 2 = 85°C 3 = -40°C TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
ERROR AMPLIFIER (Cont'd)							
Unity Gain Bandwidth[c]	BW	OSC IN = $-V_{IN}$	1	1.5	1.0		MHz
Dynamic Output Impedance[c]	Z_{OUT}	Error Amp configured for 60 dB gain	1	1000		2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	1	-2.0		-1.4	mA
		Sink V_{FB} = 4.5 V	1	0.15	0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	1	70	50		dB
CURRENT LIMIT							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	1	1.2	1.0	1.4	V
Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1	1	100		150	ns
PREREGULATOR/STARTUP							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	1		450		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10	µA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA	1	8.6	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}		1	8.1	7.0	8.9	
V_{REG} - V_{UVLO}	V_{DELTA}		1	0.6	0.3		
SUPPLY							
Supply Current	I_{CC}	C_L = 500 pF at Pin 5	1	0.85		1.5	mA
Bias Current	I_{BIAS}		1	15	10	20	µA
LOGIC							
$\overline{\text{SHUTDOWN}}$ Delay[c]	t_{SD}	C_L = 500 pF, V_{SENSE} = $-V_{IN}$ See Figure 2	1	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[c]	t_{SW}	See Figure 3	1		50		
RESET Pulse Width[c]	t_{RW}		1		50		
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW[c]	t_{LW}		1		25		
Input LOW Voltage	V_{IL}		1			2.0	V
Input HIGH Voltage	V_{IH}		1		8.0		
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		

5

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85°C 3 = -40°C TEMP	TYP[d]	LIMITS D SUFFIX -40 to 85°C MIN[b]	MAX[b]	UNIT
OUTPUT							
Output HIGH Voltage	V_{OH}	I_{OUT} = -10 mA	1 2,3		9.7 9.5		V
Output LOW Voltage	V_{OL}	I_{OUT} = 10 mA	1 2,3			0.3 0.5	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA Source or Sink	1 2,3	20 25		30 35	Ω
Rise Time	t_r	C_L = 500 pF	1	40		75	ns
Fall Time	t_f		1	40		75	

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 9 = $\leq$ 5 pF

TIMING WAVEFORMS

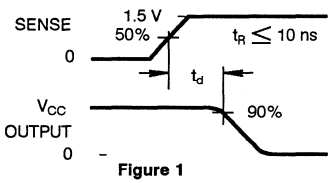


Figure 1

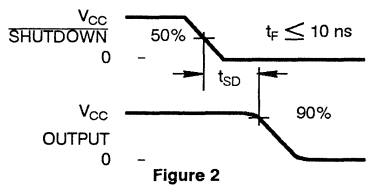


Figure 2

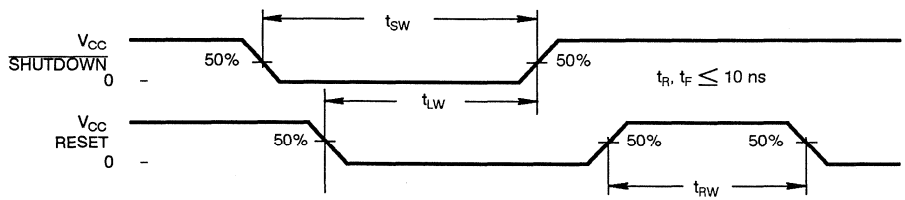
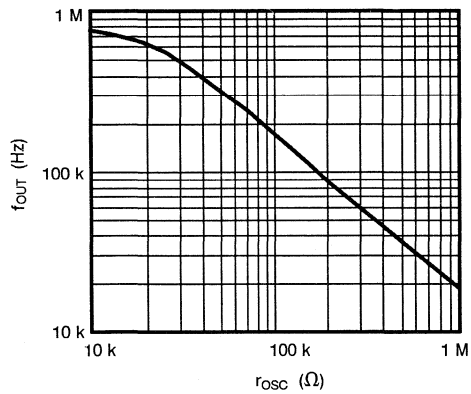


Figure 3

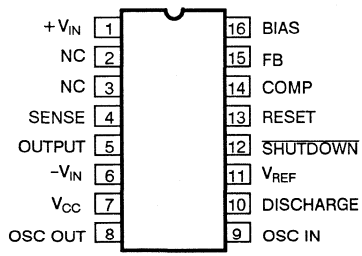
TYPICAL CHARACTERISTICS

Figure 4. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package



Top View

Order Number:
Plastic: Si9120DJ

5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9120 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 1) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET which is connected between $+V_{IN}$ and V_{CC} (pin 7). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: When driving large MOSFETs at high frequency without a bootstrap V_{CC} supply, power dissipation in the pre-regulator may exceed the power rating of the IC package.

BIAS

To properly set the bias for the Si9120, a 390 kΩ resistor should be tied from BIAS (pin 16) to $-V_{IN}$ (pin 6). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9120 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9120 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±2% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for high input impedance.The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 4 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 12) and RESET (pin 13) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET. $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

OUTPUT DRIVER

The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the IRF820, BUZ78 or BUZ80. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

NOTE: For applications information refer to AN90-2 and AN90-8.

Si9200
CAN Bus Driver

FEATURES

- Survives Shorts and Transients on Multiplexed Bus in Automotive Applications
- Single Power Supply
- Compatible with Intel 82526 CAN Controller
- Direct Interface – No External Components Required

APPLICATION

- Two Wire Multiplexer Interface

END PRODUCTS

- Automobiles
- Trucks
- Tractors
- Industrial Controls

DESCRIPTION

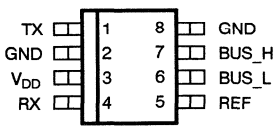
The Si9200 is designed to interface between the Intel 82526 CAN Controller and the physical bus to provide drive capability to the bus and differential receive capability to the controller. It is designed to operate reliably over the extended temperature range, absorb typical electrical transients on the bus which may occur in an automotive or industrial application, and protect itself against any abnormal bus conditions.

The Si9200 is built using the Siliconix D/CMOS process. This process supports CMOS, DMOS, and isolated bipolar transistors and uses an epitaxial layer to prevent latchup. The bus line pins are diode protected and can be driven beyond the V_{DD} to ground range.

The Si9200 is offered in the space efficient 8-pin high-density surface mount plastic package.

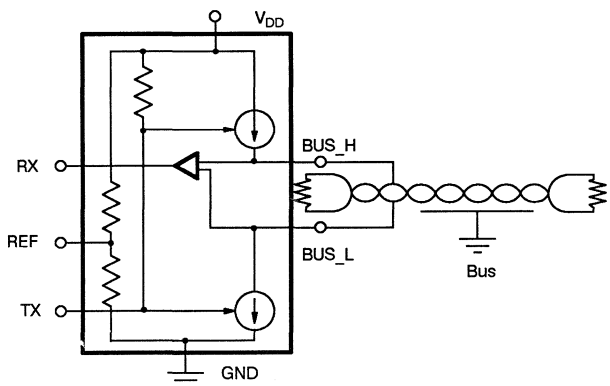
PIN CONFIGURATION/FUNCTIONAL BLOCK DIAGRAM

SO Package



Top View

Order Number:
Si9200AY



TRUTH TABLE

TX	BUS_H	BUS_L	Bus State
0	High	Low	Dominant
1 (or Floating)	Floating	Floating	Recessive

Siliconix incorporated

Si9901
Adaptive Power MOSFET Driver With 500-V Level Shift

FEATURES

- 500-V Translation Outputs to Control High-Side Drive
- dv/dt and di/dt Control
- Undervoltage Protection
- Short-Circuit Protection
- Low Quiescent Current
- CMOS Compatible Inputs
- Compatible with Wide Range of MOSFET Devices
- Bootstrap and Charge-Pump Compatible (High-Side Drive)

APPLICATIONS

- Motor Drives
- Power Supplies
- Solid State Relays

END PRODUCTS

- Washing Machines
- Fans/Blowers
- Air Conditioning
- Industrial Controllers
- Refrigerators

DESCRIPTION

This low-side power MOSFET driver complements the Si9911/Si9914 Adaptive power MOSFET drivers to complete a high voltage half-bridge logic to power interface. It provides optimized gate drive signals, protection circuitry and logic level interface. Low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. Internal charge-pump and bootstrap circuitry using external capacitors and high voltage level translation outputs provide control and power for the complete high voltage half-bridge function with minimal external components.

Undervoltage lockout feature ensures sufficient MOSFET gate voltage. An output short circuit condition immediately disables the half-bridge and indicates a fault condition. Addition of one external resistor limits maximum di/dt of the external lowside power MOSFET. Addition of one external capacitor limits maximum dv/dt.

This driver is available in 16-pin plastic DIP and SOIC packages, and is specified over the industrial D suffix (-40 to 85°C) temperature range.

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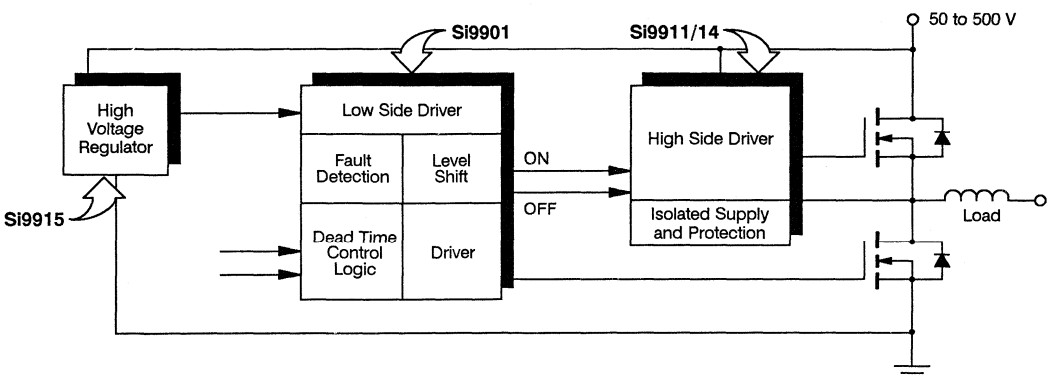
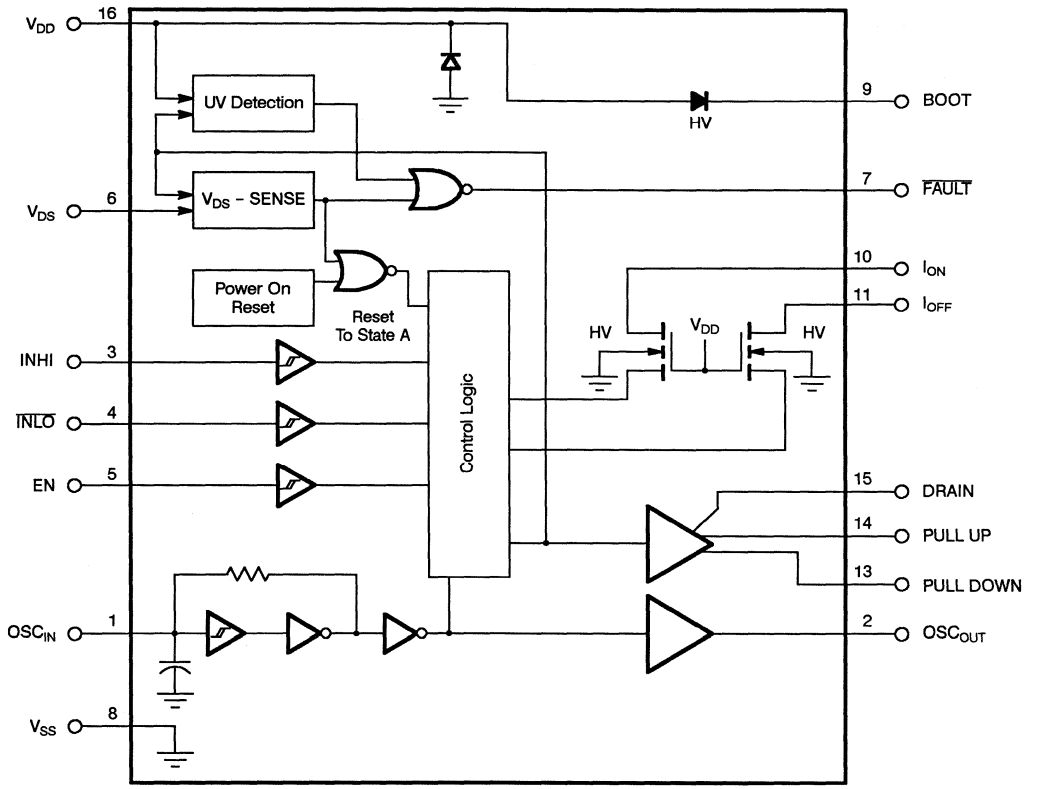
SYSTEM BLOCK DIAGRAM



Advance Information

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

STATE	NEXT STATE FOR INPUTS HLE 111	HLE 001	HLE 011	HLE 101	HLE 110	HLE 000	HLE 010	HLE 100	LOW-SIDE OUTPUTS PU to V_{DD}	PD to V_{SS}	WIRED OR PU + PD	HIGH-SIDE LEVEL SHIFTS I_{ON} HV n-Ch to V_{SS}	I_{OFF} HV n-Ch to V_{SS}
A	B	B	B	B	B	B	B	B	Float	ON	Toward V_{SS}	OFF - Float	ON ≈ 0.3 mA
B	C	C	C	C	C	C	C	C	Float	ON	Toward V_{SS}	OFF - Float	BOOST≈3 mA
C	C	D	C	C	C	C	C	C	Float	ON	Toward V_{SS}	OFF - Float	ON ≈ 0.3 mA
D	E	E	E	E	E	E	E	E	ON	Float	Toward V_{DD}	OFF - Float	ON ≈ 0.3 mA
E	F	E	F	F	F	F	F	F	ON	Float	Toward V_{DD}	OFF - Float	ON ≈ 0.3 mA
F	G	G	G	G	B	B	B	B	Float	ON	Toward V_{SS}	OFF - Float	ON ≈ 0.3 mA
G	H	H	G	G	B	B	B	B	Float	ON	Toward V_{SS}	OFF - Float	ON ≈ 0.3 mA
H	I	I	I	I	I	I	I	I	Float	ON	Toward V_{SS}	BOOST≈3 mA	OFF - Float
I	I	J	J	J	J	J	J	J	Float	ON	Toward V_{SS}	ON ≈ 0.3 mA	OFF - Float
J	K	K	K	K	B	B	B	B	Float	ON	Toward V_{SS}	OFF - Float	BOOST≈3 mA
K	D	D	K	K	B	B	B	B	Float	ON	Toward V_{SS}	OFF - Float	ON ≈ 0.3 mA

Inputs: H = INHI L = $\overline{\text{INLO}}$ E = EN PU = PULL UP PD = PULL DOWN

Si9905/Si9912/Si9915
Off Line Voltage Regulators

FEATURES

- Line Regulation ±2% @ 50-450 V
- Load Regulation ±1% @ 0-20 V
- Thermal Shutdown
- Standard TO-220 and SO-8
- Short Circuit Protected

APPLICATIONS

- Motor Drives
- Power Supplies
- Isolated Sensors
- Solid State Relays

END PRODUCTS

- Appliances
- Fans/Blowers
- Air Conditioning
- Industrial Controllers
- Industrial Sensors

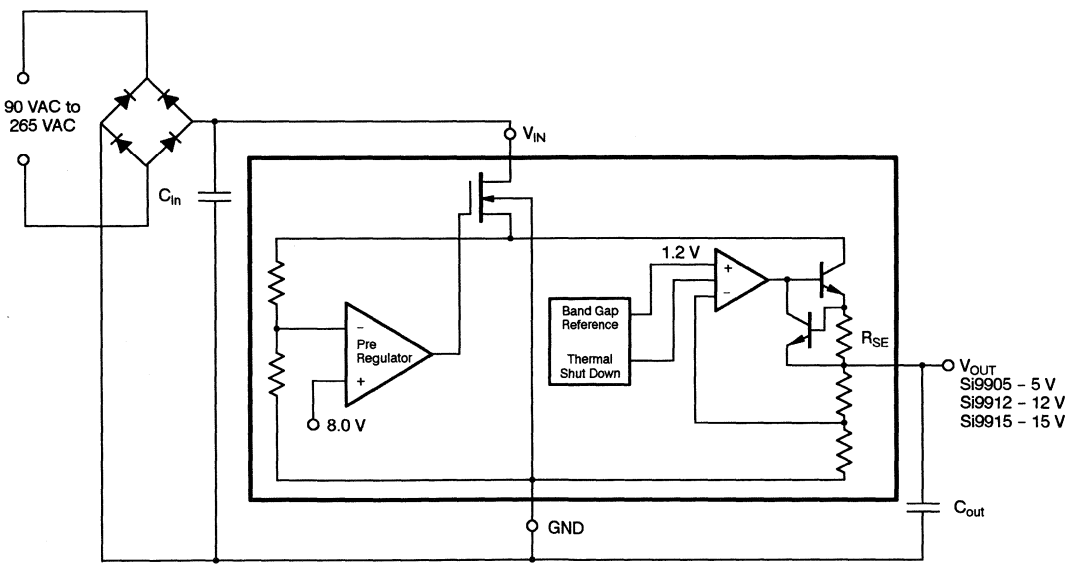
DESCRIPTION

The Si9905/Si9912/Si9915 are low power, three terminal linear regulators designed to operate directly from rectified 90 to 265 VAC sources and provide outputs of 5 V, 12 V and 15 V respectively. The family of three output voltages allow the regulators to be used in a wide range of applications.

A high voltage depletion mode, pre-regulator allows for the wide power supply input range. Additional features which include short circuit protection, over temperature protection and ESD protection allow for safe operation of the IC.

The Si9905/Si9912/Si9915 are available in standard TO-220 and SO-8 packages and are specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



5

Siliconix incorporated

Si9910
Adaptive Power MOSFET Driver[1]

FEATURES

- dv/dt and di/dt Control
- Undervoltage Protection
- Short-circuit Protection
- t_{rr} Shoot-through Current Limiting
- Low Quiescent Current
- CMOS Compatible Inputs
- Compatible with Wide Range of MOSFET Devices
- Bootstrap and Charge Pump Compatible (High-side Drive)

DESCRIPTION

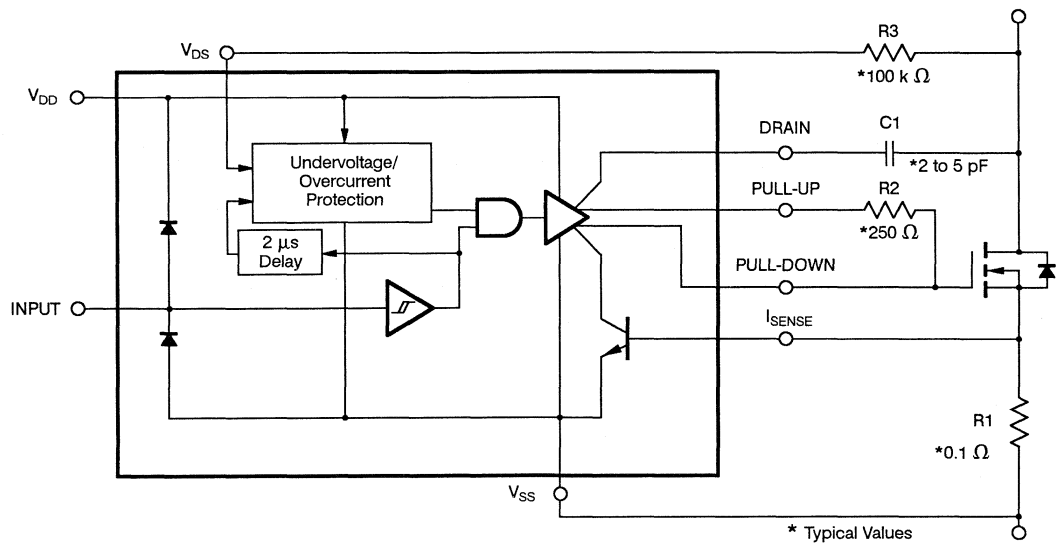
The Si9910 POWER MOSFET driver provides optimized gate drive signals, protection circuitry and logic level interface. Very low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. This efficiency allows operation in high-voltage bridge applications with "bootstrap" or "charge-pump" floating power supply techniques.

The non-inverting output configuration minimizes current drain for an n-channel "on" state. The logic input is internally diode clamped to allow simple pull-down in high-side drives.

Fault protection circuitry senses an undervoltage or output short-circuit condition and disables the power MOSFET. Addition of one external resistor limits maximum di/dt of the external Power MOSFET. A fast feedback circuit may be used to limit shoot-through current during t_{rr} (diode reverse recovery time) in a bridge configuration.

The Si9910 is available in 8-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (−40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



[1]Covered by Patent Number 484116.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{ss} Pin
V_{DD} Supply Range ..... -0.3 V to 18 V
Pin 1, 4, 5, 7, 8 ..... -0.3 V to V_{DD} + 0.3 V
Pin 2 ..... -0.7 V to V_{DD} + 0.3 V
Input Current ..... ±20 mA
Storage Temperature (D Suffix) ..... -65 to 150°C
Peak Current (I_{pk}) 1A

Operating Temperature (D Suffix) ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)
8-Pin SOIC (Y Suffix)* ..... 700 mW
8-Pin Plastic DIP (J Suffix)* ..... 700 mW

*Derate 5.6 mW/°C above 25°C

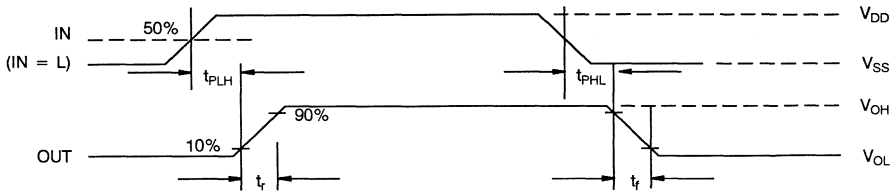
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V_{DD} 10.8 V to 16.5 V T_A = OperatingTemperature Range	LIMITS TYP[d]	LIMITS MIN[b]	LIMITS MAX[b]	UNIT
INPUT						
High Level Input Voltage	V_{IH}		7.4	0.75 x V_{DD}		V
Low Level Input Voltage	V_{IL}		6.0		0.25 x V_{DD}	V
Input Voltage Hysteresis	V_h		1.45	0.90	2.0	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}			±1	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V			±1	µA
OUTPUT						
High Level Output Voltage	V_{OH}	I_{OH} = -200 mA	10.7	V_{DD} -3		V
Low Level Output Voltage	V_{OL}	I_{OL} = 200 mA	1.3		3	V
Undervoltage Lockout	V_{UVLO}		9.2	8.3	10.2	V
I_{SENSE}	V_{TH}	I_S = 2 mA	0.8		1.0	V
Voltage Drain-Source Maximum	V_{DS}	Input HIGH	9.4	8.3	10.2	V
Input Current for V_{DS} Input	I_{VDS}		10			µA
Peak Output Source Current	I_{OS+}		1			A
Peak Output Sink Current	I_{OS-}		-1			A
SUPPLY						
Supply Range	V_{DD}			10.2	16.5	V
Supply Current	I_{DD1}	Output HIGH, No Load	0.1		1	µA
	I_{DD2}	Output LOW, No Load	100		500	µA
DYNAMIC						
Propagation Delay Time Low to High Level	t_{PLH}	C_L = 2000 pF	120			ns
Propagation Delay Time High to Low Level	t_{PHL}		135			ns
Rise Time	t_r		50			ns
Fall Time	t_f		35			ns
Overcurrent Sense Delay (V_{DS})	t_{DS}		1			µS
Input Capacitance	C_{in}		5			pF

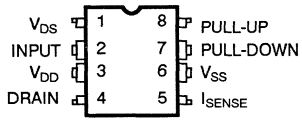
SPECIFICATIONS[a] (Cont'd)

[a]Refer to PROCESS OPTION FLOWCHART in the Siliconix data book for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY at T_A = 25°C, not guaranteed nor subject to production testing.

AC TESTING CONDITIONS

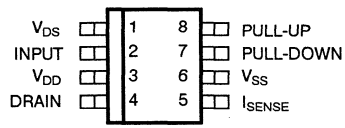


PIN CONFIGURATION



8-LEAD MOLDED DIP

Order Number:
SI9910DJ



8-LEAD SO

Order Number:
SI9910DY

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PIN DESCRIPTION

Pin 1 (V_{DS})

Pin 1 or V_{DS} is a sense input for the maximum source-drain voltage ($V_{DS(MAX)}$) limit. Two microseconds after a high transition on input pin 2, an internal timer enables the $V_{DS(max)}$ sense circuitry. A catastrophic overcurrent condition, excessive on-resistance, or insufficient gate-drive voltage can be sensed by limiting the maximum voltage drop ($V_{DS(MAX)}$) across the power MOSFET. An external resistor (R3) is required to protect pin 1 from overvoltage during the MOSFET "off" condition. Exceeding $V_{DS(max)}$ latches the Si9910 "off." Drive is re-enabled on the next positive- going input on pin 2. If pin 1 is not used, it must be connected to pin 6 (V_{SS}).

Pin 2 (INPUT)

A non-inverting, Schmidt trigger input controls the state of the MOSFET gate-drive outputs and enables the protection logic. When the input is low ($\leq V_{IL}$), V_{DD} is monitored for an undervoltage condition (insufficiently charged bootstrap capacitor). If an undervoltage ($\leq V_{DD(MIN)}$) condition exists, the driver will ignore a turn-on input signal. An undervoltage ($\leq V_{DD(MIN)}$) condition during an "on" state will not be sensed.

PIN DESCRIPTION (Cont'd)

Pin 3 (V_{DD})

V_{DD} supplies power for the driver's internal circuitry and charging current for the power MOSFET's gate capacitance. The Si9910 minimizes the internal I_{DD} in the "on" state (gate-drive outputs high) allowing a "floating" power supply to be provided by charge pump or bootstrap techniques.

Pin 4 (DRAIN)

Drain is an analog input to the internal dv/dt limiting circuitry. An external capacitor (C1) must be used to protect the input from exposure to the high-voltage ("off" state) drain and to set the power MOSFET's maximum rate of dv/dt. If dv/dt feedback is not used, pin 4 must be left open.

Pin 5 (I_{SENSE})

I_{SENSE} in combination with an external resistor (R_1) protects the power MOSFET from potentially catastrophic peak currents. I_{SENSE} is an analog feedback that limits current during the power MOSFET's transition to an "on" state. It is intended to protect power MOSFETs (in a half-bridge arrangement) from "shoot-through" current, resulting from excess di/dt and t_{rr} of flyback diodes or from logic timing overlap. A 0.8 volt drop across (R1) should indicate a current level that is approximately four times the maximum allowable load current. When the I_{SENSE} input is not used, it should be tied to pin 6 (V_{SS}).

Pin 6 (V_{SS})

V_{SS} is the driver's ground return pin. The applications diagram illustrates the connection of V_{SS} for source-referenced "floating" applications (half-bridge, high-side) and ground-referenced applications (half-bridge, low-side).

Pin 7 (PULL-DOWN)/Pin 8 (PULL-UP)

Pull-up and pull-down outputs collectively provide the power MOSFET gate with charging and discharging currents. Turn "on" or "off" di/dt can be limited by adding resistance (R_2) in series with the appropriate output.

TYPICAL APPLICATION

The Si9910 in "Floating" High-Side Drive Applications

As demonstrated in Figure 1, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 permit its use in half-bridge high-side drive applications.

A simple and inexpensive method of isolating a floating supply to power the Si9910 in high-side driver applications had to be provided. Therefore, the Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses and the charge pump circuit provides static operation.

The Si9910 is configured to take advantage of either floating supply technique if the application is not sensitive to their particular limitations, or both techniques if switching losses must be minimized and static operation is necessary. The schematic above illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

Input signal level shifting is accomplished with a passive pull-up (R4) and the Siliconix VN50300 (500-volt/300 Ω) MOSFET for pull-down in applications below 500 V. Complete specifications for the VN50300 can be found in the Siliconix Low-Power Discretes Data Book. One of the VN50300's most important features in this application is its extremely low C_{oss} (output or drain) capacitance. C_{oss} (typically 5 pF), plus the Si9910's input capacitance (also typically 5 pF) plus any stray board capacitance. Total node capacitance defines the value of R4 needed to guarantee an input transition rate which safely exceeds the maximum dv/dt rate of the output half-bridge. Another feature of the VN50300 is its inherently low saturation current. Using level-shift devices with higher current capabilities may necessitate the addition of current-limiting components such as R5.

TYPICAL APPLICATION (Cont'd)

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, care must be taken to ensure time is available to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As a catastrophic protection against abnormal conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate. For more details, please refer to Application Note 89-5.

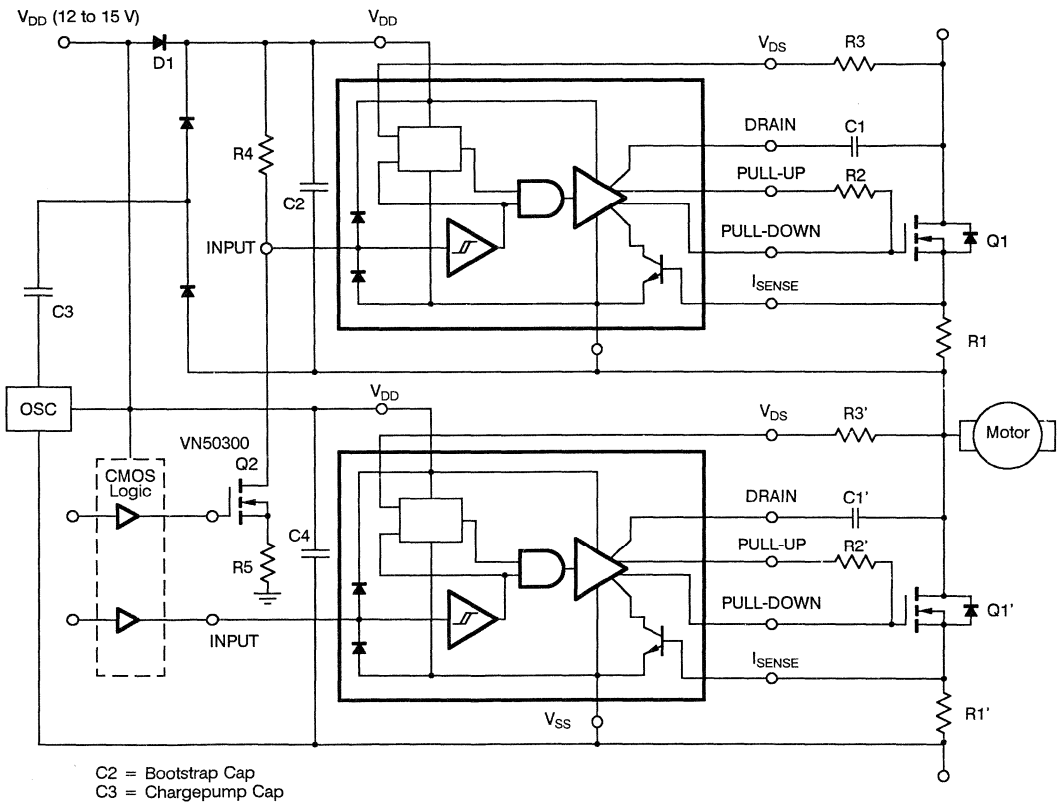


Figure 1. High-Voltage Half-Bridge with Si9910 Drivers

Siliconix incorporated

Si9911/Si9914
Adaptive Power MOSFET Drivers

FEATURES

- dv/dt and di/dt Control
- Latched Inputs
- Low Quiescent Current
- Undervoltage, Short-circuit Protection
- Bootstrap and Charge-pump Compatible (High-side Drive)

APPLICATIONS

- Motor Drives
- Power Supplies
- Solid State Relays

END PRODUCTS

- Washing Machines
- Fans/Blowers
- Air Conditioning
- Industrial Controllers
- Refrigerators

DESCRIPTION

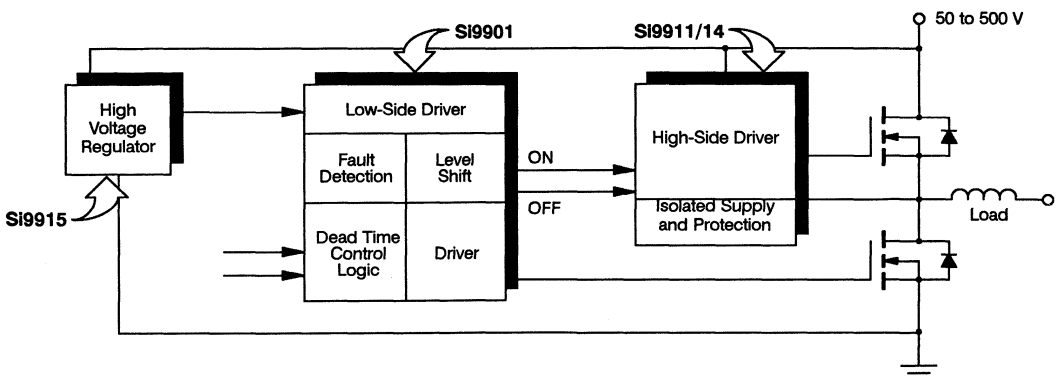
The Si9911/Si9914 POWER MOSFET drivers provide optimized gate drive signals, protection circuitry, and logic level interface. Very low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. This efficiency allows operation in high-voltage bridge applications from a "bootstrap" floating power supply. The Si9914 includes charge pump diodes to supplement the bootstrap supply.

Undervoltage lockout feature ensures sufficient MOSFET gate voltage. An output short circuit condition immediately disables the half-bridge and indicates a fault condition. Addition of one external resistor limits maximum di/dt of the external Power MOSFET. The Si9911/Si9914 is ideally suited to interface with our Si9901 for half-bridge circuits.

The Si9911 and Si9914 are available in 8-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (–40 to 85°C) temperature range.

* Covered by patent Number 4841166

SYSTEM BLOCK DIAGRAM



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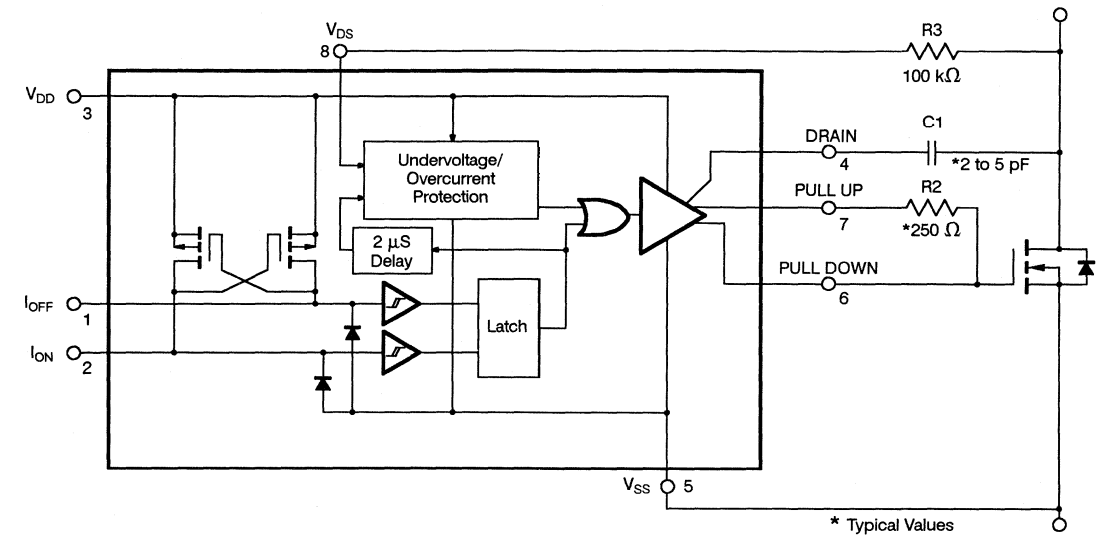
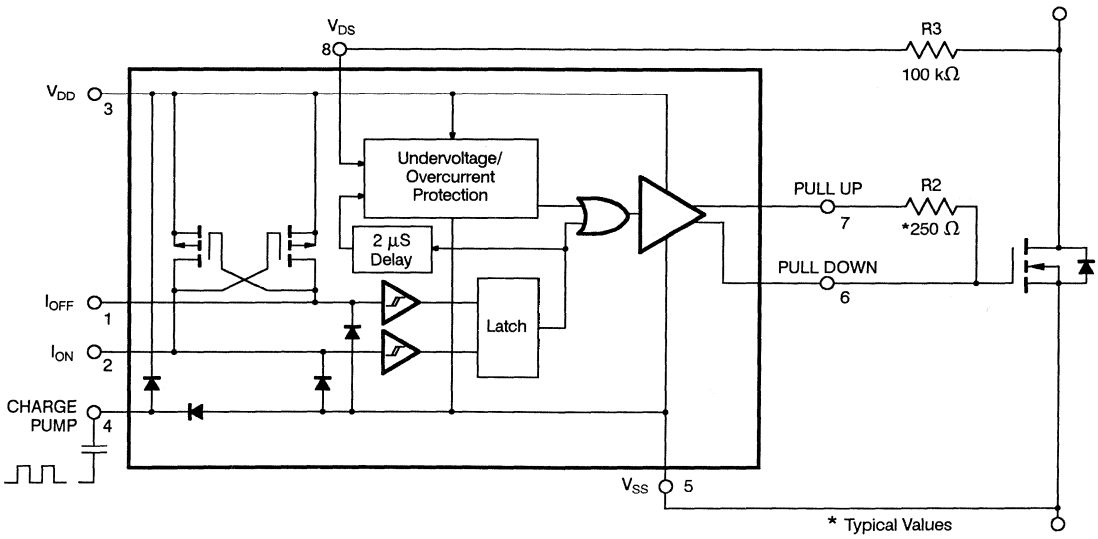
FUNCTIONAL BLOCK DIAGRAM – Si9911



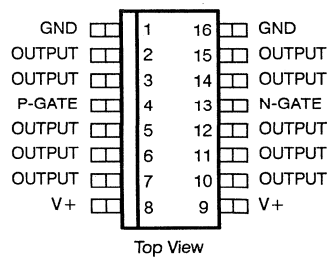
FUNCTIONAL BLOCK DIAGRAM – Si9914



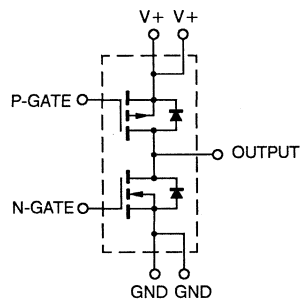
Si9950DY

Complementary MOSFET Half-Bridge

SO PACKAGE



Top View



PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N- or P-Channel	50	0.30	2.0

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N- OR P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	2.0	A
	T_A = 100°C		1.3	
Pulsed Drain Current[1]		I_{DM}	8	
Maximum Power Dissipation	T_A = 25°C	P_D	2.3	W
	T_A = 100°C		0.90	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient (Surface Mounted)	R_{thJA}	30	55	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T_J = 25°C Unless Otherwise Noted)
N- and P-Channel Devices (Negative Signs for P-Channel Device Omitted for Clarity)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch P-Ch		2.0 1.5	4.0 4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V			2.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1 A				0.3	Ω
		V_{GS} = 5 V, I_D = 0.5 A				1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1 A	N-Ch P-Ch	1.1 1.4	0.8 1.0		S
DYNAMIC							
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	N-Ch P-Ch	170 530		300 600	pF
Output Capacitance	C_{oss}		N-Ch P-Ch	90 270		200 350	
Reverse Transfer Capacitance	C_{rss}		N-Ch P-Ch	12 85		100 100	
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2 A	N-Ch P-Ch	3.7 17		6.0 26	nC
Gate-Source Charge[2]	Q_{gs}		N-Ch P-Ch	1 2.3			
Gate-Drain Charge[2]	Q_{gd}		N-Ch P-Ch	1.2 8.5			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	N-Ch P-Ch	7 10		20 20	ns
Rise Time[2]	t_r		N-Ch P-Ch	13 25		30 50	
Turn-Off Delay Time[2]	$t_{d(off)}$		N-Ch P-Ch	18 65		40 100	
Fall Time[2]	t_f		N-Ch P-Ch	13 60		25 100	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					2.0	A
Pulsed Current[3]	I_{SM}					8	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI/dt = 100 A/µs		70		100	ns

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data).

Figure 1. Output Characteristics

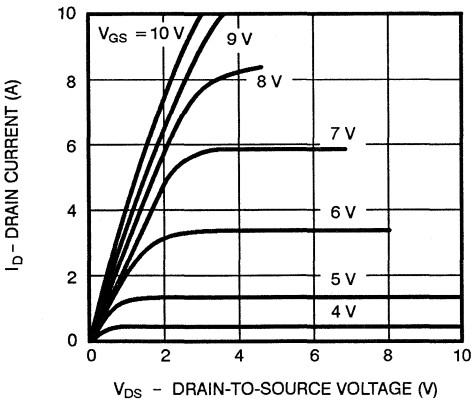


Figure 2. Transfer Characteristics

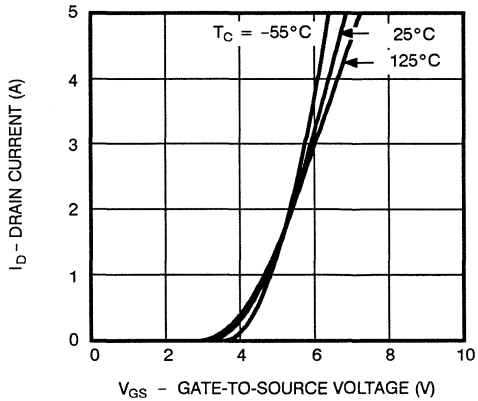


Figure 3. Transconductance

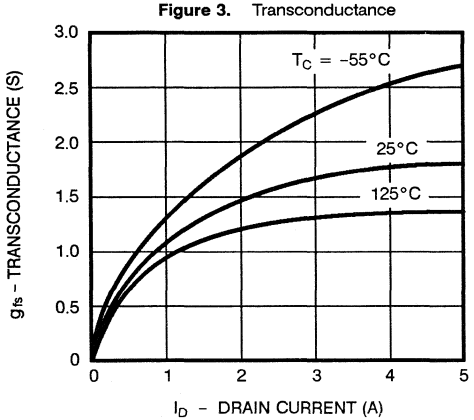


Figure 4. On-Resistance

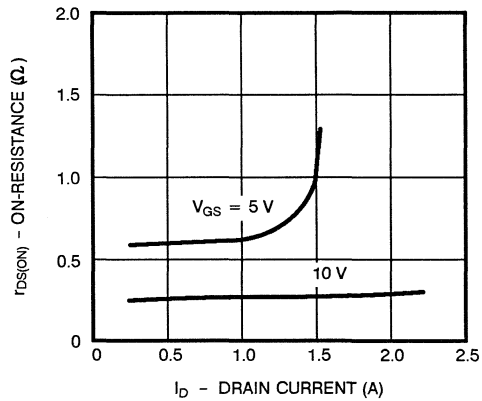


Figure 5. Capacitance

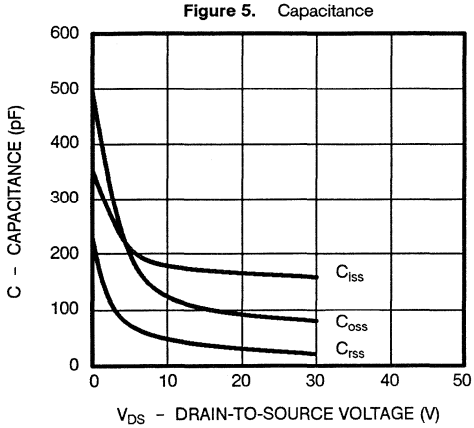


Figure 6. Gate Charge

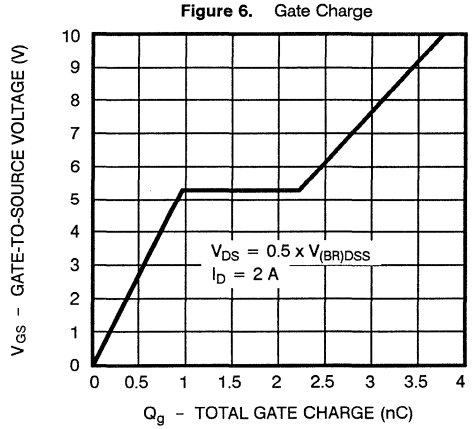


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Figure 7. On-Resistance vs. Junction Temperature

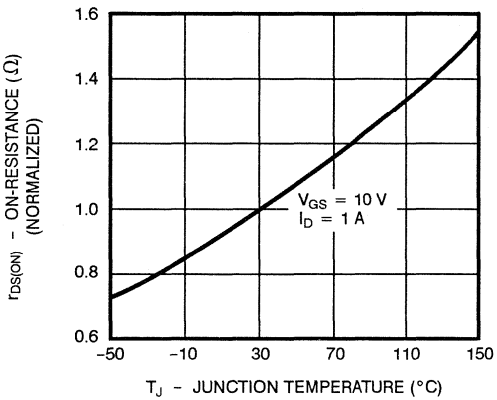
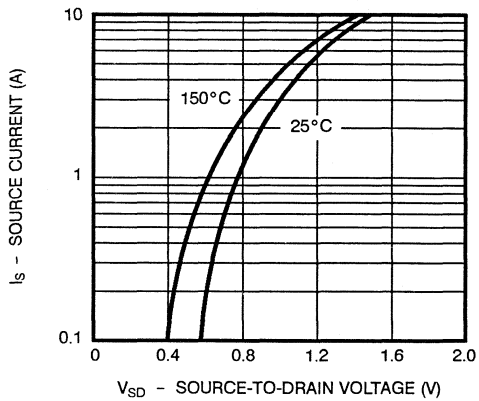


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

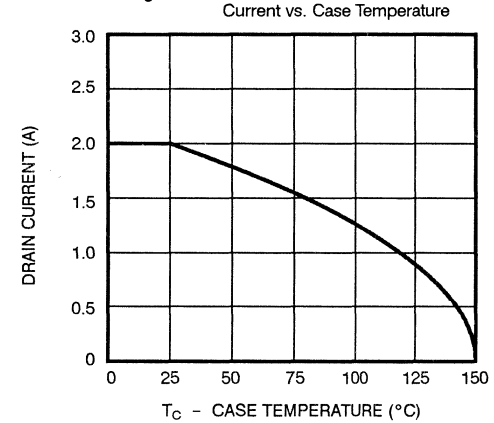


Figure 10. Safe Operating Area

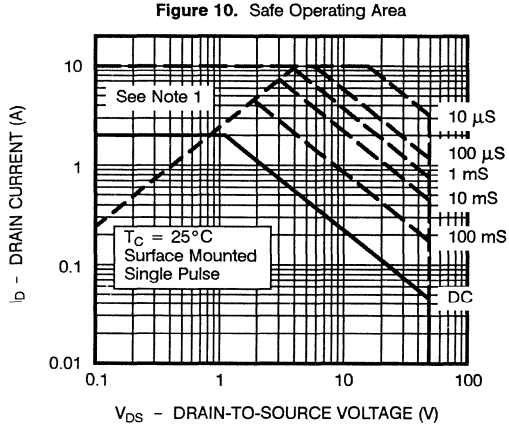


Figure 11. Normalized Effective Transient Thermal Impedance, Juntion-to-Ambient

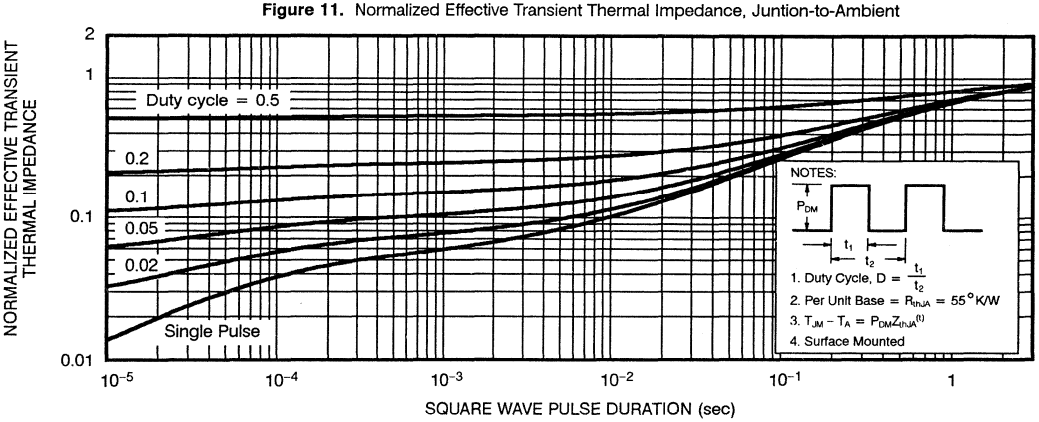


Figure 1. Output Characteristics

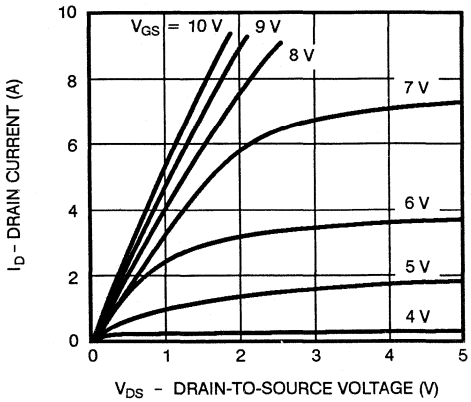


Figure 2. Transfer Characteristics

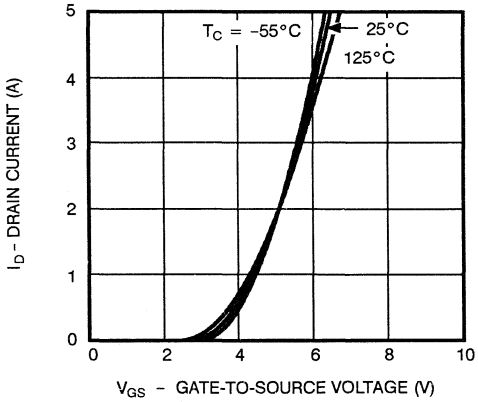


Figure 3. Transconductance

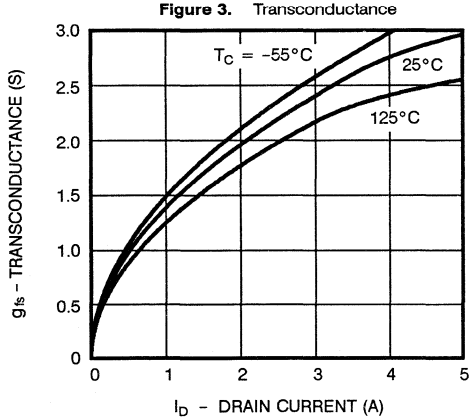


Figure 4. On-Resistance

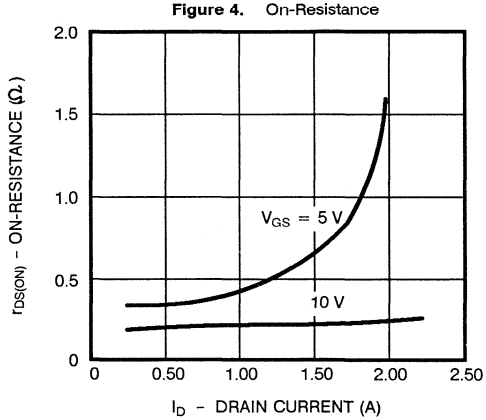


Figure 5. Capacitance

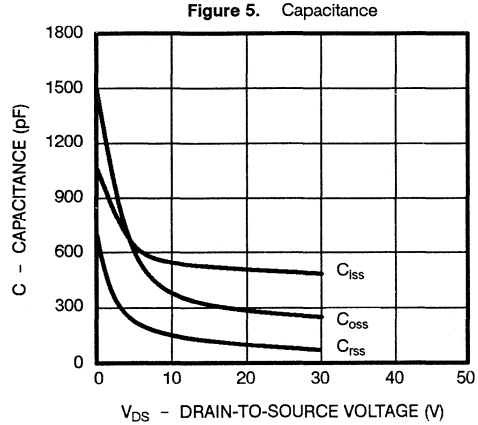


Figure 6. Gate Charge

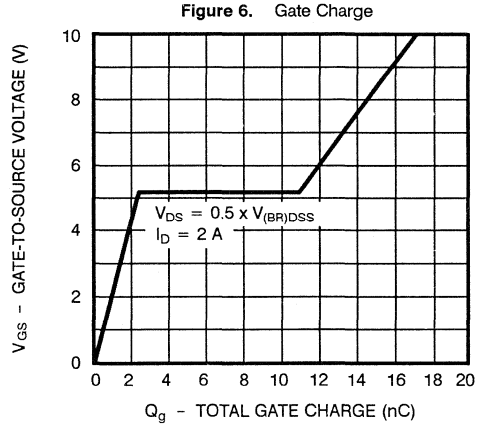


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Figure 7. On-Resistance vs. Junction Temperature

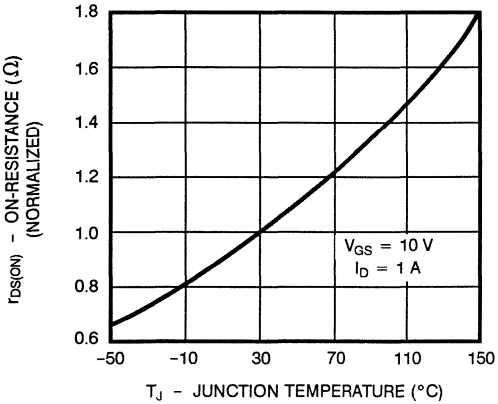
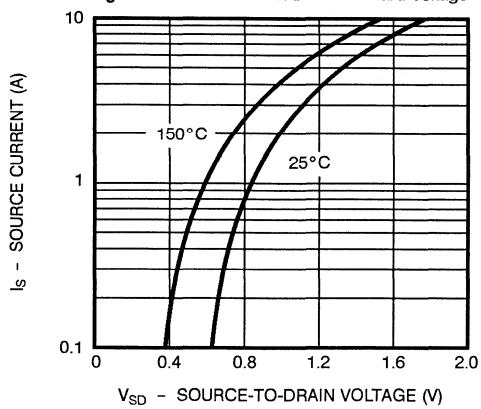


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

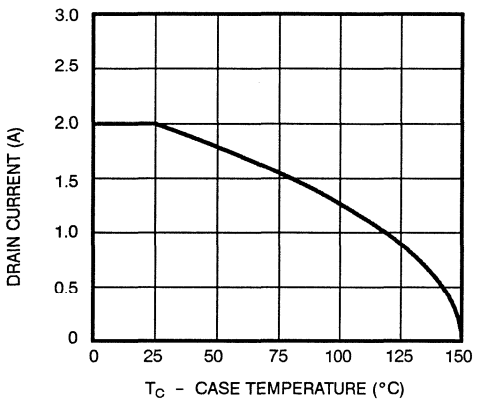
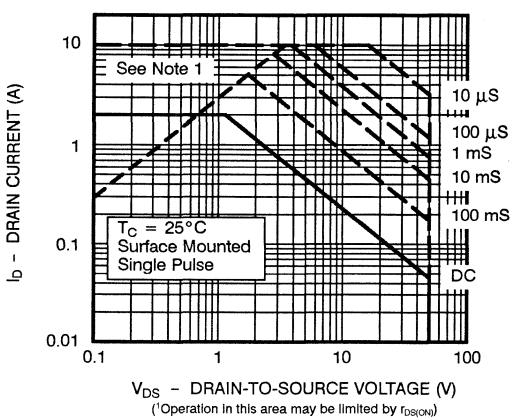
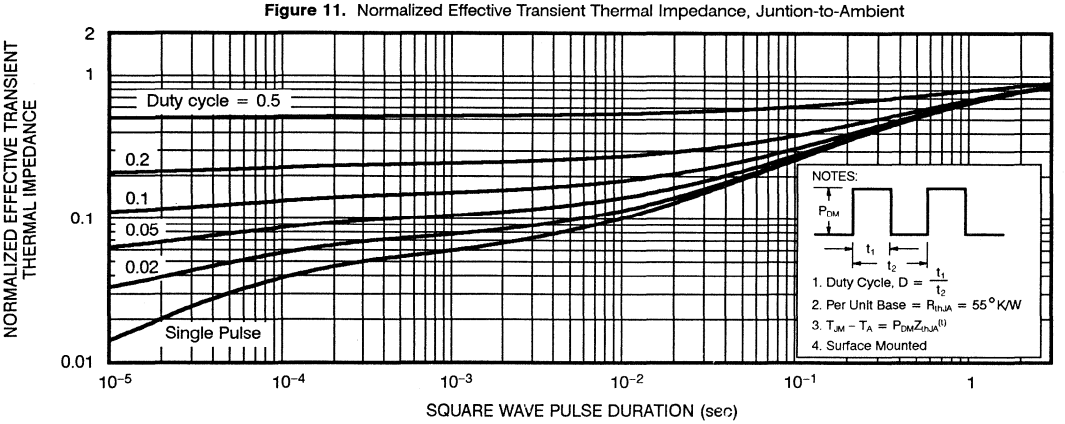


Figure 10. Safe Operating Area



(1)Operation in this area may be limited by $r_{DS(ON)}$

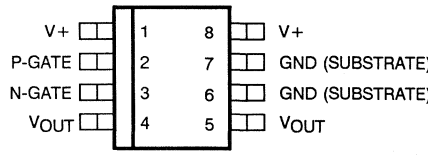
Figure 11. Normalized Effective Transient Thermal Impedance, Juntion-to-Ambient



Si9951DY

Integrated Complementary MOSFET Half-Bridge

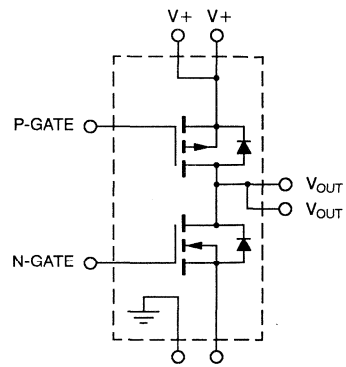
SO PACKAGE



Top View

PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	16.5	0.6	1.5
P-Channel[2]	16.5	0.7	1.5



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N- OR P-CHANNEL[2]	UNITS
Drain-Source Voltage		V_{DS}	18	V
Gate-Source Voltage		V_{GS}	GND – 0.3 to (V+) + 0.3	
Continuous Drain Current	T_A = 25°C	I_D	1.5	A
	T_A = 100°C		0.7	
Pulsed Drain Current[1]		I_{DM}	6	
Maximum Power Dissipation	T_A = 25°C	P_D	2	W
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	N- OR P-CHANNEL	UNITS
Maximum Junction-to-Ambient (Surface Mounted)	R_{thJA}	62.5	K/W

[1]Pulse width limited by maximum junction temperature.
[2]Negative signs omitted for clarity

SPECIFICATIONS (T_J = 25°C Unless Otherwise Noted)
N- and P-Channel Device (Negative Signs for P-Channel Device Omitted for Clarity)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP[4]	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			16.5		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch P-Ch		0.5 0.8	2 2	V
Gate Leakage	$I_{GATE(N)}$	$V_{GATE(P)}$ = V+ = 12 V, GND = 0 V, $V_{GATE(N)}$ = 0 V, 12 V				100	nA
	$I_{GATE(P)}$	$V_{GATE(N)}$ = 0 V, GND = 0 V, $V_{GATE(P)}$ = 12 V, 0V				100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	µA
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		5	3		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1 A	N-Ch P-Ch	0.5 0.6		0.6 0.7	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch P-Ch	1.0 1.1		1.4 1.5	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 0.5 A		0.5			S
SWITCHING							
Turn-On Delay Time[4]	$t_{d(on)}$	V_{DD} = 15 V, R_L = 24 Ω $I_D \simeq$ 1 A, V_{GEN} = 10 V, R_G = 25 Ω		25		50	ns
Rise Time[4]	t_r			25		50	ns
Turn-Off Delay Time[4]	$t_{d(off)}$			25		50	ns
Fall Time[4]	t_f		N-Ch P-Ch	28 50		50 75	ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					1.5	A
Pulsed Current[3]	I_{SM}					6.0	A
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.6	V

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.
[4]For design aid only, not subject to production testing.

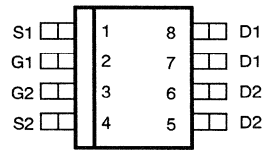
Si9952DY

N- and P-Channel Enhancement Mode MOSFETs

PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	20	0.10	3.5
P-Channel	–20	0.4	2.2

SO PACKAGE



Top View

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL[2]	LIMITS P-CHANNEL[2]	UNITS
Drain-Source Voltage		V_{DS}	20	20	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	3.5	2.2	A
	T_A = 100°C		2.2	1.1	
Pulsed Drain Current[1]		I_{DM}	14.0	8.0	
Maximum Power Dissipation	T_A = 25°C	P_D	2.0		W
	T_A = 100°C		0.8		
Operating Junction & Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	N- or P-CHANNEL	UNITS
Maximum Junction-to-Ambient (Surface Mounted)	R_{thJA}	62.5	K/W

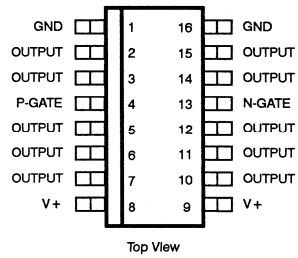
[1]Pulse width limited by maximum junction temperature.
[2]Negative Sign omitted for clarity.

5

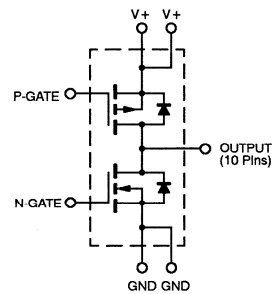
Si9954DY

Complementary MOSFET Half-Bridge

SO PACKAGE



Top View



PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	50	0.10	3.5
P-Channel	−50	0.25	2.65

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL	LIMITS P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	50	−50	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	3.5	2.65	A
	T_A = 100°C		2.2	1.6	
Pulsed Drain Current[1]		I_{DM}	14	10.6	
Maximum Power Dissipation	T_A = 25°C	P_D	2.5	3.0	W
	T_A = 100°C		1	1.25	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	N-CHANNEL	P-CHANNEL	UNITS
Maximum Junction-to-Ambient (Surface Mounted)	R_{thJA}	50	40	K/W

[1]Pulse width limited by maximum junction temperature.
[2]Limited by package power dissipation.

5

SPECIFICATIONS (T_J = 25°C Unless Otherwisw Noted)
N- and P-Channel Devices (Negative Signs for P-Channel Device Omitted for Clarity)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA			0.8	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V			7		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 1 A	N-Ch P-Ch	0.087 0.187		0.1 0.25	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch P-Ch	0.115 0.260		0.20 0.35	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1 A		2			S
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	N-Ch P-Ch	390 600			pF
Output Capacitance	C_{oss}		N-Ch P-Ch	150 325			
Reverse Transfer Capacitance	C_{rss}		N-Ch P-Ch	40 100			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$ V_{GS} = 10 V, I_D = 2 A	N-Ch P-Ch	14 26		30 32	nC
Gate-Source Charge[2]	Q_{gs}		N-Ch P-Ch	2.5 2.2			
Gate-Drain Charge[2]	Q_{gd}		N-Ch P-Ch	3.5 10			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω $I_D \simeq$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	N-Ch P-Ch	9 13		20 25	ns
Rise Time[2]	t_r		N-Ch P-Ch	8 14		20 25	
Turn-Off Delay Time[2]	$t_{d(off)}$		N-Ch P-Ch	45 180		90 200	
Fall Time[2]	t_f		N-Ch P-Ch	25 140		50 175	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S		N-Ch P-Ch			3.5 2.65	A
Pulsed Current[3]	I_{SM}		N-Ch P-Ch			14 10.6	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI/dt = 100 A/µs		70		100	ns

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data).

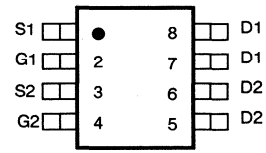
Si9955DY

Dual N-Channel Enhancement Mode MOSFETs

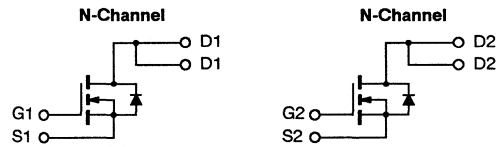
PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
Single N-Channel	50	0.13	3.0

SO PACKAGE



Top View



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SINGLE N-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[2]	T_A = 25°C	I_D	3.0	A
	T_A = 100°C		1.8	
Pulsed Drain Current[1, 2]		I_{DM}	12	
Maximum Power Dissipation	T_A = 25°C	P_D	2	W
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient (Surface Mounted)	R_{thJA}		62.5	K/W

[1]Pulse width limited by maximum junction temperature.
[2]Drain current limited by package construction

Advance Information

SPECIFICATIONS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	SINGLE N-CHANNEL MIN	SINGLE N-CHANNEL MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		7.2		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2 A	0.10		0.13	Ω
		V_{GS} = 4.5 V, I_D = 1 A	0.15		0.20	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 1 A	2			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	390			pF
Output Capacitance	C_{oss}		147			
Reverse Transfer Capacitance	C_{rss}		40			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2 A	14		30	nC
Gate-Source Charge[2]	Q_{gs}		2.6			
Gate-Drain Charge[2]	Q_{gd}		3.4			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	9		20	ns
Rise Time[2]	t_r		8		20	
Turn-Off Delay Time[2]	$t_{d(off)}$		45		70	
Fall Time[2]	t_f		25		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				3	A
Pulsed Current[3]	I_{SM}				12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	0.9		1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI/dt = 100 A/µs	70		100	ns

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

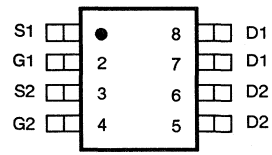
Si9956DY

Dual N-Channel Enhancement Mode MOSFETs

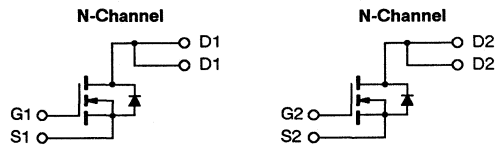
PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
Single N-Channel	20	0.10	3.5

SO PACKAGE



Top View



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SINGLE N-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[2]	T_A = 25°C	I_D	3.5	A
	T_A = 100°C		2.2	
Pulsed Drain Current[1,2]		I_{DM}	14	
Maximum Power Dissipation	T_A = 25°C	P_D	2	W
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient (Surface Mounted)	R_{thJA}		62.5	K/W

[1]Pulse width limited by maximum junction temperature.
[2]Drain current limited by package construction.

SPECIFICATIONS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	SINGLE N-CHANNEL MIN	SINGLE N-CHANNEL MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		20		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		3.5		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 2.2 A	0.087		0.1	Ω
		V_{GS} = 4.5 V, I_D = 1 A	0.115		0.20	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 2.2 A	4.4			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 16 V, f = 1 MHz	430			pF
Output Capacitance	C_{oss}		245			
Reverse Transfer Capacitance	C_{rss}		75			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.5 A	12		30	nC
Gate-Source Charge[2]	Q_{gs}		1.5			
Gate-Drain Charge[2]	Q_{gd}		3.7			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 10 V, R_L = 25 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	9		20	ns
Rise Time[2]	t_r		8		20	
Turn-Off Delay Time[2]	$t_{d(off)}$		45		90	
Fall Time[2]	t_f		25		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				3.5	A
Pulsed Current[3]	I_{SM}				14	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	0.9		1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI/dt = 100 A/µs	70		100	ns

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

PERFORMANCE CURVES (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

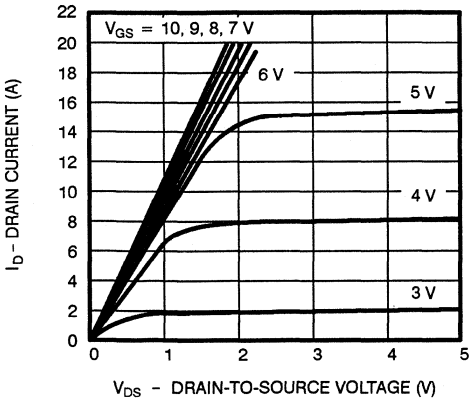


Figure 2. Transfer Characteristics

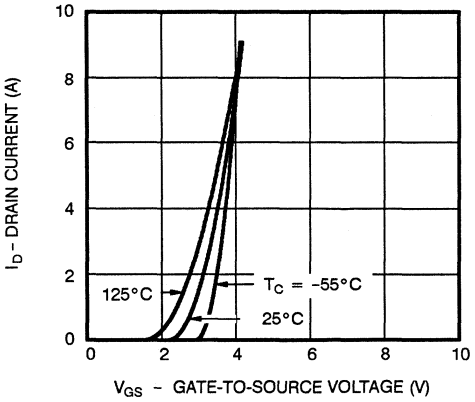


Figure 3. Transconductance

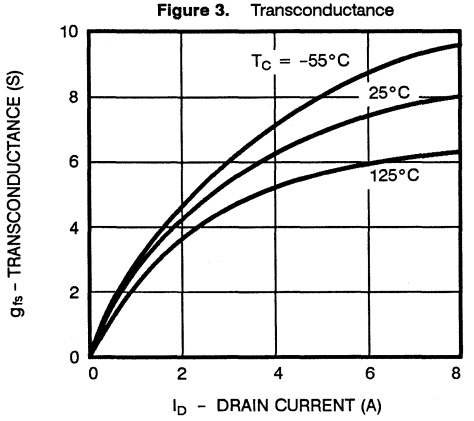


Figure 4. On-Resistance

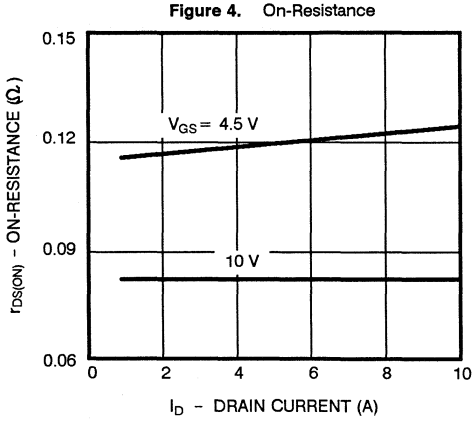


Figure 5. Capacitance

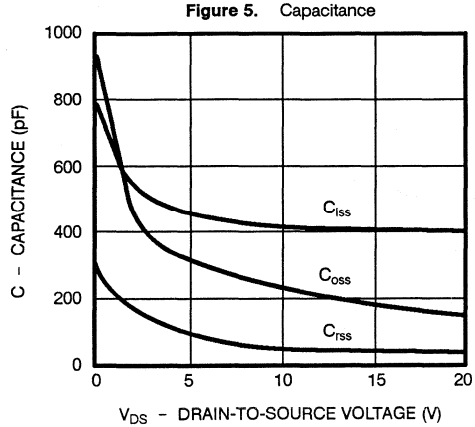
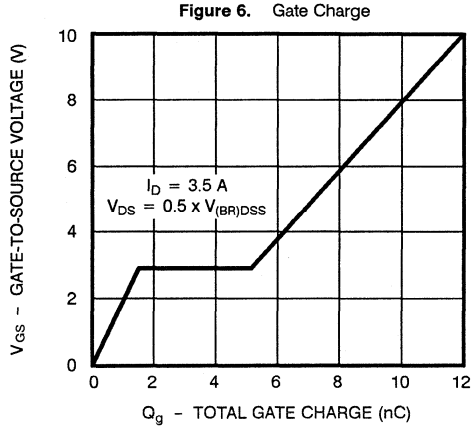


Figure 6. Gate Charge



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PERFORMANCE CURVES (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

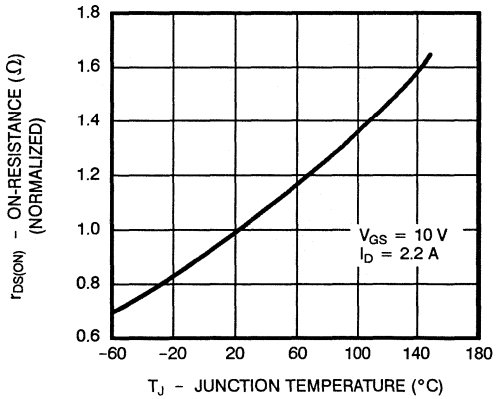
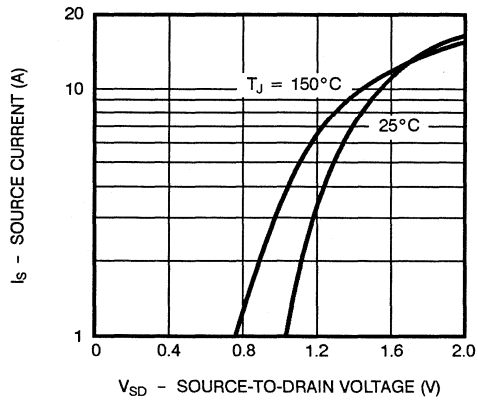


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

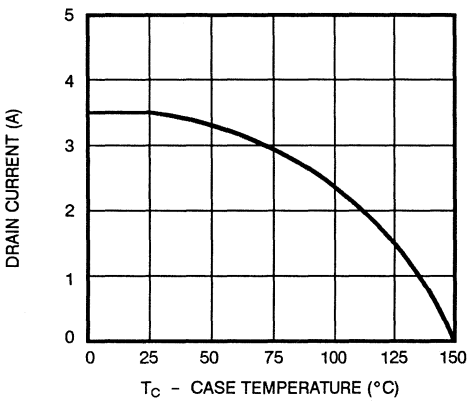
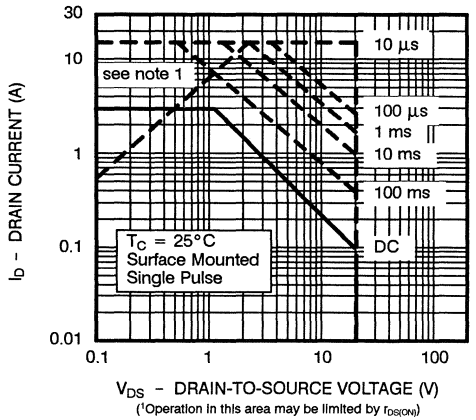
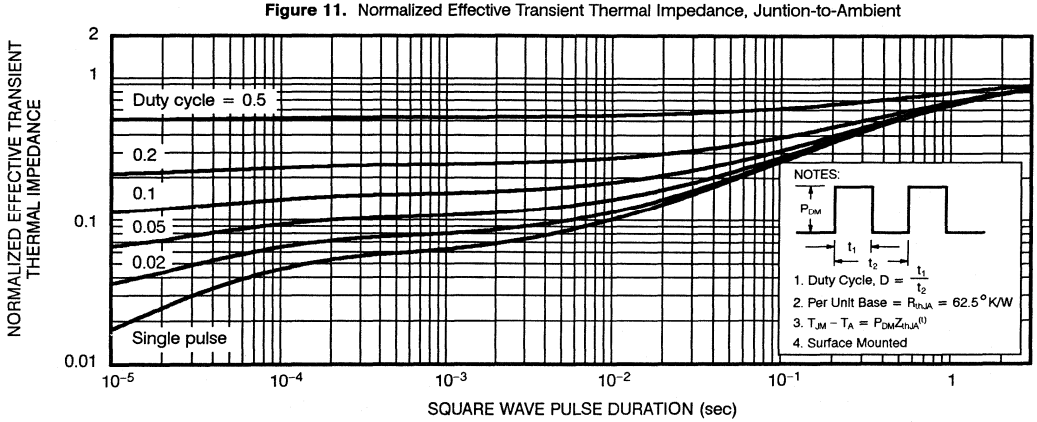


Figure 10. Safe Operating Area



([1]Operation in this area may be limited by $r_{DS(ON)}$)

Figure 11. Normalized Effective Transient Thermal Impedance, Juntion-to-Ambient



Si9961CY
12-V Voice Coil Motor Driver

FEATURES

- 1 A H-Bridge Output
- Class B Linear Operation
- Externally Programmable Gain and Bandwidth
- Undervoltage Head Retract
- Programmable Retract Current
- Low Standby Current
- Rail-to-Rail Output Swing
- Single 12-V Supply
- System Voltage Monitor
- Fault Output
- Linear "Track-Following" Operation

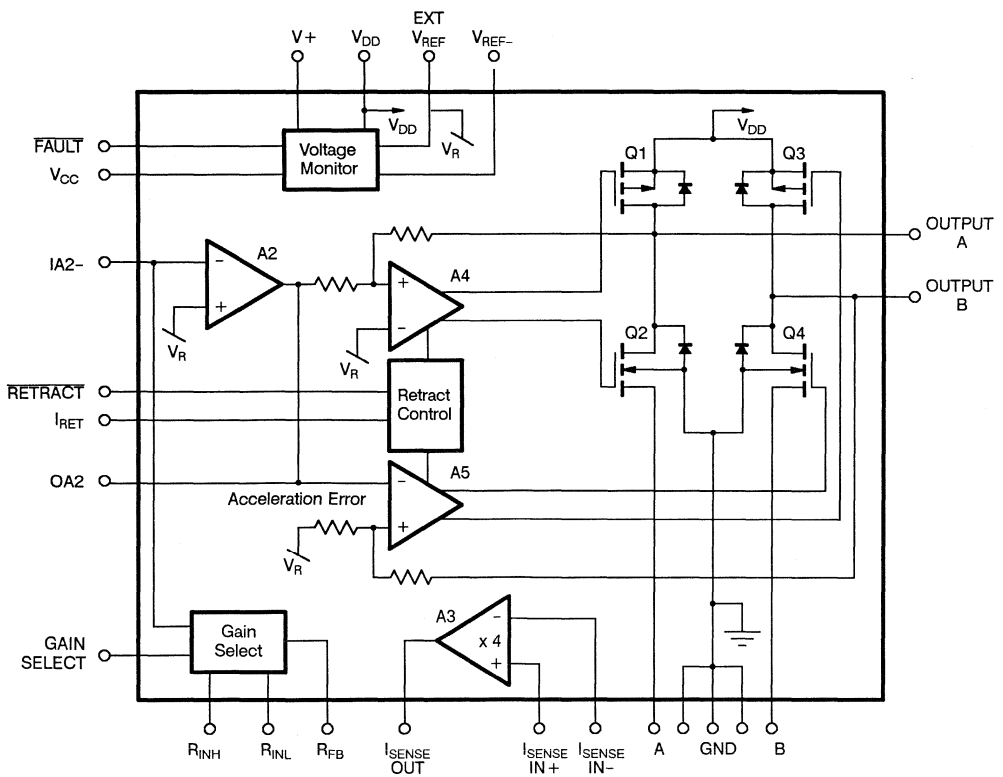
DESCRIPTION

The Si9961CY is a linear actuator (voice coil motor) driver suitable for use in disk drive head positioning systems. The Si9961CY contains all of the power and control circuitry necessary to drive the VCM that is typically found in a 3½ inch hard disk drives and optical disk drives. The driver is capable of delivering 1 A at a nominal supply of 12 V.

The Si9961CY provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a power amplifier featuring four complementary MOSFETs in a H-bridge configuration. The output crossover protection ensures no cross-conducting current and true Class B operation during linear tracking. Externally programmable gain in the current sense amplifier increases the resolution and dynamic range for a given DAC. The head retract circuitry is activated by an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract.

The Si9961CY is constructed on a self-isolated BiC/DMOS power IC process. The IC is available in 24-pin SO package for operation over the commercial, C suffix (0-70°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



5

Advance Information

Si9962CY
5-V Voice Coil Motor Driver

FEATURES

- 200 mA H-Bridge Output
- Class B Linear Operation
- Externally Programmable Gain and Bandwidth
- Undervoltage Head Retract
- Programmable Retract Current
- Low Standby Current
- Rail-to-Rail Output Swing
- Single 5-V Supply
- System Voltage Monitor
- Fault Output
- Linear "Track-Following" Operation

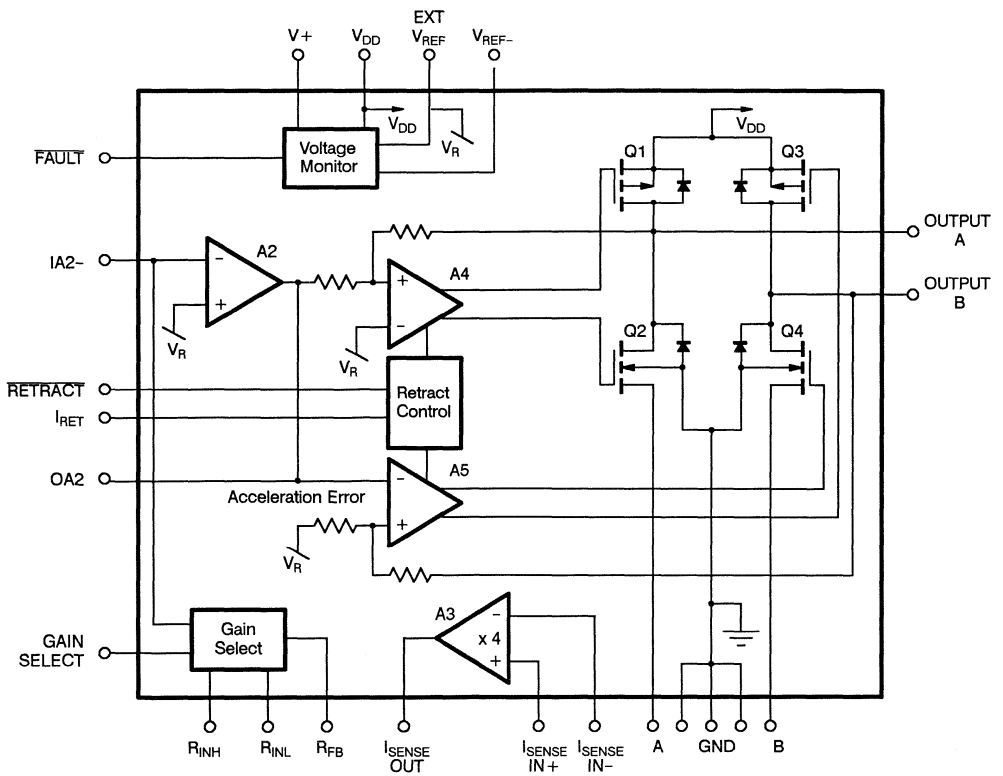
DESCRIPTION

The Si9962CY is a linear actuator (voice coil motor) driver suitable for use in disk drive head positioning systems. The Si9962CY contains all of the power and control circuitry necessary to drive the VCM that is typically found in a 2½ inch hard disk drives and optical disk drives. The driver is capable of delivering 200 mA at a nominal supply of 5 V.

The Si9962CY provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a power amplifier featuring four complementary MOSFETs in a H-bridge configuration. The output crossover protection ensures no cross-conducting current and true Class B operation during linear tracking. Externally programmable gain in the current sense amplifier increases the resolution and dynamic range for a given DAC. The head retract circuitry is activated by an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract.

The Si9962CY is constructed on a self-isolated BiC/DMOS power IC process. The IC is available in 24-pin SO package for operation over the commercial, C suffix (0-70°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



5

Si9975/Si9976
N-Channel Half-Bridge Driver

FEATURES

- 20 to 40-V Supply
- Cross-conduction Protected
- Undervoltage Lockout
- Short Circuit Protected
- ESD Protected
- Fault Feedback Si9976
- Static (dc) Operation

APPLICATIONS

- Power Supplies
- Motor Drives

END PRODUCTS

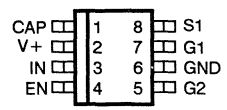
- Computer Peripherals
- Industrial Controllers
- Robotics
- Medical Equipment

DESCRIPTION

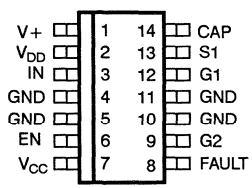
The Si9975 and Si9976 are integrated drivers for an n-channel MOSFET half-bridge. Schmitt trigger inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply range of 20 to 40 volts. Both half-bridge n-channel gates are driven directly with low-impedance outputs. Addition of one external capacitor allows an internal circuit to level shift both the power supply and logic signal for the half-bridge high-side n-channel gate drive. An internal charge pump replaces any high-side driver or gate leakage, providing "static" (dc) drive for the upper n-channel MOSFET. Undervoltage lockout assures sufficient voltage to provide safe gate drive levels. Protection logic eliminates the possibility of turning both half-bridge MOSFETs on simultaneously. The Si9975/Si9976 is available in the 8/14 pin SOIC (surface mount) package, specified to operate over the industrial (–40 to 85°C) temperature range.

PIN CONFIGURATION

SO Package

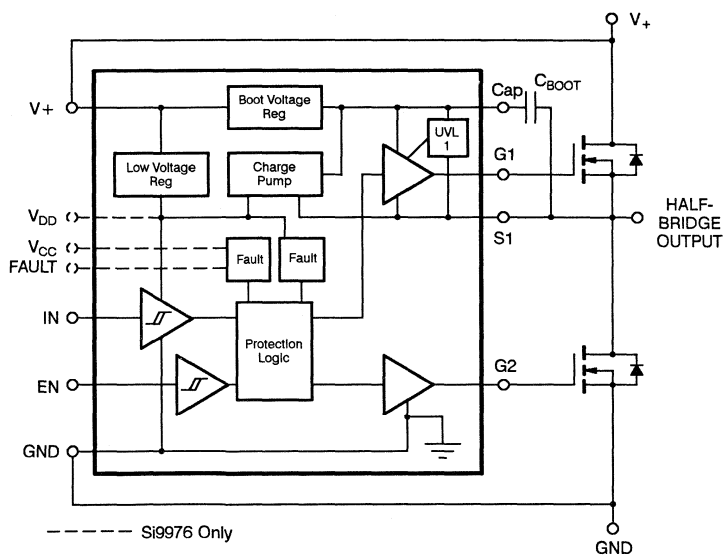


Top View
Si9975DY



Top View
Si9976DY

FUNCTIONAL BLOCK DIAGRAM



5

Si9985CY

Sensorless, 3-Phase Spindle Motor Driver

FEATURES

- 1 A, 1.4 Ω Half-bridge
- Single 5-V Supply
- Back EMF Commutation
- Rail-to-rail Output Voltage Swing
- Linear Voltage Control
- No Current Sense Resistor
- Over-temperature Protection
- 2 Types of Speed Control: Phase and Frequency Lock
- 4- or 8-Pole Motors

DESCRIPTION

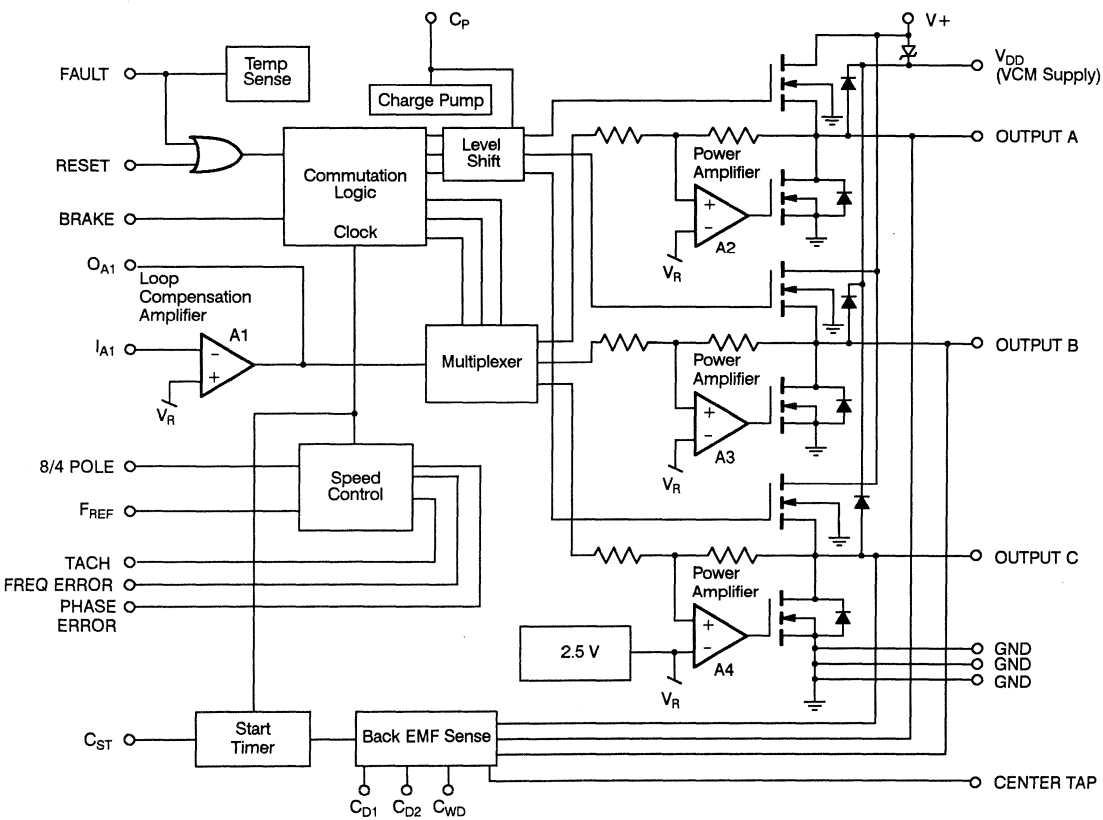
The Si9985CY is a 3-phase brushless dc (Spindle) motor driver with internal back EMF sensing circuitry that eliminates the need for hall sensors. Therefore, providing the circuitry necessary for a hard disk drive system with linear speed control to minimize EMI and RFI.

The Si9985CY features a 1 A, 1.4 Ω all n-channel MOSFET half-bridge output stage. An internal charge pump allows rail-to-rail output voltage swing with a nominal 5-V supply. Our unique output structure eliminates the need for an external Schottky diode to isolate the system 5-V supply during emergency head retract. This makes the output half-bridge equivalent to other competitive drivers with 1 A, 1 Ω specifications requiring an external Schottky diode.

Motor acceleration and velocity control is accomplished without the series voltage drop of the sense resistor. Included for system flexiblity is the circuitry for either phase lock or frequency lock speed control. Also added is the provision for either 4- or 8-pole motors.

The Si9985CY is constructed on our self-isolated BiC/DMOS process and is available in a 24-pin SO package for operation over the commercial, C suffix (0 to 70 °C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



5

Advance Information

MOSPOWER DIE PRODUCTS

Siliconix offers MOSPOWER products in die form for hybrid and multichip applications. These dice can provide the same high performance and reliability as the equivalent packaged devices.

Currently available standard die types are listed in Table 1, and die topology diagrams for these products are shown on pages 6-5 through 6-8. The Cross Reference (page 6-9) shows Siliconix MOSPOWER die types equivalent to other industry part numbers.

In addition to the standard products described here, Siliconix can also supply MOSPOWER dice specifically selected for custom requirements. Further information on these custom products can be obtained from Siliconix sales representatives and sales offices.

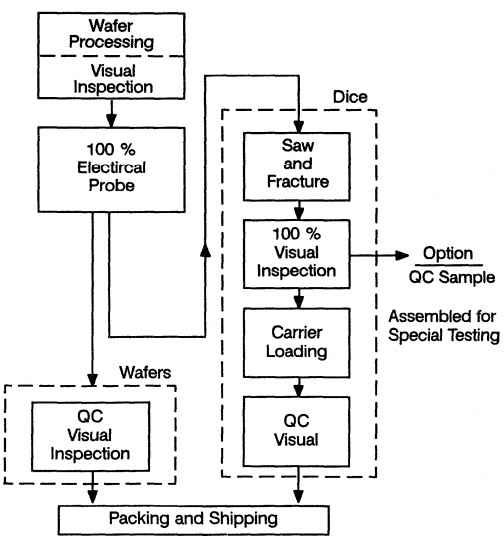


Figure 1. MOSPOWER Die Processing Flow

Die and Wafer Processing

The standard MOSPOWER die processing flow is outlined in Figure 1. The flow includes 100% electrical test in wafer form (for selected tests described below) and 100% visual inspection of separated dice.

Die Screening

Electrical Screening

Electrical tests performed on MOSPOWER dice fall into the following two classes:

1. Characteristics which can be tested using probes with the dice in wafer form include $V_{(BR)DSS}$, I_{DSS}, I_{GSS}, $r_{DS(ON)}$, and $V_{GS(th)}$. Due to limitations inherent in wafer testing, some characteristics cannot be tested to exactly the same specifications as the generic packaged device. For example, current limitations of the probes and the power dissipation limitations of dice in wafer form prevent testing of $r_{DS(ON)}$ at the full current rating. Parameters that are tested by probing in wafer form and guaranteed on all dice at 25°C ambient are shown in Table 1. Table 2 shows parameters and limits that are applicable to all MOSPOWER dice part numbers.

2. For characteristics that cannot be tested in wafer or die form, a sample group of units must be assembled into packages for testing. Examples include safe operating area, $r_{DS(ON)}$ at maximum rated current, capacitance, gate charge, switching times, and performance at hot and cold temperatures. These tests are performed by special request.

Characteristics guaranteed by design to meet the specifications of the equivalent packaged part in die form include g_{fs}, C_{iss}, C_{oss}, C_{rss}, and $T_{J(MAX)}$.

Visual Screening

All MOSPOWER dice are subjected to 100% visual sort after die separation. The visual inspection criteria of MIL-STD-750 for discrete MOS transistors are used for standard die products.

Table 1a. Standard MOSPOWER Die Types (N-Channel)

Die Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(ON)}$ @ I_D = 1 A V_{GS} = 10V Max. (Ω)	$V_{GS(th)}$ @ I_D = 0.25 mA V_{DS} = V_{GS} Min. (V)	$V_{GS(th)}$ @ I_D = 0.25 mA V_{DS} = V_{GS} Max. (V)	Die Topology	Recommended Al Bond Wire Diameter Source (mil)	Recommended Al Bond Wire Diameter Gate (mil)	Dimensions Thickness Mils ±2	Dimensions x Mils ±2	Dimensions y Mils ±2	Data Sheet for Electrical Characteristics
N-CHANNEL											
SMC14N65	650	0.55	2.0	4.0	B	20	5	21	289	280	SMM14N65
SMC7N60	600	1.1	2.0	4.0	C	15	5	21	177	234	SMP7N60
SMC4N60	600	2.0	2.0	4.0	E	8	5	21	127	182	SMP4N60
SMC20N50	500	0.30	2.0	4.0	B	20	5	21	289	280	SMM20N50
IRF450CHP	500	0.40	2.0	4.0	H	20	5	21	263	259	IRF450
SMC14N50F[1]	500	0.40	2.0	4.0	H	20	5	21	263	259	SMW14N50F[1]
IRF440CHP	500	0.85	2.0	4.0	C	15	5	21	177	234	IRF440
SMC8N50F[1]	500	0.85	2.0*	4.0*	C	15	5	21	177	234	SMP8N50F[1]
IRF430CHP	500	1.5	2.0	4.0	E	8	5	21	127	182	IRF430
SMC5N50F[1]	500	1.5	2.0*	4.0*	E	8	5	21	127	182	SMP5N50F[1]
IRF820CHP	500	3.0	2.0	4.0	D	6	5	21	100	142	IRF820
SMC3N50F[1]	500	3.0	2.0*	4.0*	D	6	5	21	100	142	SMP3N50F[1]
SMC24N40	400	0.20	2.0	4.0	B	20	5	21	280	289	SMM24N40
IRF350CHP	400	0.30	2.0	4.0	H	20	5	21	263	259	IRF350
IRF340CHP	400	0.55	2.0	4.0	C	15	5	21	177	234	IRF340
IRF330CHP	400	1.0	2.0	4.0	E	8	5	21	127	189	IRF330
IRF720CHP	400	1.8	2.0	4.0	D	6	5	21	100	142	IRF720
SMC40N20	200	0.060	2.0	4.0	B	20	5	21	286	280	SMM40N20
IRF250CHP	200	0.085	2.0	4.0	H	20	5	21	250	254	IRF250
SMC20N20	200	0.160	2.0	4.0	S	15	5	14	170	200	SMP20N20
IRF240CHP	200	0.180	2.0	4.0	C	15	5	21	170	229	IRF240
IRF230CHP	200	0.40	2.0	4.0	E	8	5	21	118	180	IRF230
IRF620CHP	200	0.80	2.0	4.0	D	6	5	21	88	137	IRF620
IRF610CHP	200	1.5	2.0	4.0	L	4	4	21	75	81	IRF610
SMC70N10	100	0.025	2.0	4.0	A	3x15	5	18	246	250	SMM70N10
SMC40N10	100	0.040	2.0	4.0	U	3x15	5	18	224	185	SMP40N10
IRF150CHP	100	0.055	2.0	4.0	U	3x15	5	18	224	185	SMW45N10
IRF140CHP	100	0.085	2.0	4.0	J	15	5	18	141	187	SMP30N10
SMC30N10	100	0.060	2.0	4.0	J	15	5	18	141	187	SMP30N10
IRF130CHP	100	0.18	2.0	4.0	M	8	5	18	99	115	IRF530
IRF520CHP	100	0.30	2.0	4.0	F	6	5	18	80	87	IRF520
IRF510CHP	100	0.60	2.0	4.0	K	4	4	18	51	81	IRF510
SMC60N06-14	60	0.014	2.0*	4.0*	P	3x15	5	14	234	177	SMP60N06-14
SMC60N06-18	60	0.018	2.0*	4.0*	Q	3x15	5	14	187	172	SMP60N06-18
SMC50N06-25	60	0.025	2.0*	4.0*	R	2x15	5	14	123	190	SMP50N06-25
SMC25N06	60	0.060	2.0*	4.0*	G	12	5	18	119	135	SMP25N06
BUZ11CHP	50	0.040	2.1*	4.0*	J	2x15	5	18	141	187	BUZ11
BUZ71CHP	50	0.10	2.1*	4.0*	N	15	5	14	72	92	BUZ71

*Measured at 1 mA

[1]Integral fast reverse recovery diode

Table 1b. Standard MOSPOWER Die Types ((P-Channel)

Die Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(ON)}$ @ I_D = 1 A V_{GS} = 10V Max. (Ω)	$V_{GS(th)}$ @ I_D = 0.25 mA V_{DS} = V_{GS} Min. (V)	Max. (V)	Die Topology	Recommended Al Bond Wire Diameter Source (mil)	Gate (mil)	Dimensions Thickness Mils ±2	x Mils ±2	y Mils ±2	Data Sheet for Electrical Characteristics
P-CHANNEL											
SMC11P20	200	0.50	2.0	4.0	C	15	5	18	170	229	SMP11P20
IRF9230CHP	200	0.80	2.0	4.0	E	8	5	18	118	180	IRF9230
IRF9620CHP	200	1.5	2.0	4.0	D	6	5	18	88	137	IRF9620
SMC2P20	200	3.0	2.0	4.0	L	4	4	18	75	81	SMP2P20
SMC20P10	100	0.25	2.0	4.0	C	15	5	18	170	229	SMP20P10
IRF9130CHP	100	0.30	2.0	4.0	E	8	5	18	118	180	IRF9130
IRF9520CHP	100	0.60	2.0	4.0	V	6	5	18	76	113	IRF9520
SMC3P10	100	1.2	2.0	4.0	L	4	4	18	75	81	SMP3P10
BUZ171CHP	50	0.40	2.1*	4.0*	T	15	5	18	94	130	BUZ171

*Measured at 1 mA

Table 2. Parameters and limits applicable to all MOSPPOWER dice

Parameter	Condition	Limit
I_{DSS}	V_{DS} = rated $V_{(BR)DSS}$	0.25 mA
I_{GSS}	V_{GS} = 20 V	100 nA

Assembly Techniques

Die Attach

The backside drain metallization used on Silconix MOSPOWER dice is titanium-nickel-silver. This metallization is suitable for die mounting using standard "soft solders" such as 95/5 Pb/Sn, 92.5/5/2.5 Pb/Sn/Ag, 65/25/10 Sn/Ag/Sb, and 92.5/5/2.5 Pb/In/Ag. Copper, nickel-plated copper, and gold-plated molybdenum, beryllia, or alumina are among the most commonly used substrate or header materials that give good results. The substrate must be de-oxidized prior to assembly by chemical cleaning or by prefiring in a reducing atmosphere such as hydrogen or forming gas.

MOSPOWER dice shipped in die trays (see "Packaging and Handling Methods") will not normally require cleaning. If cleaning is performed, however, a one-minute de-ionized water wash followed by two one-minute rinses in an isopropyl alcohol agitated bath is the recommended method. Drying should be accomplished in a 70°C nitrogen chamber.

Dice may be mounted using mechanical scrubbing or by heating in a profiled belt furnace using a reducing atmosphere. Care must be exercised not to expose the dice to temperatures in excess of 400°C. Control of the die mounting procedure is extremely important in most applications, as a uniform, void-free die attach is necessary to achieve good thermal conductivity between the die and its mounting surface.

In lower power applications, conductive adhesives have been used successfully to mount MOSPOWER dice. This alternative is particularly applicable when lower temperature processing is desired.

Wire Bonding

On all die types, gate and source bonding pad (topside) metallization is aluminum with a 1% silicon content of either 1.8 μm or 2.8 μm in nominal thickness.

Ultrasonic wire bonding using aluminum wire with an elongation of no more than 10% is recommended for making connections to gate and source pads. Thermocompression gold wire bonding may also be used. Maximum recommended aluminum wire diameter for each die type is shown in Table 1.

Wire bonding must be performed with care to ensure that the entire bonding footprint remains within the bonding pad and that appropriate bonding force is used; device failure might otherwise result. Optimization of bonding parameters is highly dependent on the bonding equipment and, thus, should be determined by the user. Siliconix recommends performing a routine wire bond strength monitor similar to that described in MIL-STD-750, Method 2037.

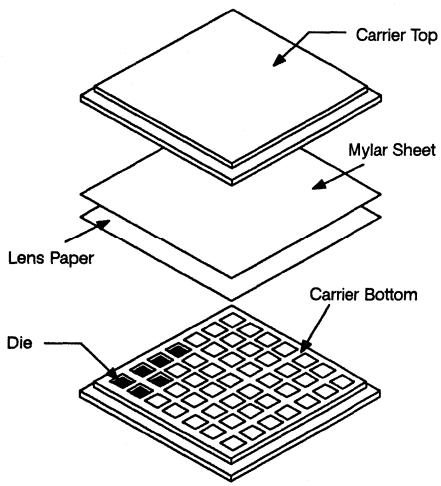
Encapsulation

It is critical that the die and assembly be kept in a dry environment prior to encapsulation. Although the passivation layer on the die (silicon nitride or deposited glass) is relatively impermeable, unacceptably high surface leakage may result from adsorbed moisture.

Since the long-term stability of the die-attach interface is also adversely affected by the presence of moisture or oxygen in a hermetic package, it is strongly recommended that the die header assembly be baked prior to encapsulation to drive off moisture. The subsequent encapsulation process should be performed in an inert atmosphere, such as nitrogen. Die coatings, if used, should be applied in accordance with the suggestions of the coating manufacturer.

Packaging and Handling Methods

Individual dice are packaged in antistatic die trays with cavities (known as "waffle" carriers), as shown in Figure 2. Each carrier has a cavity size that allows easy loading and unloading of the die and that prevents die rotation.



NOTE: Carrier Top & Bottom Secured By Clips

Figure 2. Die Tray

Quantities of dice packaged in each die tray, which are also the incremental quantities for ordering, are shown in Table 3.

Table 3. Die Tray Quantities

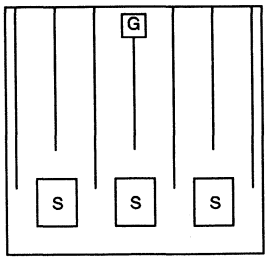
Die Topology	Quantity per Die Tray
A	36
B	25
C	36
D	140
E	20
F	100
G	80
H	36
J	20
K	100
L	100
M	100
N	100
P	36
Q	36
R	20
S	36
T	140
U	36
V	140

Dice should preferably be handled with a vacuum pickup, that has a protected (non-reactive) tip, at an electrostatic discharge (ESD) protected workstation to prevent mechanical and ESD damage. While MOSPOWER chips have some inherent resistance to damage due to ESD, due to their larger gate capacitance and thicker oxides, it is nevertheless essential to take precautions to prevent ESD damage. Refer to Section 9 of this data book for further details.

Special Requirements

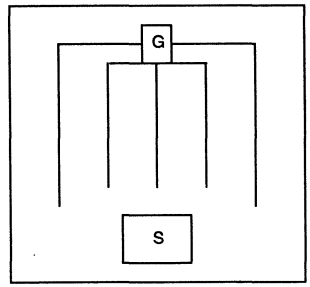
The Siliconix sales representative should be consulted regarding requirements for alternate back metallization or visual inspection, lot qualification by quality conformance inspection of encapsulated dice, scanning electron microscope (SEM) inspection, or any other special requirements.

MOSPOWER Die Topologies



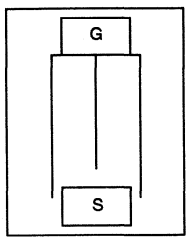
Gate Pad: 0.0175 X 0.0175
Source Pads: 0.0340 X 0.0520

TOPOLOGY A



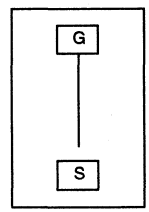
Gate Pad: 0.0250 X 0.0400
Source Pad: 0.0700 X 0.0500

TOPOLOGY B



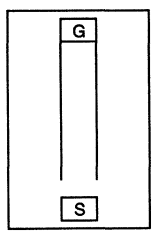
Gate Pad: 0.0615 X 0.0375
Source Pad: 0.0615 X 0.0375

TOPOLOGY C



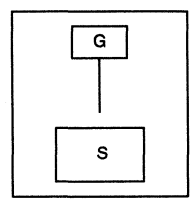
Gate Pad: 0.0281 X 0.0192
Source Pad: 0.0273 X 0.0186

TOPOLOGY D



Gate Pad: 0.0340 X 0.0222
Source Pad: 0.0347 X 0.0229

TOPOLOGY E

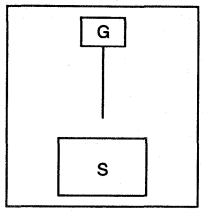


Gate Pad: 0.0250 x 0.0150
Source Pad: 0.0400 x 0.0250

TOPOLOGY F

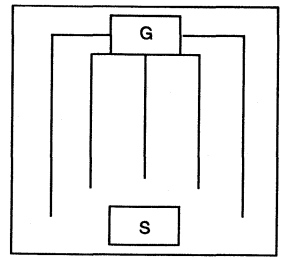
Note: x and y from Table 1a and 1b are represented by horizontal and vertical dimensions respectively

MOSPOWER Die Topologies (Cont'd)



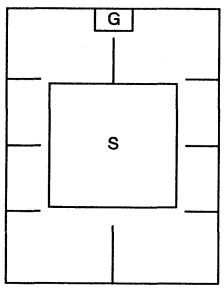
Gate Pad: 0.0250 X 0.0150
Source Pad: 0.0600 X 0.0400

TOPOLOGY G



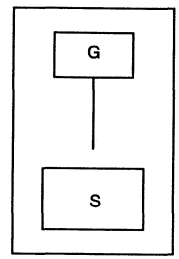
Gate Pad: 0.0664 X 0.0397
Source Pad: 0.0664 X 0.0384

TOPOLOGY H



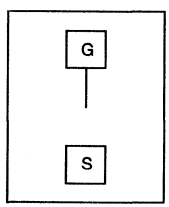
Gate Pad: 0.0250 x 0.0150
Source Pads: 0.0840 x 0.0840

TOPOLOGY J



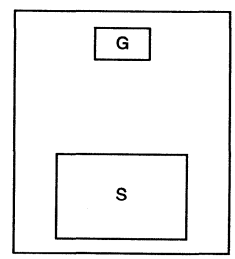
Gate Pad: 0.0250 x 0.0150
Source Pad: 0.0320 x 0.0200

TOPOLOGY K



Gate Pad: 0.0155 X 0.0125
Source Pad: 0.0160 X 0.0118

TOPOLOGY L

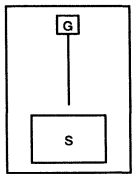


Gate Pad: 0.0250 x 0.0150
Source Pad: 0.0600 x 0.0400

TOPOLOGY M

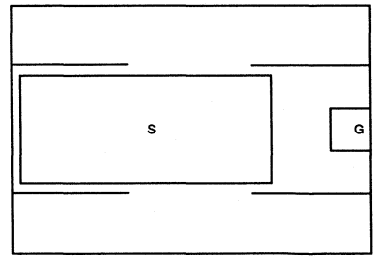
Note: x and y from Table 1a and 1b are represented by horizontal and vertical dimensions respectively

MOSPOWER Die Topologies (Cont'd)



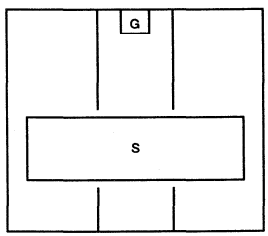
Gate Pad: 0.017 x 0.025
Source Pad: 0.030 x 0.048

TOPOLOGY N



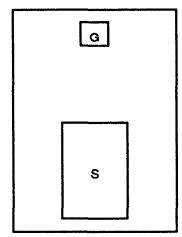
Gate Pad: 0.015 x 0.020
Source Pad: 0.147 x 0.055

TOPOLOGY P



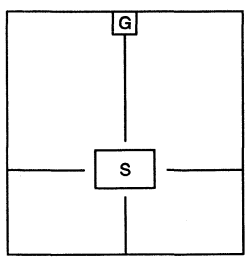
Gate Pad: 0.017 x 0.023
Source Pad: 0.059 x 0.149

TOPOLOGY Q



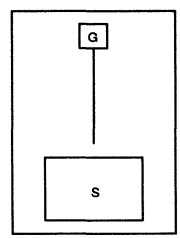
Gate Pad: 0.017 x 0.023
Source Pad: 0.100 x 0.054

TOPOLOGY R



Gate Pad: 0.017 x 0.027
Source Pads: 0.045 x 0.060

TOPOLOGY S

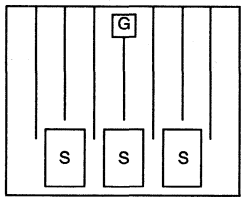


Gate Pad: 0.0183 X 0.0142
Source Pad: 0.0528 X 0.0394

TOPOLOGY T

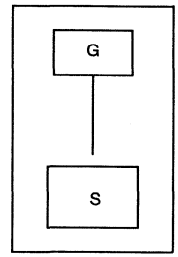
Note: x and y from Table 1a and 1b are represented by horizontal and vertical dimensions respectively

MOSPOWER Die Topologies (Cont'd)



Gate Pad: 0.0180 X 0.0180
Source Pads: 0.0340 X 0.0520

TOPOLOGY U



Gate Pad: 0.0249 x 0.0151
Source Pad: 0.0320 x 0.0263

TOPOLOGY V

Note: x and y from Table 1a and 1b are represented by horizontal and vertical dimensions respectively

MOSPOWER Dice – Industry Cross Reference

Industry Type	Siliconix Type
IRFC020	BUZ71CHP
IRFC030	BUZ11CHP
IRFC040	SMC50N06
IRFC110	IRF510CHP
IRFC113	IRF510HP
IRFC120	IRF520CHP
IRFC123	IRF520CHPC
IRFC130	IRF130CHP
IRFC133	IRF130CHP
IRFC140	IRF140CHP
IRFC143	IRF140CHP
IRFC150	IRF150CHP
IRFC153	IRF150CHP
IRFC210	IRF610CHP
IRFC213	IRF610CHP
IRFC220	IRF620CHP
IRFC223	IRF620CHP
IRFC230	IRF230CHP
IRFC233	IRF230CHP
IRFC240	IRF240CHP
IRFC243	IRF240CHP
IRFC250	IRF250CHP
IRFC253	IRF250CHP
IRFC320	IRF720CHP
IRFC323	IRF720CHP
IRFC330	IRF330CHP
IRFC333	IRF330CHP
IRFC340	IRF340CHP
IRFC343	IRF350CHP
IRFC350	IRF350CHP
IRFC353	IRF350CHP
IRFC420	IRF820CHP
IRFC423	IRF820CHP
IRFC43O	IRF430CHP
IRFC433	IRF430CHP
IRFC440	IRF440CHP
IRFC443	IRF440CHP
IRFC450	IRF450CHP
IRFC453	IRF450CHP
IRFC9110	SMC3P10
IRFC9113	SMC3P10
IRFC9120	IRF9520CHP
IRFC9123	IRF9520CHP
IRFC9130	IRF9530CHP
IRFC9133	IRF9530CHP
IRFC9140	SMC20P10
IRFC9143	SMC20P10

Industry Type	Siliconix Type
IRFC9210	SMC2P20
IRFC9213	SMC2P20
IRFC9220	IRF9620CHP
IRFC9223	IRF9620CHP
IRFC9230	IRF9630CHP
IRFC9233	IRF9630CHP
IRFC9240	SMC11P20
IRFC9243	SMC11P20
MTC2N18	IRF610CHP
MTC2N20	IRF610CHP
MTC2N45	IRF820CHP
MTC2N50	IRF820CHP
MTC4N08	IRF510CHP
MTC4N10	IRF510CHP
MTC4N18	IRF620CHP
MTC4N20	IRF620CHP
MTC4N45	IRF830CHP
MTC4N50	IRF830CHP
MTC5N18	IRF620CHP
MTC5N20	IRF620CHP
MTC5N35	IRF730CHP
MTC5N40	IRF730CHP
MTC6N08	IRF510CHP
MTC6N10	IRF510CHP
MTC7N18	IRF620CHP
MTC7N20	IRF620CHP
MTC7N45	IRF440CHP
MTC7N50	IRF440CHP
MTC8N08	IRF510CHP
MTC8N10	IRF510CHP
MTC8N18	IRF230CHP
MTC8N20	IRF230CHP
MTC8P08	IRF9130CHP
MTC8P10	IRF9130CHP
MTC10N08	IRF520CHP
MTC10N10	IRF520CHP
MTC12N08	IRF130CHP
MTC12N10	IRF130CHP
MTC12N18	IRF230CHP
MTC12N20	IRF230CHP
MTC13N50	IRF450CHP
MTC15N05	BUZ71CHP
MTC15N06	SMC25N06
MTC15N18	IRF230CHP
MTC15N20	IRF350CHP
MTC15N35	IRF350CHP
MTC15N40	IRF350CHP

Industry Type	Siliconix Type
MTC15N45	IRF450CHP
MTC15N50	IRF450CHP
MTC20N08	IRF130CHP
MTC20N10	IRF130CHP
MTC25N05	SMC25N06
MTC25N06	SMC25N06
MTC25N10	IRF140CHP
MTC35N05	SMC25N06
MTC35N06	SMC25N06
MTC40N10	IRF150CHP
MTC40N20	IRF250CHP
MTC50N05	SMC50N06-25
MTC50N06	SMC50N06-25
MTC55N10	IRF150CHP
MTC3055A	BUZ71CHP
PCF3N45	IRF820CHP
PCF4N35	IRF720CHP
PCF6N45	IRF830CHP
PCF7N35	IRF730CHP
PCF8N18	IRF230CHP
PCF8P08	IRF9130CHP
PCF10N45	IRF450CHP
PCF12N08	IRF130CHP
PCF12P08	IRF9130CHP
PCF12N18	IRF240CHP
PCF12N35	IRF350CHP
PCF15N05	BUZ71CHP
PCF18N08	IRF140CHP
PCF25N05	SMC25N06
PCF25N18	IRF240CHP
PCF25P08	SMC20P10
PCF35N08	IRF150CHP
PCF45N05	BUZ11CHP
PCF111	IRF510CHP
PCF121	IRF520CHP
PCF131	IRF130CHP
PCF211	IRF610CHP
PCF221	IRF620CHP
PCF231	IRF230CHP
PCF321	IRF720CHP
PCF331	IRF330CHP
PCF421	IRF820CHP
PCF431	IRF430CHP
SIRF150	IRF150CHP
SIRF250	IRF250CHP
SIRF350	IRF350CHP
SIRF450	IRF450CHP

TEST CIRCUITS

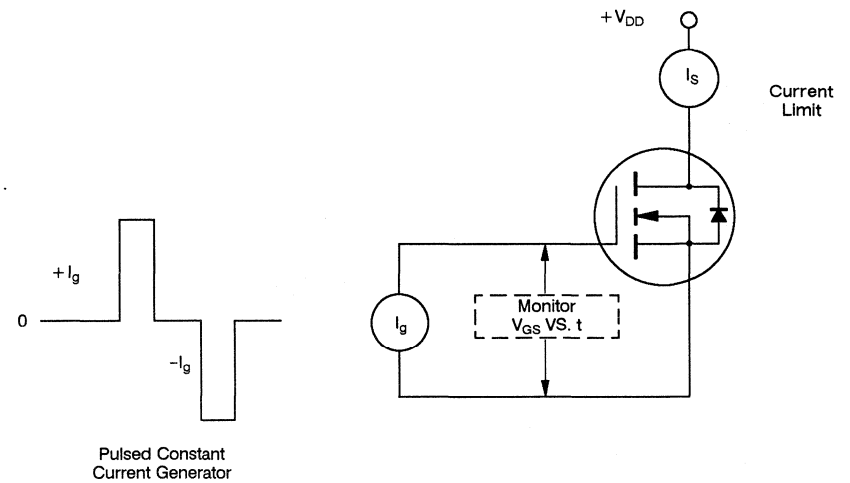


Figure 1. Gate Charge Test Circuit

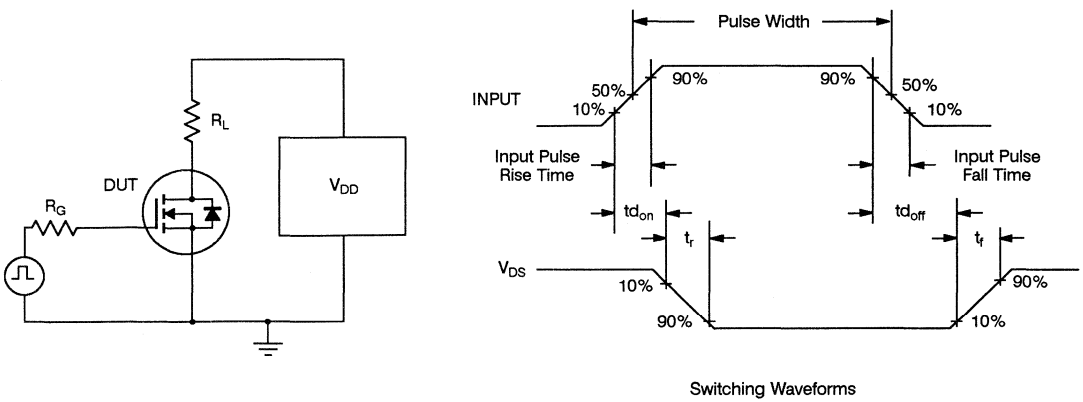
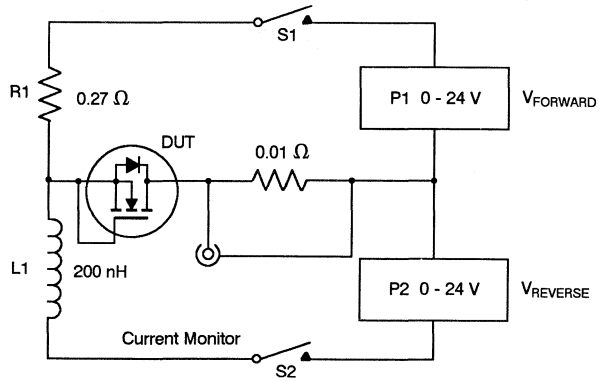
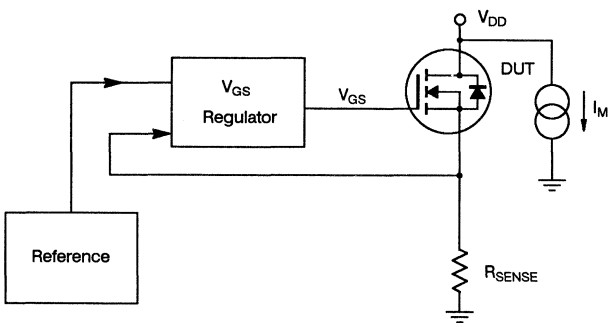


Figure 2. Switching Time Test Circuits and Defintitions



The forward current is controlled by resistor R1 and power supply P1. Switch S1 is opened and switch S2 is closed simultaneously. The di/dt of the reverse current is controlled by inductor L1 and power suply P2. S1 & S2 may be implemented with Power MOSFETs.

Figure 3. Diode Reverse Recovery Test Circuit



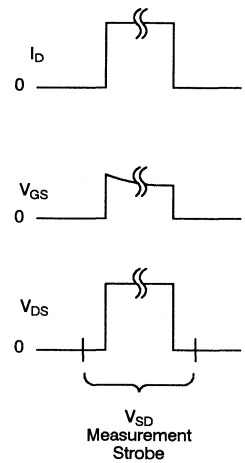
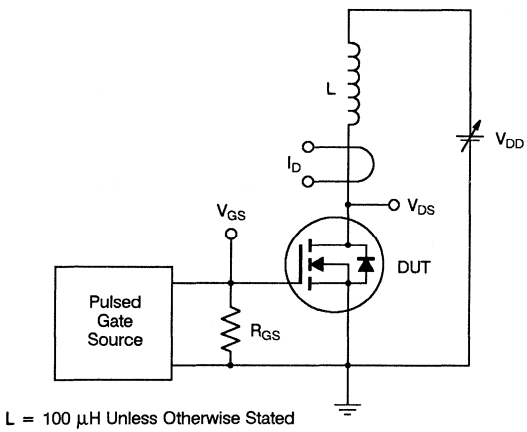
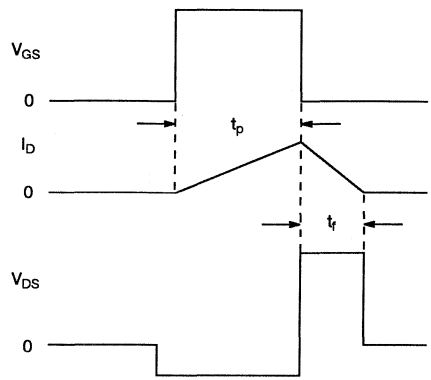


Figure 4. Thermal Resistance Test Circuit

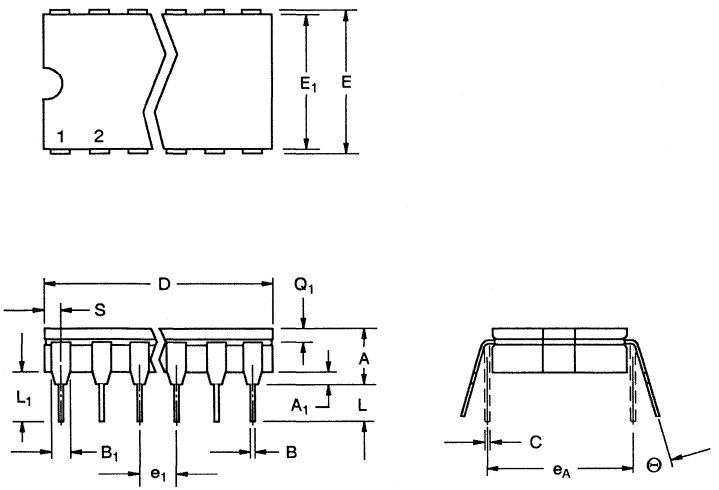




L = 100 µH Unless Otherwise Stated

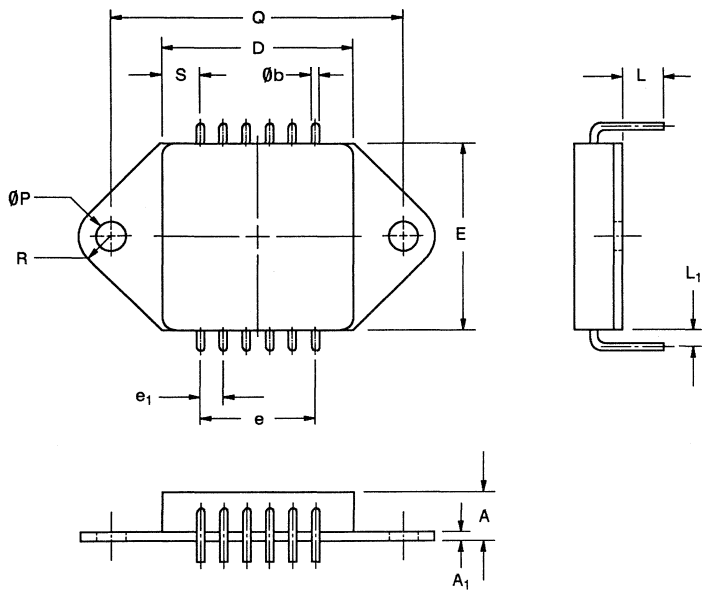
Figure 5. Unclamped Inductive Switching Test Circuit

CerDIP (K, Q Suffix), 14–16 Leads



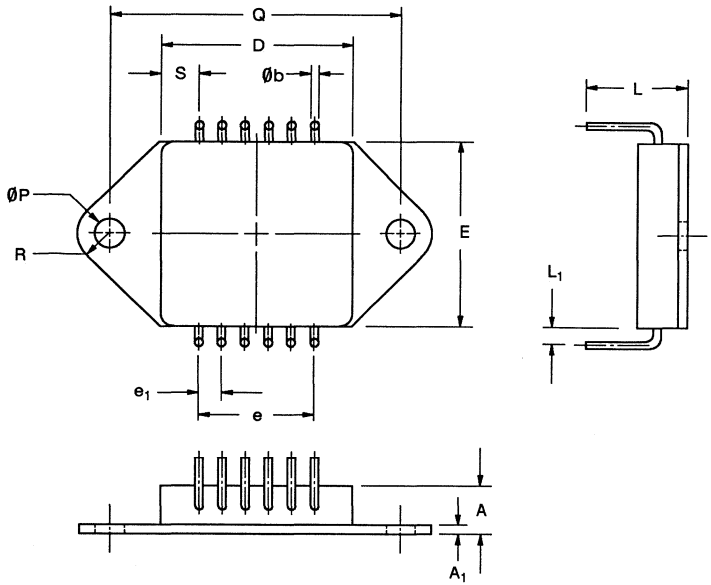
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D-14	19.05	19.56	0.750	0.770
D-16	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S-14	1.65	2.41	0.065	0.095
S-16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

Hermetic Power Module (Bent Down Lead)



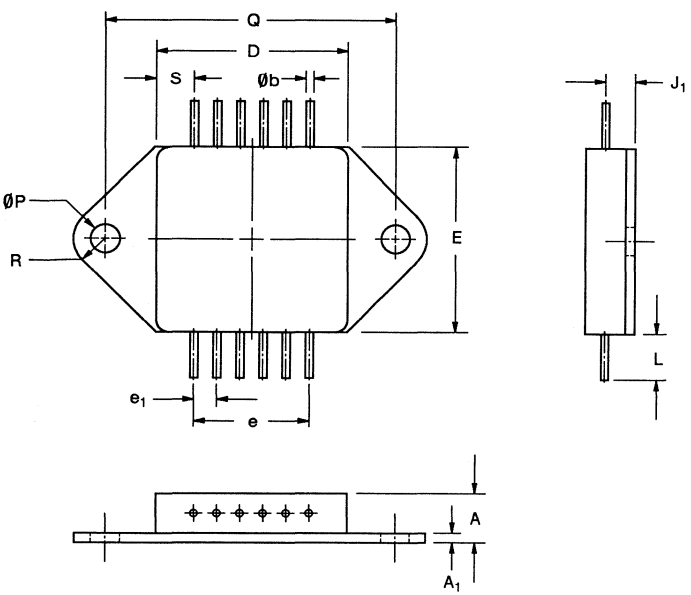
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	0.240	0.280
A_1	1.14	1.40	0.045	0.055
Ø b	0.89	1.14	0.035	0.045
D	24.89	25.91	0.980	1.020
E	24.89	25.91	0.980	1.020
e	15.62	16.13	0.615	0.635
e_1	2.92	3.43	0.115	0.135
L	4.44	6.35	0.175	0.250
L_1	2.79	3.30	0.110	0.130
Ø P	3.84	4.09	0.151	0.161
Q	38.35	38.86	1.510	1.530
R	4.19	4.44	0.165	0.175
S	4.57	4.95	0.180	0.195

Hermetic Power Module (Bent Up Lead)



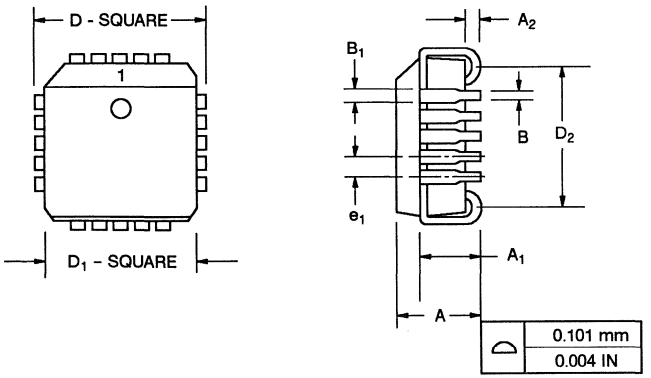
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	0.240	0.280
A_1	1.14	1.40	0.045	0.055
Øb	0.89	1.14	0.035	0.045
D	24.89	25.91	0.980	1.020
E	24.89	25.91	0.980	1.020
e	15.62	16.13	0.615	0.635
e_1	2.92	3.43	0.115	0.135
L	12.32	–	0.485	–
L_1	2.79	3.30	0.110	0.130
ØP	3.84	4.09	0.151	0.161
Q	38.35	38.86	1.510	1.530
R	4.19	4.44	0.165	0.175
S	4.57	4.95	0.180	0.195

Hermetic Power Module (Straight Lead)



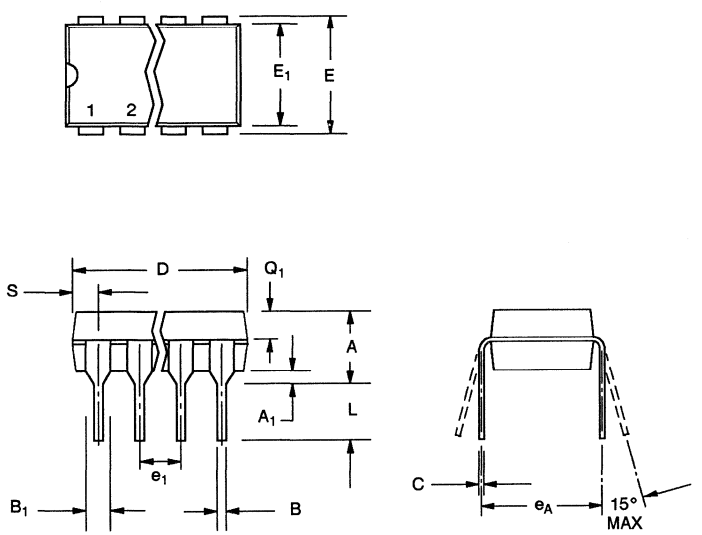
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	0.240	0.280
A_1	1.14	1.40	0.045	0.055
Øb	0.89	1.14	0.035	0.045
D	24.89	25.91	0.980	1.020
E	24.89	25.91	0.980	1.020
e	15.62	16.13	0.615	0.635
e_1	2.92	3.43	0.115	0.135
J_1	3.56	4.06	0.140	0.160
L	6.35	–	0.250	–
ØP	3.84	4.09	0.151	0.161
Q	38.35	38.86	1.510	1.530
R	4.19	4.44	0.165	0.175
S	4.57	4.95	0.180	0.195

PLCC Package (N, P Suffix), 20 Leads



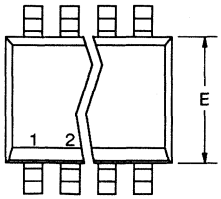
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
A_2	0.51	–	0.020	–
B	0.331	0.553	0.013	0.021
B_1	0.661	0.812	0.026	0.032
D	9.78	10.03	0.385	0.395
D_1	8.890	9.042	0.350	0.356
D_2	7.37	8.38	0.290	0.330
e_1	1.27 BSC		0.050 BSC	

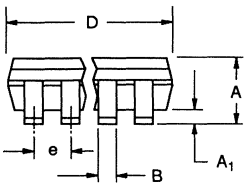
Plastic DIP (J, N Suffix), 8–16 Leads

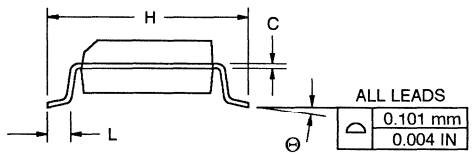


DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D-8	9.65	11.68	0.380	0.460
D-14	17.27	19.30	0.680	0.760
D-16	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	3.175	3.81	0.125	0.150
Q_1	1.27	2.03	0.050	0.080
S-8	1.02	2.03	0.040	0.080
S-14	1.02	2.03	0.040	0.080
S-16	0.38	1.52	0.015	0.060

SO Package (Y Suffix), 8–16 Leads

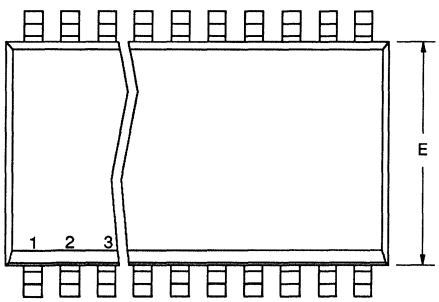




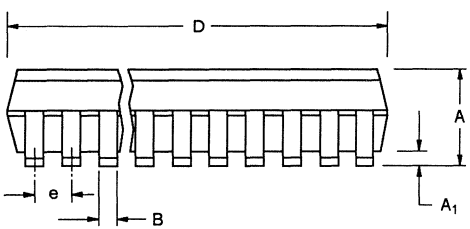


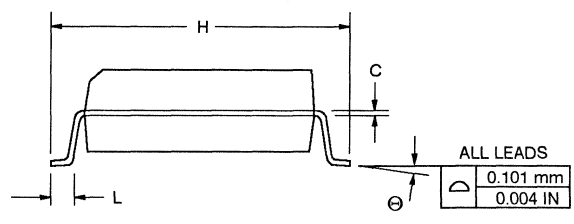
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-14	8.35	8.95	0.329	0.352
D-16	9.60	10.20	0.378	0.402
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

SO Package (Y Suffix), 20–28 Leads

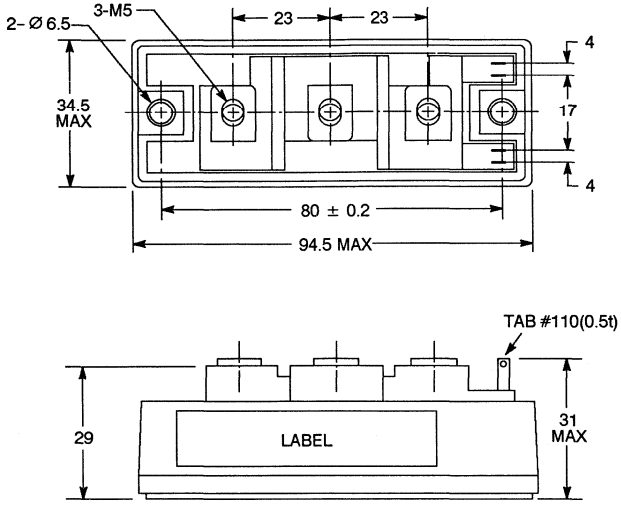


DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.15	2.90	0.085	0.114
A_1	0.10	0.30	0.004	0.012
B	0.35	0.45	0.014	0.018
C	0.23	0.28	0.009	0.011
D-20	12.50	13.30	0.492	0.524
D-24	15.05	15.85	0.593	0.624
D-28	17.60	18.40	0.693	0.724
E	7.25	8.00	0.285	0.315
e	1.27 BSC		0.050 BSC	
H	9.80	10.60	0.386	0.417
L	0.60	1.00	0.024	0.039
Θ	0°	8°	0°	8°



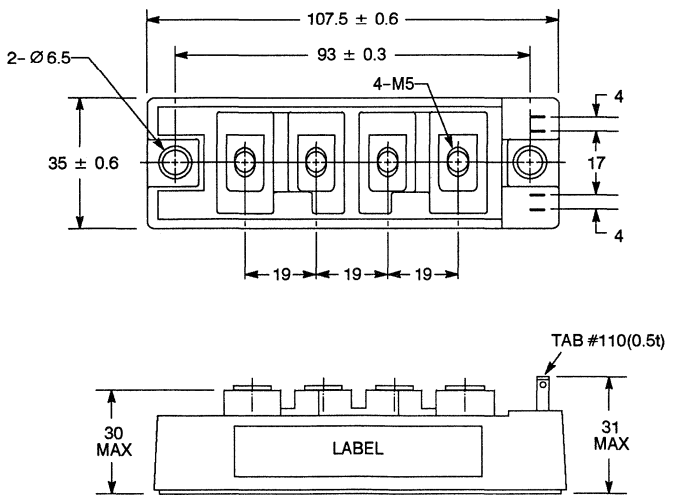


SPMB50A500



NOTE: ALL DIMENSIONS IN MILLIMETERS

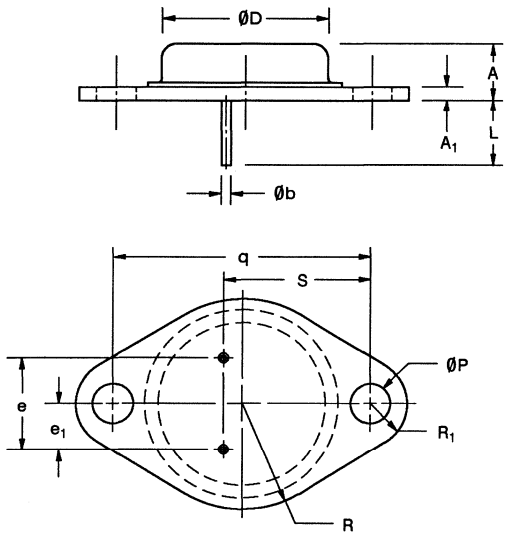
SPMF50A500



NOTE: ALL DIMENSIONS IN MILLIMETERS

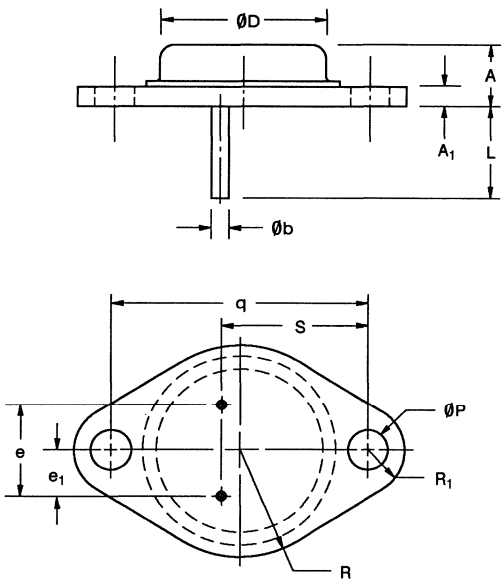
8

TO-204 AA



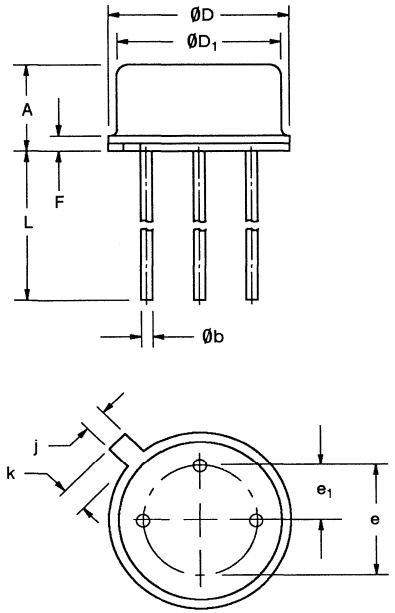
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.35	8.89	0.250	0.350
A_1	–	3.43	–	0.135
Øb	0.96	1.09	0.038	0.043
ØD	–	22.22	–	0.875
e	10.67	11.18	0.420	0.440
e_1	5.21	5.72	0.205	0.225
L	7.92	–	0.312	–
ØP	3.84	4.09	1.51	0.161
q	30.15 BSC		1.187 BSC	
R	–	13.34	–	0.525
R_1	–	4.78	–	0.188
S	16.64	17.14	0.655	0.675

TO-204 AE



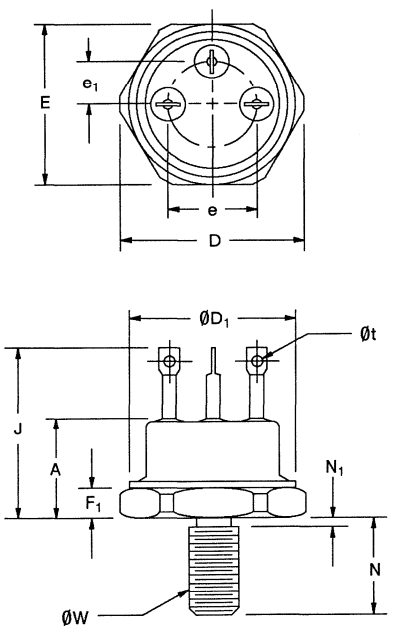
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.35	8.89	0.250	0.350
A_1	1.52	3.43	0.060	0.135
Øb	1.45	1.60	0.057	0.063
ØD	–	22.22	–	0.875
e	10.67	11.18	0.420	0.440
e_1	5.21	5.72	0.205	0.225
L	10.92	12.19	0.430	0.480
ØP	3.84	4.09	1.51	.161
q	30.15 BSC		1.187 BSC	
R	12.57	13.34	0.495	0.525
R_1	–	4.78	–	0.188
S	16.64	17.14	0.655	0.675

TO-205 AF



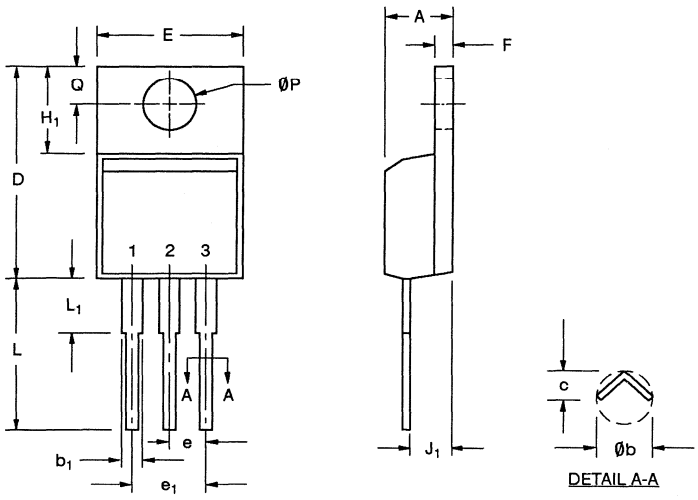
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.07	4.57	0.160	0.180
Øb	0.41	0.53	0.016	0.021
ØD	8.64	9.39	0.340	0.370
$ØD_1$	8.01	9.01	0.315	0.335
e	5.08 BSC		0.200 BSC	
e_1	2.54 BSC		0.100 BSC	
F	0.23	1.04	0.009	0.041
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	19.05	0.500	0.750

TO-210 AC



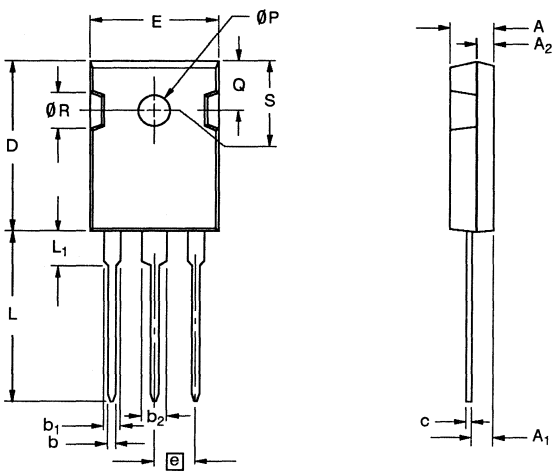
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.67	11.43	0.420	0.450
D	18.80	19.30	0.740	0.760
$ØD_1$	16.38	17.40	0.645	0.685
E	17.14	17.40	0.675	0.685
e	9.91	10.41	0.390	0.410
e_1	4.83	5.33	0.190	0.210
F_1	3.30	3.56	0.130	0.140
J	19.05	20.45	0.750	0.805
N	10.72	11.56	0.422	0.455
N_1	–	1.27	–	0.050
Ø t	1.32	1.57	0.052	0.062
ØW	1/4-28 UNF-2A		1/4-28 UNF-2A	

TO-220 AB



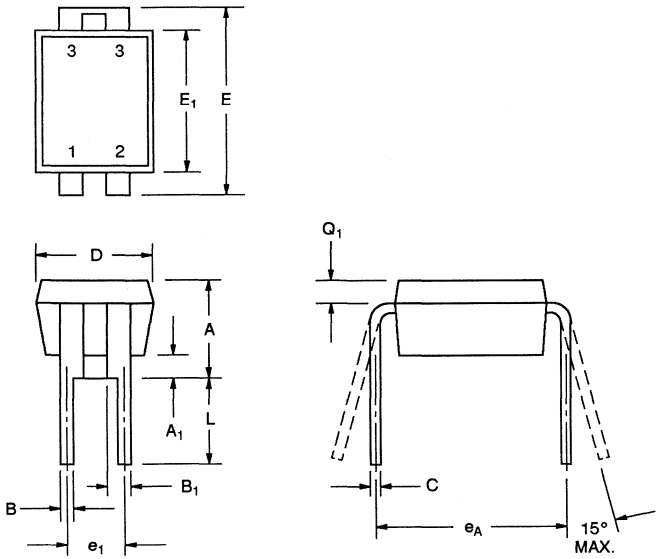
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.70	0.170	0.185
b_1	1.27	1.65	0.050	0.065
Øb	0.76	1.02	0.030	0.040
c	0.38	0.76	0.015	0.030
D	14.60	15.49	0.575	0.610
E	10.03	10.41	0.395	0.410
e	2.41	2.67	0.095	0.105
e_1	4.95	5.33	0.195	0.210
F	1.14	1.40	0.045	0.055
H_1	5.97	6.73	0.235	0.265
J_1	2.41	2.79	0.095	0.110
L	13.08	14.22	0.515	0.560
L_1	–	3.81	–	0.150
ØP	3.68	3.94	0.145	0.155
Q	2.54	3.05	0.100	0.120

TO-247 AD



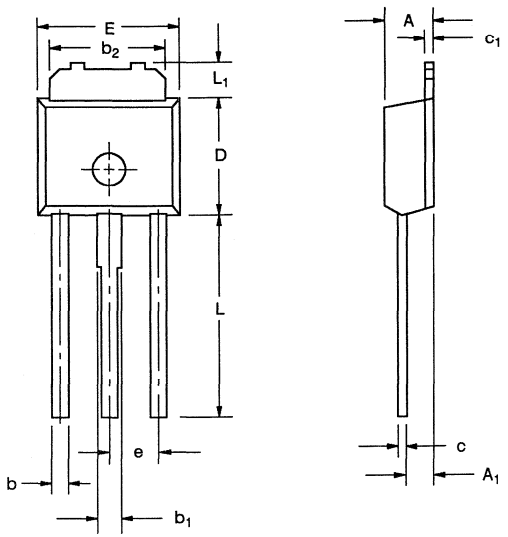
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.70	5.30	0.185	0.209
A_1	2.20	2.59	0.087	0.102
A_2	1.50	2.50	0.059	0.098
b	1.02	1.40	0.040	0.055
b_1	1.65	2.13	0.065	0.084
b_2	2.87	3.13	0.113	0.123
c	0.40	0.79	0.016	0.031
D	20.80	21.46	0.819	0.845
E	15.49	16.26	0.610	0.640
e	5.46 BSC		0.215 BSC	
L	19.81	20.32	0.780	0.800
L_1	–	4.50	–	0.177
ØP	3.56	3.66	0.140	0.144
Q	5.38	6.20	0.212	0.244
ØR	4.32	5.49	0.140	0.216
S	5.84	6.48	0.230	0.255

TO-250



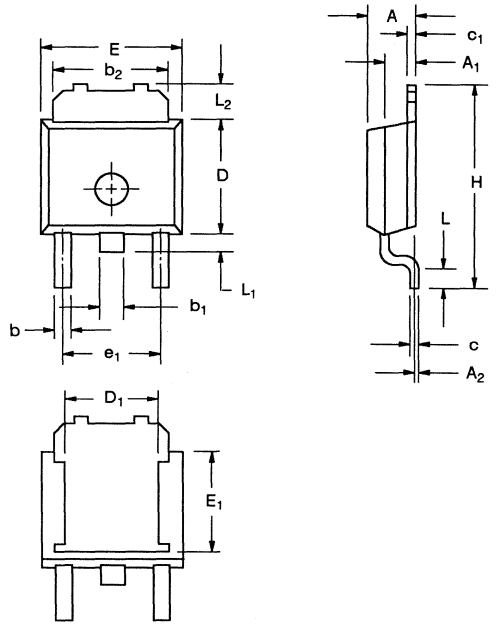
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	4.57	0.160	0.180
A_1	0.89	1.40	0.035	0.055
B	0.51	0.61	0.020	0.024
B_1	0.89	1.14	0.035	0.045
C	0.33	0.43	0.013	0.017
D	4.93	5.03	0.194	0.198
E	7.62	8.26	0.300	0.325
E_1	5.97	6.48	0.235	0.255
e_1	2.29	2.79	0.090	0.110
e_A	7.62	7.87	0.300	0.310
L	3.18	4.06	0.125	0.160
Q_1	0.86	1.12	0.034	0.044

TO-251



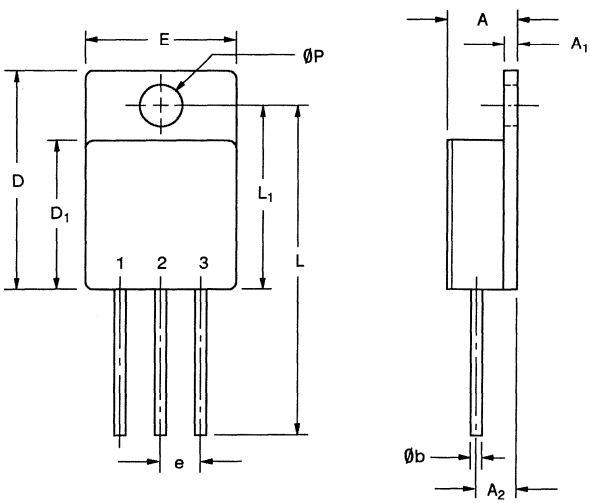
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
A_1	0.89	1.50	0.035	0.059
b	0.70	0.90	0.028	0.035
b_1	1.10	1.20	0.043	0.047
b_2	5.30	5.50	0.209	0.216
c	0.25	0.45	0.010	0.018
c_1	0.45	0.55	0.018	0.022
D	5.40	6.22	0.213	0.245
E	6.40	6.60	0.252	0.260
e	1.79	2.79	0.070	0.110
L	8.89	–	0.350	–
L_1	0.88	2.20	0.035	0.087

TO-252



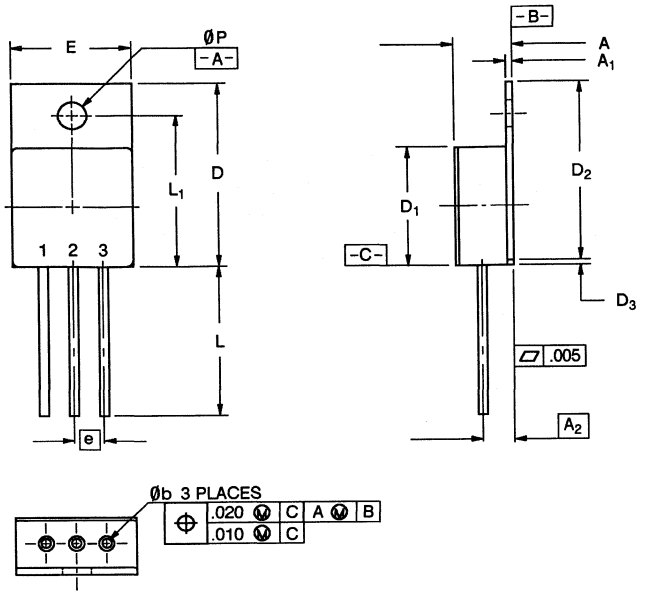
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
A_1	0.89	1.50	.035	.059
A_2	0.03	0.23	0.001	0.009
b	0.70	0.90	0.028	0.035
b_1	1.10	1.20	0.043	0.047
b_2	5.30	5.50	0.209	0.216
c	0.25	0.45	0.010	0.018
c_1	0.45	0.55	0.018	0.022
D	5.40	6.22	0.213	0.245
D_1	4.00	5.00	0.158	0.197
E	6.40	6.60	0.252	0.260
E_1	3.18	3.67	0.125	0.145
e_1	3.97	5.17	0.156	0.204
H	8.80	10.60	0.346	0.417
L	0.25	–	0.10	–
L_1	0.5	1.2	0.020	0.048
L_2	0.88	2.20	0.035	0.087

TO-254 AA



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.32	6.60	0.249	0.260
A_1	1.02	1.27	0.040	0.050
A_2	3.81 BSC		0.150 BSC	
Øb	0.89	1.14	0.035	0.045
D	20.07	20.32	0.790	0.800
D_1	13.59	13.84	0.535	0.545
e	3.81 BSC		0.150 BSC	
E	13.59	13.84	0.535	0.545
L	30.35	31.40	1.195	1.235
L_1	16.89	17.40	0.665	0.685
ØP	3.53	3.78	0.139	0.149

TO-257 AB



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	5.33	–	0.210
A_1	0.64	0.89	0.025	0.035
A_2	2.79 BSC		0.110 BSC	
Øb	0.89	1.14	0.035	0.045
D	16.26	17.02	0.645	0.665
D_1	10.41	10.92	0.410	0.430
D_2	16.26	17.02	0.645	0.665
D_3	–	0.51	–	0.020
e	2.54 BSC		0.100 BSC	
E	10.41	10.92	0.410	0.430
L	12.70	14.73	0.500	0.580
L_1	13.20	13.72	0.520	0.540
ØP	3.56	3.81	0.140	0.150

TABLE OF CONTENTS

Low-Power Universal-Input Power Supply Achieves High Efficiency

Craig Varga

Expanding global markets have created a demand for what have become known as universal-input power supplies -- that is, power supplies that allow devices to be plugged into wall outlets anywhere in the world. These power supplies must be able to operate directly from 100-, 110-, and 220-V ac power lines without the use of selector switches or jumpers. A power supply with the ability to operate under such conditions while remaining cost-effective is now becoming a necessity.

In the under 30-W power range, meeting the above requirements while maintaining high efficiency has been a challenge. Add to this the need to meet various international safety standards, and the circuit designer has his hands full.

The demands of low-power universal-input power supplies are met by the Si9120 pulse width modulation (PWM) controller from Siliconix. Using the Si9120, the flyback circuit presented in this application note demonstrates that designing universal-input supplies can be a simple task.

Circuit Topology

For the low power levels that are of interest here (under 30 W), the discontinuous-mode (DCM) flyback converter is the preferred topology. The biggest advantage of this topology is simplicity. The parts count in the power path cannot get any lower.

The peak-to-average primary current ratio in a DCM flyback is high relative to other topologies; however, at low power levels, this is not a serious drawback. On-state losses are minimal. Magnetics are small. Also, the transformer reset voltage is set by the minimum input voltage and remains fairly constant as the line voltage changes. As a result, a 600-V MOSFET proves adequate, even with ac inputs up to 300 V RMS.

The DCM flyback converter, when operated under current-mode control, provides a natural input volt-second limit, which helps keep the drain voltage from getting out of control during line or load transient conditions. Also, today's power MOSFETs are able to withstand avalanche current many times greater than a low power circuit can typically deliver (see appendix A). As such, the MOSFET will serve as a clamp for the occasional spike which may result from a short circuit or extreme load transient.

Cross regulation is fairly good, especially if leakage inductance between windings can be kept low.[1] In a universal-input application, meeting VDE input-to-output isolation requirements is essential. Depending on the end product, this can be as high as 3750 V RMS, primary to secondary -- a figure that is totally inconsistent with the desire to achieve low leakage inductance. As a result, cross regulation between primary and secondary-referenced windings will be poor. This complicates the regulation of the primary-side bootstrap winding used to avoid secondary-to-primary feedback across the isolation boundary. The addition of a simple spike-blanking circuit solves the problem (see AN90-2, "Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC").

When using the Si9120 for universal-input applications, it is recommended that a bootstrap winding be employed. While not strictly necessary, the power dissipation and chip temperature are higher if bootstrapping is not utilized. As an example, at V_{in} = 400 V dc and I_{CC} = 1.5 mA, the power dissipation on the chip without a bootstrap is 600 mW. If a 10 V bootstrap supply is used, the dissipation is only 15 mW. This becomes more of a concern as the gate charge requirements of the power MOSFET increase, since the value of I_{CC} for the controller is largely dependent on gate drive demands.

Another advantage of the DCM flyback converter is its single-pole loop response. This makes compensating the feedback loop comparatively simple. In addition, transient response can be quite good in DCM flyback converters. It is possible (though not practical in a closed-loop system) to slew the power stage from no load to full load in only one switching cycle.

Design Example

The circuit shown in Figure 1 is an 11.1-W, 3-output off-line supply. The input voltage is specified from 90 to 260 V ac. Outputs are +5 V at 1.5 A, +12 V at 150 mA, and -12 V at 150 mA. The design features full VDE isolation, primary side regulation, and true foldback current limiting. Operating frequency is 100 kHz.

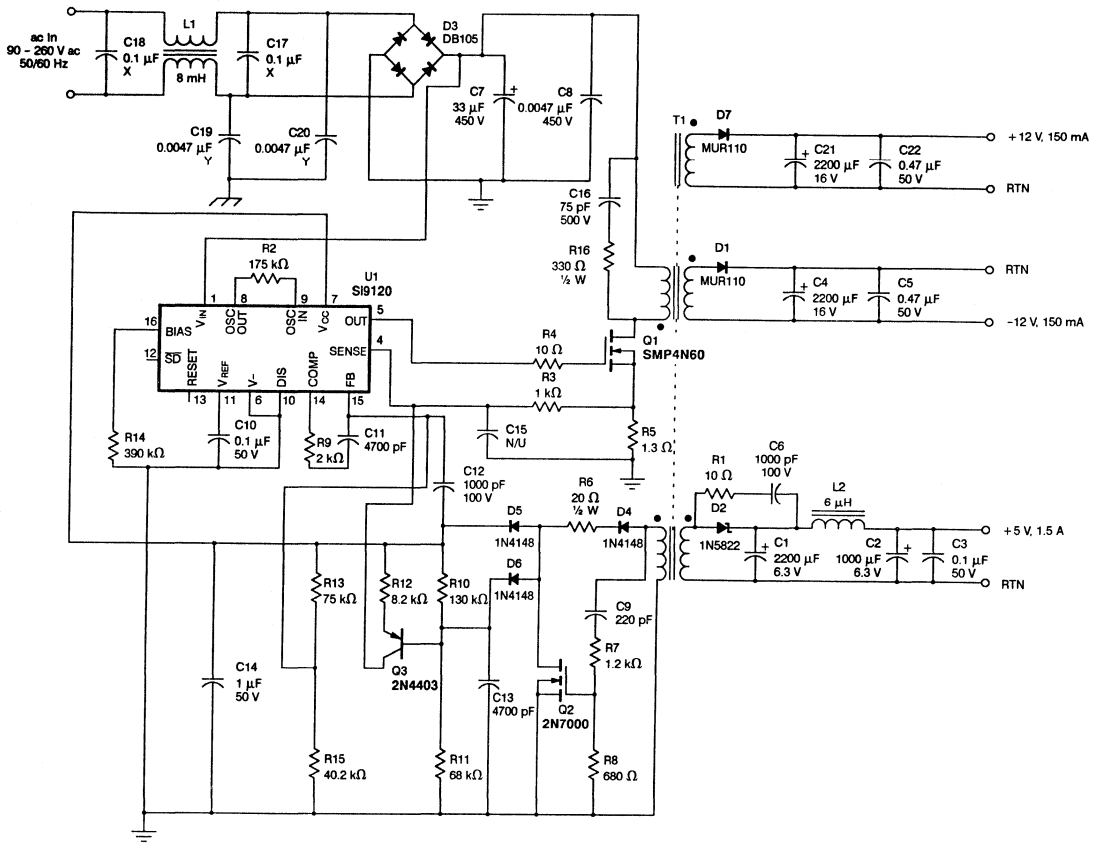


Figure 1. Schematic for Universal-Input Power Supply

DCM flyback operating principles are generally well understood and will not be presented here. Refer to Siliconix Application Note 90-2 for a detailed design example. References 2 and 3 are also recommended.

Sizing the input capacitor and rectifiers for universal input requires more thought than for comparable single-input converters. Keep in mind that while the maximum input voltage occurs at high-input line, the maximum current stresses will occur at low line. This implies that the input capacitor value must be sized at low line while the voltage rating is dictated by the high-line condition. The bridge rectifier should be rated at 600 V dc minimum. The RMS current rating is calculated below.

For the present example:

$$\text{Output power} = 5.0\ \text{V} \times 1.5\ \text{A} + 12\ \text{V} \times 0.15\ \text{A} \times 2$$
$$= 11.1\ \text{W}$$

If efficiency is assumed to be 70%,

$$\text{Input power} = 11.1\ \text{W}/0.7$$
$$= 15.86\ \text{W}.$$

For a little cushion, assume a low-input line voltage of 85 V ac.

Thus,

$$V_{dc} = 85\sqrt{2} = 120\ \text{V dc}.$$

Assuming a 20-V pk-pk input-capacitor ripple voltage the minimum voltage is

$$V_{min} = 120\ V - 20\ V = 100\ V.$$

$$I_{in} = P_{in}/V_{dc}$$

$$= 15.86\ W/\ 100\ V = 0.1586\ A$$

$$C = I\frac{dt}{dV}$$

$$= \frac{0.1586\ A \times 0.01\ s}{20\ V}$$

$$= 79\ \mu F$$

68 μF is a standard value. With 68 μF, the ripple voltage is

$$V_{pp} = I\frac{dt}{C}$$

$$= \frac{0.16\ A \times 0.01\ s}{68E\text{-}6\ F}$$

$$= 23.5\ V, \text{ an acceptable value.}$$

The capacitor voltage rating is calculated:

$$V_{max} = 260\ V\ ac \times \sqrt{2}$$

$$= 368\ V\ dc.$$

A 400 V capacitor is acceptable. A rating of 450 V dc is preferable if high reliability is required or significant line transients are expected.

Assuming a power factor of 0.65, the RMS input current is

$$I_{ac} = \frac{P_o}{\eta\ V_{ac}\ (PF)}$$

$$= \frac{11.1\ W}{(0.7)\ (85\ V)\ (0.65)}$$

$$= 0.287\ A$$

A 1-A bridge rectifier is more than adequate.

The primary inductance value is chosen by analyzing the lowest input voltage case. For a given load, the value of the peak transformer primary current will remain constant regardless of the input voltage. Since the primary inductance is fixed, the time to ramp to a given value of current is inversely proportional to input voltage (V = Ldi dt). Therefore, low line is where the most time is needed to ramp to the desired primary current. The duty factor limit dictates an on-time limit. After choosing an operating frequency and calculating the peak primary current, a value for primary inductance, L_P, can be determined as follows:

For 100 kHz, period = 10 μs.

At 50% duty factor, $t_{on(max)} = 5\ \mu s$.

$$I_{pk} = I_{in} \times 4$$

$$= (0.1586\ A)\ (4)$$

$$= 0.634\ A\ pk.$$

For V_{in} (dc) = 100 V

$$L = V\frac{dt}{di}$$

$$= \frac{(100\ V)\ (5E\text{-}6\ s)}{0.634\ A}$$

$$= 788\ \mu H.$$

The actual inductance used was 735 μH. [For high-volume production applications, the design engineer should consider the worst case tolerances for clock frequency and inductor value.]

See AN90-2 for transformer design equations and a fully worked example.

The biggest considerations for universal input are related to the additional insulation required to comply with VDE isolation specifications. The physical space occupied by the insulation typically reduces the useable fill factor to 25%. Furthermore, the increase in leakage inductance caused by large physical separation of the windings has the undesirable effects of creating large voltage spikes on the power MOSFET drain, contributing to power losses, and degrading load regulation.

Barrier tape at window ends will take up a lot of useable space, so a core geometry with a long, low window should be selected to minimize wasted area. This has the added benefit of reducing leakage inductance. (See equation 6.4 of reference 4.)

Wind the primary first. Apply the required insulation, and then wind the secondaries. All secondaries should be wound together with no intervening insulation, if voltage levels allow. Optimal cross regulation is achieved in this way.

Further reductions in leakage inductance can be realized by using interleaved windings. First wind one half of the primary, followed by the secondaries and remaining primary turns. The multiple primaries are usually connected in parallel. The spike blanking circuit described in AN90-2 virtually eliminates the primary-to-secondary leakage inductance problems, at least from the standpoint of the regulation effects.

In selecting a power MOSFET, the main concerns will be the $r_{DS(on)}$ and the drain voltage ratings. The transformer primary voltage during the off time is $V_P = (V_o + V_D)\ N_P/N_S$. Using the 5-V winding,

$$V_P = (5.0\,V + 0.4\,V)\,(45\,T/7\,T) = 81\,V$$

Therefore,

$$V_{DS(off)} = V_{in(max)} + V_P$$
$$= 368\,V + 81\,V = 449\,V.$$

A 600 V MOSFET allows for a 150 V spike due to leakage inductance at high line. The RC snubber was sized empirically to keep the peak drain voltage below 600 V.

The SMP4N60 is the smallest 600-V device available. At 25°C the $r_{DS(on)}$ is 2.0 Ω. At 100°C, $r_{DS(on)}$ = 1.75 x 2 Ω = 3.5 Ω. The peak drain current was previously calculated at 0.634 A. The maximum RMS drain current is given by

$$I_{RMS} = I_{pk}(D/3)^{1/2}$$
$$= 0.634\,A\left(\sqrt{\frac{0.5}{3}}\right)$$
$$= 0.26\,A.$$

On-state losses are given by

$$P_{on} = I_{RMS}^2 \times r_{DS(on)}$$
$$= (0.26\,A)^2 \times 3.5\,\Omega$$
$$= 237\,mW.$$

Switching losses are estimated at 350 mW. Since the thermal resistance is specified at 80°C/W, a total temperature rise of 47°C is expected. This permits operation up to approximately 50°C ambient temperature, while holding the maximum junction temperature to 100°C.

Something of more concern for universal-input than for a single-input voltage supply is the range of duty factor to be expected. Since the on time varies inversely with input voltage, the high-line on-time can become quite small in a high-frequency converter. For this kind of application, try to keep the minimum on time to not much less than 1 μs. This will help minimize noise problems with the current sense.

Also, be sure to use a non-inductive resistor for the current sense (carbon composition or film type). Use of a wire-wound resistor will produce large spikes which have to be filtered out. The dual-delay current-limit comparators of the Si9120 will frequently eliminate the need for a current-sense filter altogether. The magnitude of the noise on the current sense voltage will be affected by transformer parasitic capacitances and PCB layout. As such, every design will exhibit slightly different characteristics. Careful attention to detail in the magnetics design and construction as well as the board layout is a must.

For designs using current-sense resistors in the power MOSFET's source leg, note that the gate drive current is "seen" by the sense resistor. In very low-power designs, this can easily exceed the full load sense voltage causing severe noise problems. Adding a fairly large-value gate resistor will help in this case. Also, an RC current-sense filter becomes much more important.

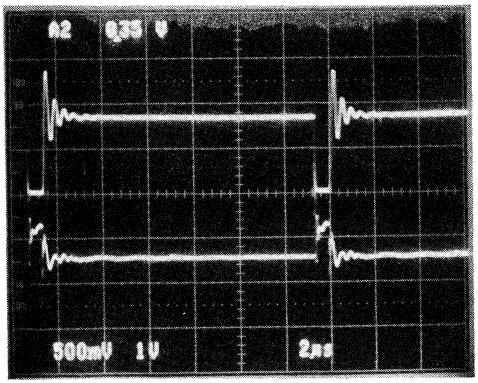
Foldback Circuit

Foldback current limiting is provided by Q3 and its associated components. Under normal operating conditions, diode D6 keeps C13 charged to V_{CC}. Hence, Q3 is biased off. In the event of a short circuit on any output, all winding voltages are clamped low. This causes the voltage on C13 to drop to a level set by divider R10 and R11. V_{CC} is held at 8.6 V by the Si9120's start-up regulator. The current set by the value of R12 flows through Q3 and R3, and causes the voltage on pin 4 to rise. Since a peak threshold of 1.2 V is internally set on pin 4, the voltage required across R5 to terminate a pulse is reduced by an amount equal to the drop on R3.

$$I_D = \{1.2 - (I_{Q3})(R3)\}/R5.$$

Thus as I_{Q3} increases, I_D decreases.

See Figure 2a for foldback operating waveforms.



Short Circuit On 5 V Output

Q1 Drain Voltage (100 V/Div)

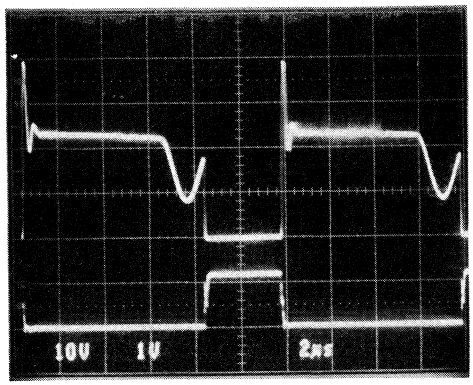
– 0

Voltage On U1, Pin 4 (Current Sense) (0.5 V/Div)

– 0

NOTE: 0.8 V dc pedestal caused by the foldback circuit.

a)



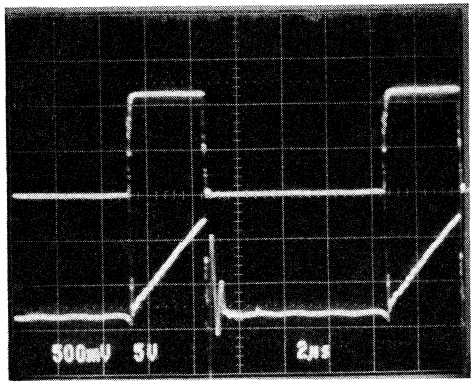
Q1 Drain Voltage (100 V/Div)

– 0

– 0

Q1 Gate Voltage (100 V/Div)

b)



Q1 Gate Drive (5 V/Div)

– 0

Voltage On U1, Pin 4 (Current Sense) (0.5 V/Div)

– 0

c)

Figure 2. Operating Waveforms (all photos full load, V_{in} = 150 V dc)

9

The foldback circuit will not perform correctly without the spike blanking circuit. The leakage spike will peak charge C13 even with a shorted load. However, the foldback function is completely optional and all associated components can be eliminated if a lower cost supply is desired.

Test Results

Data compiled on the test circuit appear in Table 1. Combined line and load regulation measures ±2.7%, well within a ±5% specification. Measured efficiency is 73.4% with no effort at optimization. A detailed loss assessment could, no doubt, offer some improvements. Pulse load tests show reasonable transient response, and phase margin is measured at 60 degrees. For details on how to close the feedback loop, refer to Siliconix application notes AN87-1 and AN90-2.

Table I. Universal-Input Supply Test Data

All data taken with dc input source to ensure stable readings.

Full Load:				
V_{in} (dc)	**I_{in} (mA)**	**+5 V**	**+12 V**	**-12 V**
100 V	143.9	4.974	12.64	12.50
200 V	72.3	5.014	12.76	12.61
300 V	48.9	5.027	12.79	12.65
385 V	39.4	5.049	12.81	12.67
Half Load:				
100 V	78.0	5.153	12.99	12.83
200 V	40.3	5.205	13.10	12.96
300 V	27.9	5.235	13.12	12.97
385 V	23.0	5.254	13.14	13.01

Pk-Pk Output Ripple Voltages (Spikes Not Included)		
5 V	+12 V	-12 V
60 mV	45 mV	40 mV

NOTE: Worst case over full line-voltage range.

Measured efficiency at V_{in} = 300 V_{dc} was 73.4%.

During testing, an input capacitor value of as little as 33 µF proved adequate versus the design value of 68 µF. The low-value capacitor produces an input ripple voltage of 30 V pk-pk. Since the primary inductance is slightly lower than the design maximum value, the circuit is still able to maintain regulation with the higher input ripple voltage value. This is a good example of where trade-offs can be made during development programs. By using the larger input capacitance and primary inductance, the peak input current could be reduced slightly, and a slight improvement in efficiency should result. However, a larger input capacitance will decrease the conduction angle of the input rectifiers, and consequently will reduce the input power factor. The priorities of a particular application will determine the optimal approach.

Conclusion

The simple universal-input power supply design that has been presented combines economy and performance which should prove more than adequate for the majority of applications. The overall cost of the supply should rival linear regulators of similar power level if heatsink cost is considered. Good regulation has been achieved while maintaining the 3750 V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for any external start-up circuitry. Also, foldback current-limiting is demonstrated which requires no feedback across the isolation boundary.

Appendix A

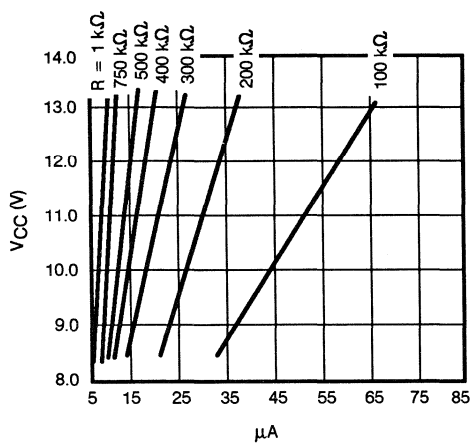
The SMP4N60 was tested for ability to withstand repetitive avalanche currents and for non-repetitive capability. Inductance values of 12 µH and 94 µH were used. Repetitive tests were run at 3 A, with 94 µH at 25°C. Failure current was measured at 25°C and 100°C. Results were as follows:

L = 94 µH		L = 12 µH	
25°C	100°C	25°C	100°C
4.25 A	2.40 A	7.28 A	6.40 A

For the 11.1-W flyback supply presented here, the leakage inductance is specified at 60 µH maximum. The maximum drain current is set to approximately 1.0 A. Therefore, based on the above data, adequate margin is present to prevent avalanche failure.

Appendix B

A number of performance parameters of the Si9120 can be altered by setting I_{bias} to a value other that 15 µA. At lower I_{bias}, higher efficiency can be obtained. At higher I_{bias}, lower propagation delays and a wider error amplifier bandwidth are possible. Also, if a V_{CC} supply other than 10 V is used, R_{bias} should be something other than 390 kΩ. Figure 3 below relates V_{CC} to R_{bias} and typical I_{bias}. The equation given can be used for points not on the graph.



$$R_{bias} = \frac{V_{CC} - 2.3\ V - 484\sqrt{I_{bias}}}{I_{bias}}$$

Figure 3. Relationship of V_{CC} to R_{bias} and Typical I_{bias}

References

1) Liu, K.H., "Effects of Leakage Inductance on the Cross Regulation in a Discontinuous-Mode Flyback Converter," Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., "High Frequency Switching Power Supplies," McGraw Hill 1984.

3) Billings, K., "Switchmode Power Supply Handbook," McGraw Hill 1989.

4) McLyman, Col. W.T., "Transformer and Inductor Design Handbook," McGraw Hill 1988.

Universal Input Power Supply Parts List

C1	2200 µF, 6.3 V Al. Electrolytic - United Chemicon SXC
C2	1000 µF, 6.3 V Al. Electrolytic - United Chemicon SXC
C3, C10	0.1 µF, 50 V Ceramic
C4, C21	2200 µF, 16 V Al. Electrolytic - United Chemicon SXC
C5, C22	0.47 µF, 50 V Ceramic
C6, C12	1000 pF, 100 V Ceramic
C7	33 µF, 450 V Al Electrolytic (400 V ok)
C9	220 pF, 100 V Ceramic
C11, C13	4700 pF, 100 V Ceramic
C14	1 µF, 50 V Ceramic
C16	75 pF, 500 V Ceramic or Mica
C17, C18	0.1 µF, 250 V,ac VDE Class X2 Wima MKS 4-R
C8, C19, C20	0.0047 µF, 250 V,ac VDE Class Y Wima MP3-Y
D1, D7	MUR 110 Motorola 1 A 100 V
D2	1N5822 3 A, 40 V Schottky
D3	Bridge 1 A, 600 V DB105
D4, D5, D6	1N4148
L1	Common mode choke Renco 1361-2
L2	Inductor 6 µH, 1.5 A
Q1	FET N-channel SMP4N60 Siliconix
Q2	FET N-channel 2N7000 Siliconix
Q3	2N4403 PNP (or 2N2907)
R1, R4	10 Ω,, 1/8 Carbon Film or Metal Film
R2	175 kΩ, 1/8 W Carbon Film or Metal Film
R3	1 kΩ, 1/8 W Carbon Film or Metal Film
R5	1.3 Ω, 1/4 W Carbon Film or Metal Film
R6	20 Ω, 1/2 W Carbon Film or Metal Film
R7	1.2 kΩ, 1/8 W Carbon Film or Metal Film
R8	680 Ω, 1/8 W Carbon Film or Metal Film
R9	2 kΩ, 1/8 W Carbon Film or Metal Film
R10	130 kΩ, 1/8 W Carbon Film or Metal Film
R11	68 kΩ, 1/8 W Carbon Film or Metal Film
R12	8.2 kΩ, 1/8 W Carbon Film or Metal Film
R13	75 kΩ, 1/8 W 1% Carbon Film or Metal Film
R14	390 kΩ, 1/8 W Carbon Film or Metal Film
R15	40.2 kΩ, 1/8 W 1% Carbon Film or Metal Film
R16	330 Ω, 1/2 W 5% Carbon Composition
T1	Schott Corp. #67122700

Siliconix incorporated

Thermal Characteristics of Siliconix' Surface-Mount MOSFET Half-Bridges

Jim Harnden

Although a wide selection of digital and linear ICs have been available in surface-mount packages for some time, circuits that require power devices have, for the most part, required "mixed-technology" assembly processes. Several versions of DPAK and SOT packages evolved in an attempt to provide compatible discrete solutions. Both, however, have limitations. The DPAK provides, at best, tolerable compatibility with other surface-mount components, and it offers little density advantage over "through-hole" technologies. SOT packages are more compatible with standard SOIC (small outline IC) packaging but have severely limited thermal transfer capabilities. And they accommodate only the smallest power MOSFET die. Siliconix' family of surface-mount MOSFET half-bridges provides a much more flexible, cost-effective alternative. This packaging innovation is based on 1) low resistance MOSFETs, 2) the density advantages of higher level integration, and 3) copper lead-frames for improved thermal transfer characteristics.

While small-outline (SO-8 and SO-16) surface-mount packages offer limited potential for direct heat dissipation, the copper lead-frames designed for the Si995x surface-mount half-bridge family maximize heat transfer to the PC board. This reduced thermal impedance, combined with the availability of very low on-resistance MOSFETs, greatly extends the range of surface-mount technology in power applications.

The copper lead-frames are designed to bring the die bond pad directly in contact with PC board traces through as many pins as possible. In SOIC packaging, the close proximity of the silicon die to the PC board contributes to efficient thermal transfer. Because its mass is considerably greater than that of the die, the copper lead-frame also serves as a very efficient heat spreader.

With discrete (vertical conduction) MOSFETS, the bottom of both p- and n-channel die serve as drain connections. When a p-channel upper device and an n-channel lower device are combined in a half-bridge configuration, their common (output) connection is their two drains. With the Si9950DY and Si9954DY, ten of the package's sixteen pins are directly connected to this common die bond pad and become the output connection to the PC board (Figure 1).

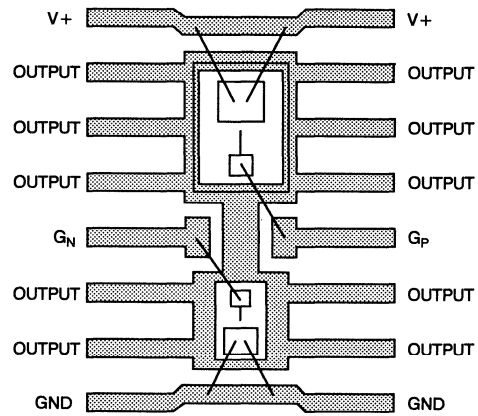


Figure 1. Si9950DY and Si9954DY Leadframe

An n-channel half-bridge requires isolation of the two devices in order to allow connection of the upper device's source with the drain of the lower device. The Si9955DY and Si9956DY contain two isolated n-channel devices with the drains of each attached to separate die bond pads which are brought out on two pins each (Figure 2).

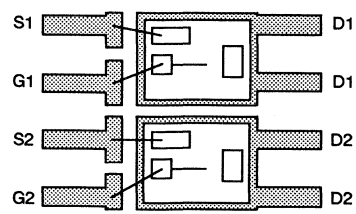


Figure 2. Si9955DY and Si9956DY Leadframe

The Si9951DY is a monolithic complementary half-bridge constructed on a self-isolating power IC process. The substrate (ground) of the Si9951DY is connected to the PC board through two pins that are common to the copper lead-frame (Figure 3).

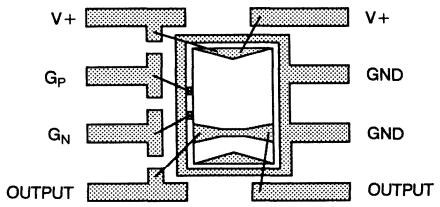


Figure 3. Si9951DY Leadframe

The common multi-layer PC board and its printed copper conductors can play a significant role in dissipating heat from electrical components. Unfortunately the extent of the effect on a working circuit board is almost impossible to calculate with any precision. While the thermal conductivity of various weights of copper clad and PC board material are well characterized and available (see references), the proximity of neighboring components on densely populated surface-mount boards, the effects of multi-layer board construction, solder masks, etc., dominate the equations. The references at the end of this application note are offered for those attempting a thermal model; but, to date, significant data has come only from characterization of "best-" and "worst-case" prototypes.

Thermal Transfer Characterization

The data presented here was obtained using the MOSFET's intrinsic diode to measure the die junction temperature. The thermal characteristics of each MOSFET's intrinsic diode have been determined; thus, the diode provides a predictable thermal sensor located precisely at the junction in question. At the beginning of each thermal dissipation test, the diode was first measured to determine the die's "ambient" starting temperature (Figure 4a). The device was then forced to dissipate a controlled power level (Figure 4b) for a precise amount of time, and the diode was immediately remeasured to determine the resulting junction temperature increase (Figure 4c). During step two (Figure 4b), the power level was regulated by applying a drain voltage (5 V) and varying the MOSFET's gate voltage to yield a programmed drain current consistent with the desired power level of each test. (The power level was increased proportionally for shorter pulse durations to increase resolution.)

The complete series of tests was performed for each die on each lead frame connected to thermally "best-" and "worst-case" PC board layouts. The PC board layouts tested are reproduced (1:1) next to each set of results (Figures 5, 6, and 7). Actually, the layout representing the best case is more correctly a single-sided, maximum-copper, one-inch-square board that is easily surpassed by the thermal dissipation of the larger, multi-layered boards used in most applications. The worst-case example employs the "standard" spacing and trace width used for non-power devices. The worst-case example was coated with a solder mask and the best-case example was left uncoated.

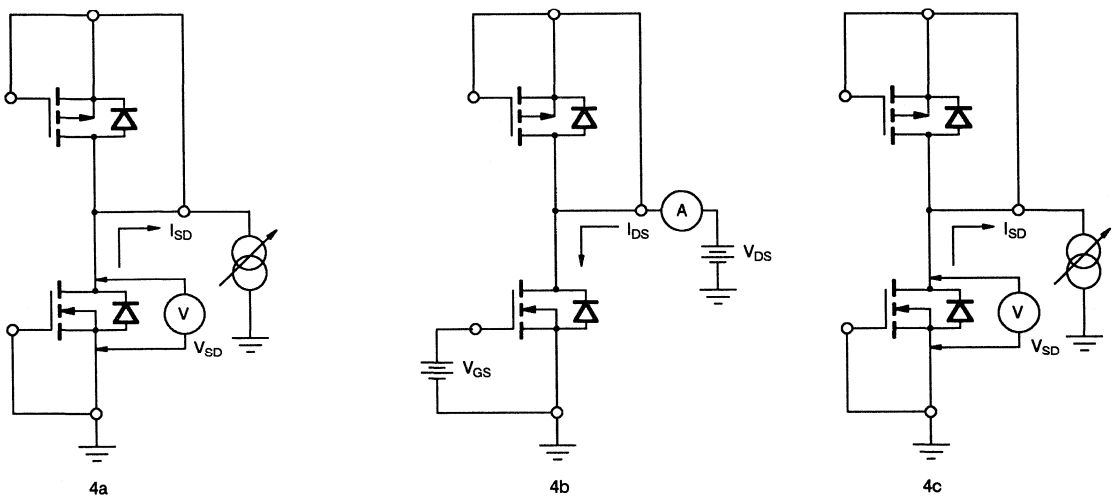


Figure 4. Thermal Impedance Test Sequence

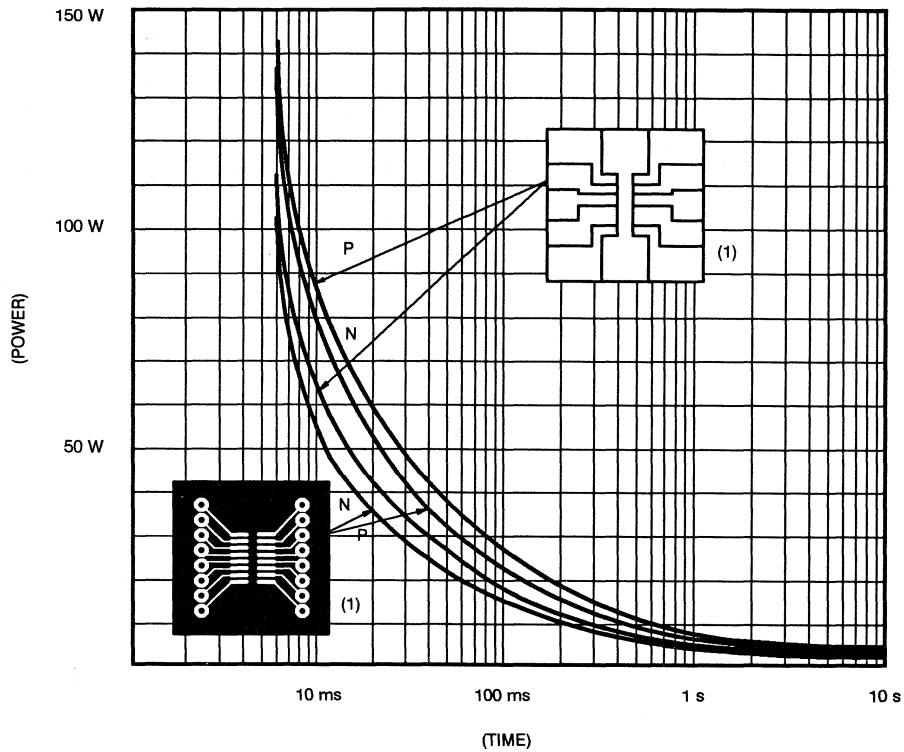


Figure 5. Single Pulse Power vs. P.C.B. Copper Area for Si9950DY/Si9954DY

NOTE: (1) P.C. board layouts approximately 1 x 1. "White" area indicates copper clad surface area, black indicates seperation between copper contacts and traces.

Pulsed Power Capability

The characteristics shown in Figures 5, 6, and 7 are presented as the power level that a room temperature device can absorb for a given amount of time without exceeding $T_{j(max)}$ = 150°C (the absolute maximum junction temperature rating). An approximation of the pulse duration or power level for a junction temperature increase from an elevated ambient to $T_{j(max)}$ can be obtained by multiplying the indicated power by the ratio $\Delta T/125°C$.

Conclusion

Dramatically increasing the amount of copper trace area electrically connected to or immediately adjacent to the substrate pins of the SO-packaged half-bridge devices ***does not*** contribute to steady-state thermal dissipation as greatly as one might expect. The SO-16 devices (Si9950DY and Si9954DY), for which the ten output pins are extensions of the lead-frame and thereby connected directly to the die, show a 30% to 50% increased power dissipation at 10 seconds. No differences could be resolved with power pulses greater than 1 second in duration on the SO-8 packaged devices (the Si9951DY, Si9955DY and Si9956DY). While steady-state power dissipation is limited for all of these devices, their peak power capabilities are considerable (approximately an order of magnitude increase for a 100 ms pulse, two orders of magnitude increase for a 1-ms pulse). And as Figures 5, 6 and 7 indicate, increased copper surface area ***does*** increase thermal dissipation for power pulses of less than about 100 ms duration in both the SO-8 and SO-16 devices.

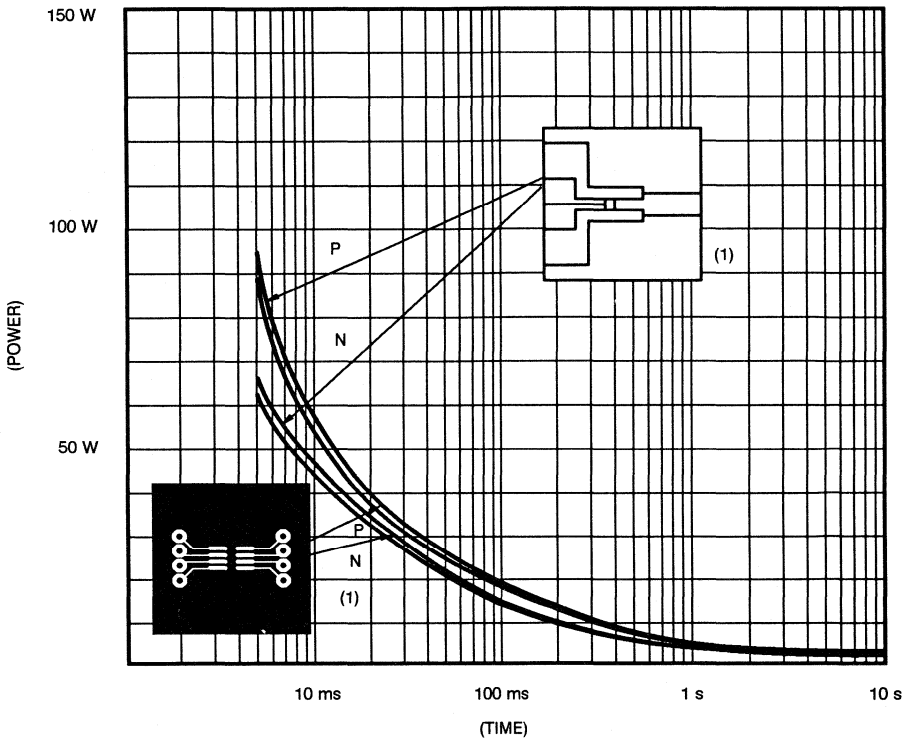


Figure 6. Single Pulse Power vs. P.C.B. Copper Area for Si9951DY

NOTE: (1) P.C. board layouts approximately 1 x 1. "White" area indicates copper clad surface area, black indicates seperation between copper contacts and traces.

A half-bridge configuration is most commonly used in switching applications to drive motors and similar (inductive) mechanical loads. With inductive loads, the most severe transient power peaks are associate with diode reverse-recovery losses, long switching transitions, and shoot-through current – not with (direct) load current. Although they result in severe power losses, these transients are of limited duration (usually microseconds). Peak load currents, on the other hand, are usually lesser in value but with longer durations, consistent with the load's mechanical time constant. The greater peak-current handling capabilities of the SO-packaged half-bridges are consistent with the 100 ms to 1 second peak load currents that result from high-performance (high mechanical bandwidth) motors, voice coils, solenoids, and linear actuators. Longer duration motor currents will have to be considered "steady-state" loads and thermal dissipation calculated accordingly.

In summary, this characterization leads to the following points for designing with the Si995X surface-mount half-bridge series.

1. Their considerable power switching capability is primarily a function of their extremely low on-impedance.

2. They not only exceed their rated steady-state power dissipation but are capable of considerably more for pulse durations consistent with those found in many applications.

3. In most applications, it is not necessary or beneficial to alter conventional PC board layout rules (established for other SO devices) by increasing the copper trace area. This obviously does not take into account any additional trace area necessary for the current conduction.

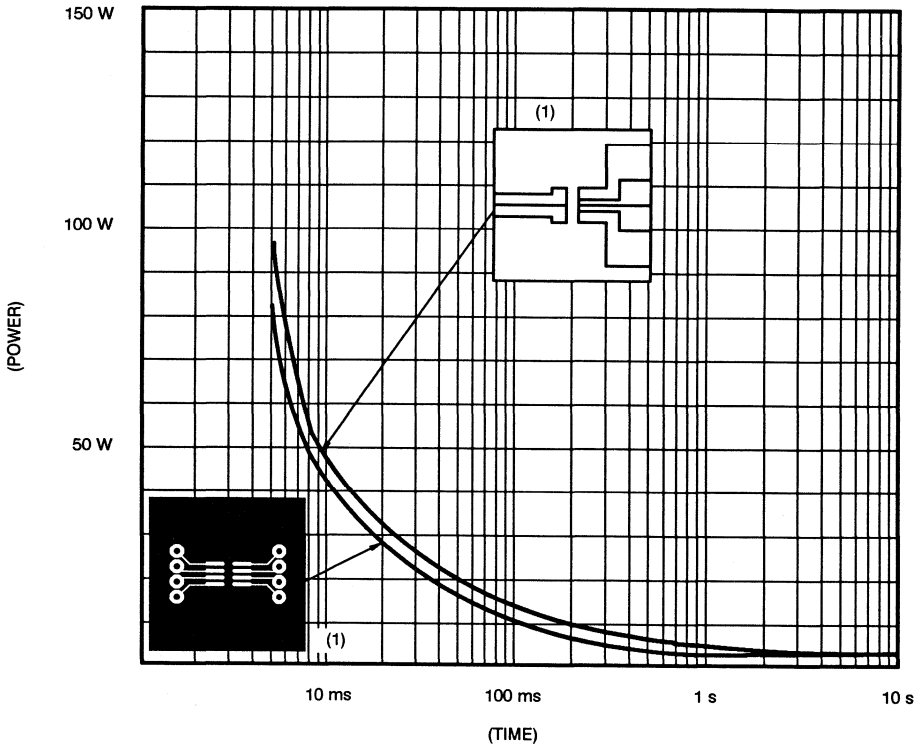


Figure 7. Single Pulse Power vs. P.C.B. Copper Area for Si9955DY/Si9956DY

NOTE: (1) P.C. board layouts approximately 1 x 1. "White" area indicates copper clad surface area, black indicates seperation between copper contacts and traces.

References

A. J. Chapman, Heat Transfer, Second Edition, Macmillan 1967.

R. H. Norris, et al., Heat Transfer Data Book, General Electric Corporate Research and Development, Schenectady, N.Y.

Fredric Wenthen, The Heat Sink Effect of Printed Conductors, IEEE Transactions on Parts, Hybrids and Packaging, Vol PHP-12, No. 2, June 1976

Low-Voltage Motor Drive Designs Using N-Channel Half-Bridges

Jim Harnden

Two basic MOSFET configurations are used in low-voltage motor drives – the n-channel half-bridge and the p- and n-channel (complementary) half-bridge. The main advantage of the complementary approach is the simplicity of its gate-drive circuitry, as discussed in Siliconix Application Note AN90-4. When an n-channel MOSFET is used for the high-side (or "upper") switch, the gate drive signal requires level shifting, resulting in increased complexity and cost.

But n-channel power MOSFETs are more efficient than p-channel MOSFETs in terms of $r_{DS(on)}$ vs. die area. This efficiency translates into lower cost, smaller die size for a given current and voltage, and the minimum $r_{DS(on)}$ that can fit in a given package. For both vertical and lateral transistors, n-material has better carrier mobility than p-material. Further exaggerating the disparity is the fact that most Power IC processes have been optimized for n-channel devices; thus, the processes yield even less area-efficient p-channel MOSFETs. For a given $r_{DS(on)}$ and breakdown voltage rating, a p-channel power MOSFET can easily be 2.5 to 4 times the area of a comparable n-channel device.

For applications where the n-channel half-bridge configuration is preferred, Siliconix has introduced the Si9955DY and Si9956DY. Each contains two electrically isolated, low $r_{DS(on)}$, n-channel MOSFETs in an 8-pin SOIC package. When the trade-offs have been carefully weighed and system efficiency dictates use of an n-channel bridge, several options remain in selecting the optimum isolated power supply and gate-drive level-shifting techniques for the application.

5-V Applications

In Figure 1, a charge-pump circuit is used to boost the 5-V supply (actually 4.5 V minimum) to a voltage sufficient to drive both the upper and lower MOSFET gates directly. Given the input level variations (4.5 to 5.5 V) and the charge pump's losses, the resulting supply voltage will range from approximately 12 to 16 V. This voltage range is safely within the ±20-V absolute maximum gate-source

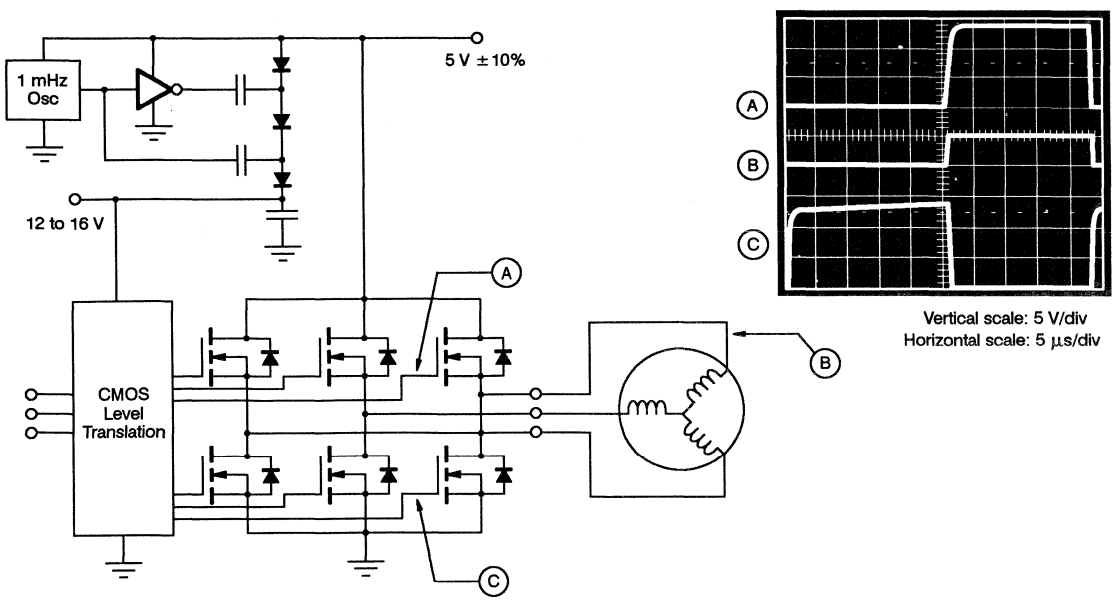


Figure 1. 5-Volt, 3-Phase Motor Drive

voltage rating for the lower n-channel device and provides at least 7.5 V of gate enhancement for the upper n-channel MOSFET. Driving all of the gates "rail-to-rail" results in a slightly lower impedance in the lower devices. In motor drives, however, the total impedance (one upper MOSFET plus one lower MOSFET) is usually more important than symmetry.

Directly driving both the upper and lower gates from a common voltage, as illustrated in Figure 1, not only eliminates the need for an intermediate voltage supply but also removes the need for isolation between the supplies used to drive the three upper n-channels.

12-V Applications

Intermediate low-voltage applications (around 12 V) can be simplified greatly if a dynamic gate-drive technique is acceptable. The bootstrap capacitor arrangement is a simple and inexpensive method of providing the necessary voltage to drive the high-side gates (Figure 2). Within a relatively narrow voltage range (about 10 to 20 V), a simple passive pull-up (R1) value can be selected to provide fast transition rates with tolerable switching losses. For operation above 20 V, it may be necessary to incorporate an active pull-up level-shift arrangement, and the gate-source of Q2 should be clamped with a Zener diode to guarantee that the absolute maximum V_{GS} rating is not violated. Operation below about 10 V could result in an insufficient Q2 gate-drive with this technique. The voltage stored in the bootstrap capacitor is the 10 V (supply voltage) minus a diode drop and minus the MOSFET voltage drop (load current x $r_{DS(on)}$ across Q1). This voltage is further reduced by the charge which must be transferred to fully enhance the gate of Q2, and the voltage decays over time by leakage current through D1 and Q3. In Figure 2 the inputs of the lower MOSFET (Q1) and the level-shift MOSFET (Q3) are tied together. A bootstrap arrangement does not completely eliminate use of a commutation or modulation sequence that turns both output devices off, and it is absolutely necessary that Q1 be turned on to recharge the bootstrap capacitor prior to turning on Q2. Q2 cannot be held on indefinitely, and the inherently "dynamic" nature of the bootstrap arrangement renders it unusable in some motor drive applications. But for many others it can provide a technically acceptable and highly cost-effective solution.

To understand the operation of the circuit shown in Figure 2, it is best to begin with the input high and both Q1 and Q3 turned on. Q3 pulls the gate of MOSFET Q2 to ground, turning it off, and Q1 (aside from driving the output low) provides a ground return for recharging the bootstrap capacitor to 12 V (minus the diode drop of D1 and the $V_{DS(on)}$ of Q1). When the input goes low, both Q1 and Q3 are turned off. This allows resistor R1 to pull Q2's gate high. Initially, Q2's gate charging current is drawn directly from the 12-V supply (via R1). When Q2's gate-source voltage exceeds its V_{th} (threshold voltage), it begins to turn on, pulling the half-bridge output (and the bottom end of the bootstrap capacitor) toward the upper rail. As the half-bridge output goes high, diode D1 is reverse biased, allowing the bootstrap capacitor voltage to level-shift above the 12-V supply. A bootstrap capacitor value approximately ten times greater than the effective capacitance of Q2 allows it to be fully enhanced without sacrificing more than 10% of the bootstrap's initial voltage charge.

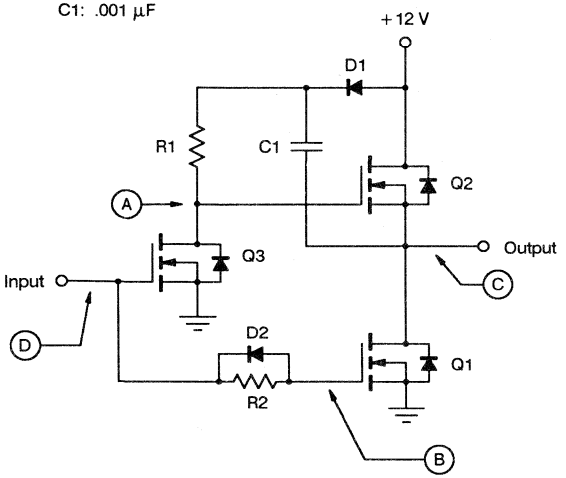
R2 has been added in series with Q1's gate to slow its turn-on rate, while D2 provides a lower gate-drive impedance to allow a rapid turn-off rate. Turning off both Q1 and Q2 quickly and turning them on at a reduced rate minimizes shoot-through current during transitions.

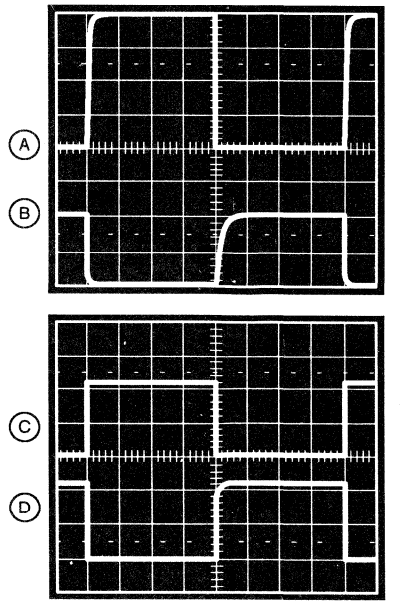
Although the leakage current through D1 and Q3 is extremely low, if Q2 is left on without some method of replenishing the lost charge, the bootstrap capacitor voltage will eventually collapse. As the bootstrap capacitor voltage depletes, the enhancement voltage of Q2 is reduced. This increases Q2's on-resistance and power dissipation to potentially damaging levels.

12- to 36-V Applications

A simple, minimum component charge-pump circuit can provide static operation and tolerable switching times for medium-voltage applications. The charge-pump circuit demonstrated in Figure 3 has been reduced to the smallest number of components and assumes a system 12-V supply can be used to drive the ground-referenced MOSFET gates and the oscillator. An oscillator frequency much higher than the desired switching frequency will charge the high-side MOSFET gate in minimal time with a small charge-pump capacitance (C1). In this example, to achieve a 20 kHz switching frequency with tolerable switching losses, a 2 MHz oscillator and a 0.001 µF charge-pump capacitor were chosen to obtain an output rise time of 500 ns.

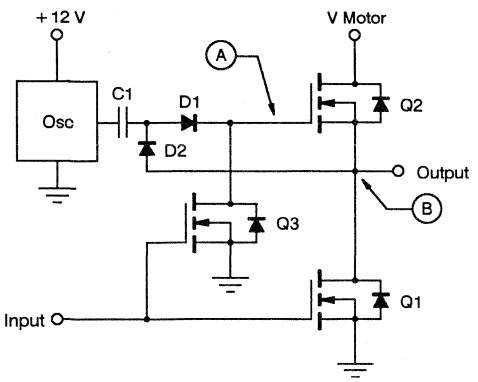
Q1, Q2: Si9955DY
Q3: 2N7000
D1, D2: IN4148
R1, R2: 200 Ω
C1: .001 µF

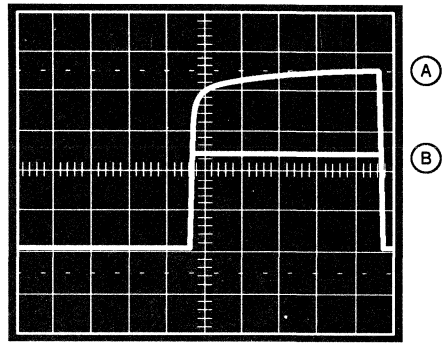




Vertical scale: 5 V/div
Horizontal scale: 5 µs/div

Figure 2. 12-Volt Motor Drive





Vertical scale: 5 V/div
Horizontal scale: 5 µs/div

D1, D2: IN4148
C1: 0.001 µF
Q1, Q2: Si9955DY or Si9956DY
Q3: 2N7002

Figure 3. 12 to 36-Volt Motor Drive

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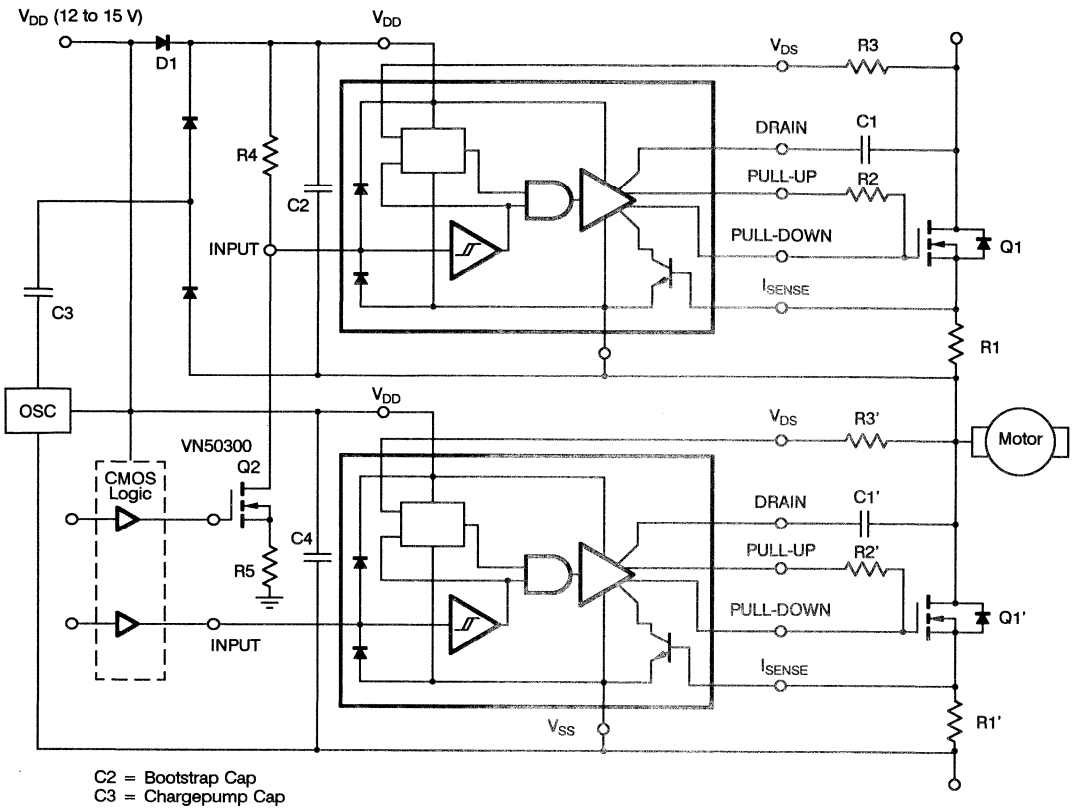


Figure 4. Si9910DY Adaptive MOSFET Gate Driver

Turning off a MOSFET with a charge-pump gate drive can also contribute significantly to switching losses unless some method is provided to "shunt" the gate charge. Traditionally this has been accomplished by providing a passive resistance between the MOSFET's gate and source. Thus the gate charge is drained off when the oscillator is disabled. The additional load on the charge-pump usually leads to a series of trade-offs concluding with marginal (at best) turn-on and turn-off rates. Aside from the usual switching losses, the turn-off time of the upper MOSFET is somewhat critical, as the turn-on signal to the lower MOSFET must be offset by a corresponding dead time to avoid simultaneous conduction (crossover current). At low voltages, a MOSFET such as the 2N7002 (Q3) can be used to simply "crow-bar" the upper MOSFET's gate charge to ground when the lower output MOSFET is turned on. The circuit in Figure 3 is intended for use at low voltages (less than the 50-V $V_{(BR)DSS}$ rating of the Si9955DY); thus, no current-limiting (for Q3) and no additional gate protection has been added to prevent the upper MOSFET's gate from being pulled more than 20 V below the source. Since the 2N7002 and the lower output MOSFET (of the Si9955DY) have compatible threshold voltages (V_{th}), and since their gates are tied together, the gate-source is inherently protected against overvoltage under all normal operating conditions, and crossover current is minimized. Increased efficiency could be achieved by disabling the oscillator when the half-bridge output is switched low.

Si9910DY Adaptive MOSFET Gate Driver

The Si9910DY adaptive MOSFET gate driver (Figure 4) provides a third method of driving dual n-channel half-bridges. Although designed to drive MOSFETs at much higher power levels, the Si9910 has proven to be an extremely cost-effective solution for low-power systems (compared to the discrete solutions).

Unique among integrated MOSFET gate drivers, the Si9910 provides low output impedance while drawing less than 1 μA of supply current when on (output high). This allows the driver to be referenced to the source of the high-side switch and powered by either a bootstrap capacitor, a charge-pump, or a combination of both. Combining the Si9910 with the high peak-current capability of the bootstrap capacitor allows rapid, highly efficient transition rates. The addition of a small charge-pump will overcome the on-state leakage losses, providing continuous (static) operation of the high-side output device. The Si9910 also provides a means for di/dt, dv/dt, and shoot-through current control as well as undervoltage and catastrophic current protection. Details of the Si9910's operation can be found in the *Siliconix Power Products Data Book* and in Application Note AN89-5.

The Si9910DY in the small-outline (SO-8) package provides assembly compatibility with the Si9955DY and Si9956DY n-channel half-bridges in SO-8 packages.

Summary

Although the n-channel power MOSFET half-bridge requires a somewhat more complex gate-drive arrangement for the high-side device, it offers $r_{DS(on)}$ advantages which extend the power range of surface-mount power devices. With the selection of a high-side gate-drive circuit that complements an application's needs, the n-channel half-bridge can provide a surface-mount compatible option that is economical and reliable.

When using n-channel half-bridges in motor drives, the commutation and modulation switching sequences and the operating-voltage range must be considered to select the optimum high-side gate-drive circuit. The problem to be solved is how to drive the gate of the upper n-channel MOSFET above the half-bridge supply voltage to fully enhance the device. The Si9955DY and Si9956DY exhibit good $r_{DS(on)}$ characteristics with only 4.5 V of gate enhancement, and the efficiency of these half-bridges in 5-V applications is further improved by the use of a circuit that increases gate-drive voltage for the lower MOSFET and provides sufficient voltage to enhance the upper device. As shown in Figure 1, the generation of a higher voltage to drive both the upper and lower gates does not necessitate circuits of undue expense or complexity.

With intermediate and higher voltage drives (above 5 V), sufficient voltage exists to fully enhance the power MOSFETs' gates, and the problem becomes that of level-shifting the gate drive to the high-side device without violating its absolute maximum gate-source voltage. Figures 2 and 3 show just two of the many solutions available which are based on the inexpensive bootstrap and/or charge-pump isolated supply techniques.

Both the bootstrap and charge pump have inherent characteristics which restrict their use to compatible drive sequences. Although a charge pump provides a method of direct, continuous, high-side gate drive, it usually results in slower transition rates. Bootstrap circuits provide a floating supply that allows considerable peak gate-charging current and thus, very rapid transition rates – but this occurs at the expense of static operation.

Combining the best of both the charge-pump and bootstrap circuits, the Si9910 offers an inexpensive, surface-mount solution with minimal parts count, providing both efficient transition rates and static operation. In addition, it offers control and protection measures that facilitate design of reliable, efficient motor drives.

Siliconix incorporated

Designing with Complementary Power MOSFET Half-Bridges in Standard-Outline (SO) Packaging

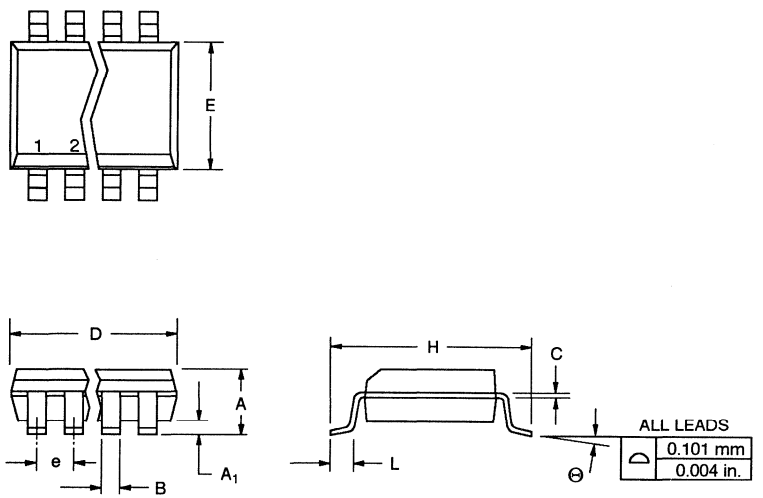
Jim Harnden

The Si9950DY, Si9951DY and Si9954DY are low-voltage, low on-resistance complementary p-channel and n-channel half-bridges that pack potent power handling into tiny surface-mount packages. Their standard-outline surface-mount packages (SO-16 and SO-8, see Figure 1) have copper lead-frames that maximize thermal transfer while maintaining complete compatability with existing surface-mount technology. Each of these devices can be used to drive inductive loads such as motors, solenoids, and relays directly, or they may be used as low-impedance buffers to drive larger power MOSFETs or other capacitive loads.

MOSPOWER devices offer measurable advantages in a variety of low-voltage motor drive applications. In a computer hard disk, key features such as track density, seek time, and power consumption are directly related to the efficiency of the spindle motor and the head actuator drive circuitry. Disk drives must squeeze maximum motor performance from low-voltage supplies (traditionally, well-regulated 12-V supplies) provided by the computer system. The advent of sophisticated full-function portable computers brings new performance expectations of battery driven systems (and 5-V operation).

For 12-V battery powered applications, designers must strive to limit voltage drops – which waste motor drive voltage, reduce battery life, and contribute heat that must be dissipated, often at considerable expense. The Si9950DY, Si9951DY, and Si9954DY complementary half-bridges substantially increase the motor size that can be driven from surface-mount power devices without additional heatsinking.

The complementary half-bridge can also be used in power conversion applications as a buffer stage to drive highly capacitive power MOSFET gates at the high frequencies used in modern designs. For example, by using an Si9950DY half-bridge to buffer the output of highly efficient CMOS PWM controllers, capacitive loads in excess of 3000 pF can be efficiently switched at rates greater than 1 MHz. This switching ability greatly extends the output power range of CMOS switchmode ICs.



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.53	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-16	9.60	10.20	0.378	0.402
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

Figure 1. SO-8 and SO-16 Package Dimensions

This application note describes the basic MOSFET parameters that are important when driving inductive and capacitive loads and shows characteristics of each of the three devices in this series of complementary half-bridges.

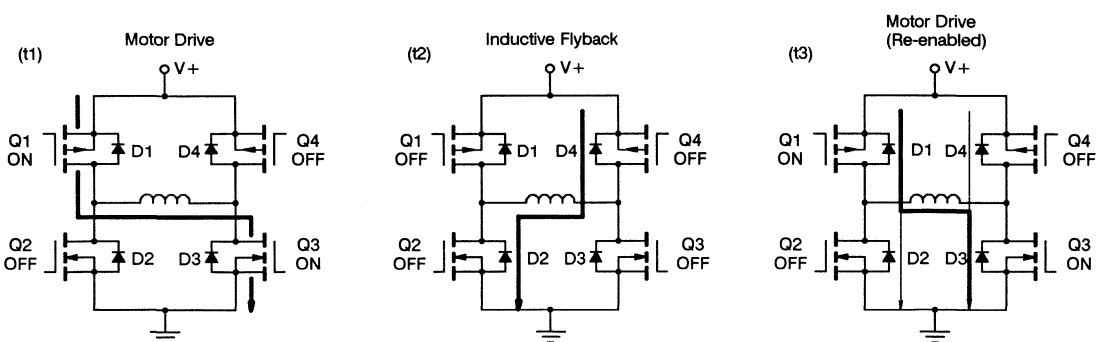
Driving Inductive Loads

When driving inductive loads with a power MOSFET half-bridge, several parameters that might otherwise be of secondary concern become very important. One characteristic of inductive loads is flyback energy. When inductor drive current is interrupted, damaging flyback voltages can result unless diodes are used to clamp the voltage and allow the inductive flyback current to freewheel. Each power MOSFET contains a fast-recovery intrinsic diode that can be used as a reliable and efficient clamp for inductive flyback energy. Of particular importance in the use of the MOSFET's reverse characteristics are its intrinsic diode specifications – such as, V_{SD} (reverse source-drain voltage, which is the diode forward voltage drop) and t_{rr} (reverse-recovery time).

The flyback current recirculating through the diode clamps is equal to the motor current, which reaches its maximum level during motor acceleration or braking. Although power lost in the clamp diodes (V_{SD} times the recirculation current) occupies a small percentage of the duty cycle, it can contribute significantly to overall MOSFET heating if the forward voltage drop is excessive. Both the n-channel and p-channel devices of each half-bridge are specified with a maximum forward voltage drop of 1.6 V at the MOSFETs' maximum (continuous) forward drain current rating.

The intrinsic diode t_{rr} becomes important any time the motor current is interrupted by turning off the MOSFET swtiches. When drive is re-enabled in the same path, while flyback current is still recirculating in the opposing clamp diodes, recombination will have to occur before the diode recovers and blocks voltage. This is demonstrated in Figure 2.

Figure 3 illustrates the relationship of the diode reverse-recovery characteristics with gate drive impedance. The load inductance is shown referenced to V+, and the upper MOSFET's gate is shorted to the source to isolate its intrinsic diode for demonstration purposes.



(t1) Q1 and Q3 ON for motor drive.

(t2) Power MOSFETs OFF, inductor flyback is conducted through current diodes D2 and D4.

(t3) If Q1 or Q3 are turned on before the flyback energy is fully dissipated, a current path will exist between the power supply and the ground during the diodes t_{rr}. The amount of shoot-through current that results depends on series impedance (how fast the opposing MOSPOWER device is turned on), stray series inductance, and diode reverse recovery time.

Figure 2. Clamping Inductive Flyback Energy

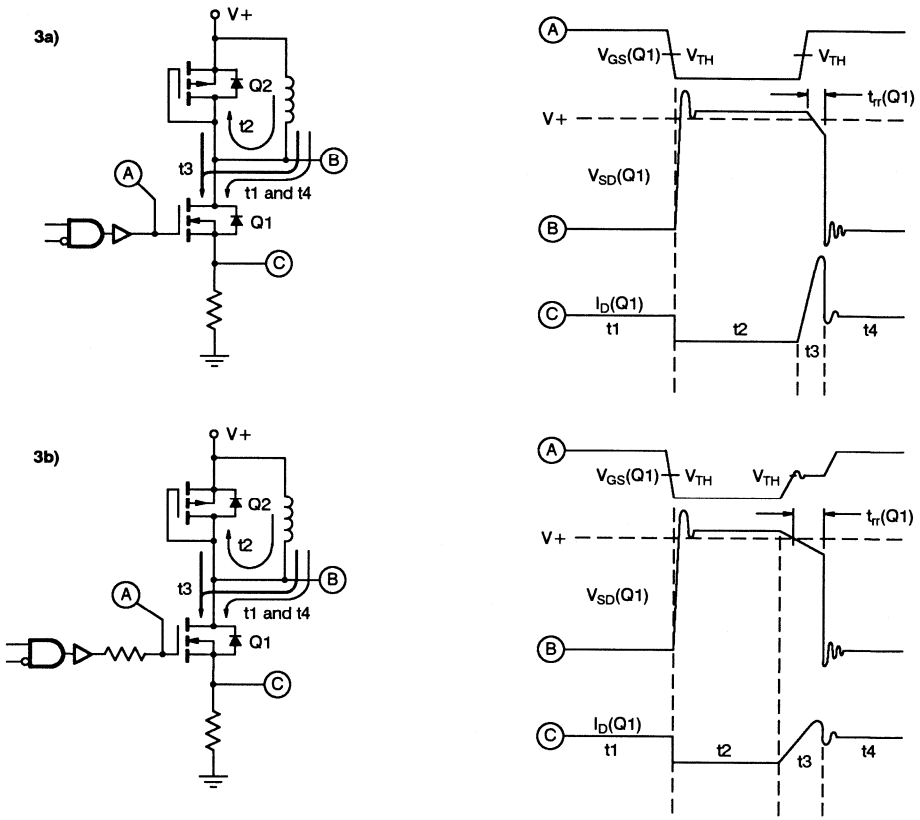


Figure 3. Shoot-Through Current and dv/dt vs. Gate Drive Impedance

During time t1, the lower MOSFET (Q1) is turned on and load current is conducted through the inductor to ground. At the leading edge of time t2, Q1 is turned off and flyback current from the inductor recirculates through the intrinsic diode in MOSFET Q2. Shoot-through current occurs during time t3, when Q1 is switched back on. As Q1 is turned back on, it conducts current from both the load and reverse current through the diode of Q2, which has yet to recover. When enough current is conducted to reverse the voltage potential across the diode of Q2, it begins to recover. Duration of the current spike is dependent on the power MOSFET t_{rr} (a function of the diode's forward current and forced recovery di/dt). The current spike magnitude depends on the product of the gate voltage and the g_{fs} of Q1 at the time of Q2's diode recovery (Figure 3a).

As the value of gate drive resistance (R1) is increased, the turn-on rate of Q1 (during time t3) is reduced (Figure 3b). By reducing the rate of gate drive voltage rise ($d\text{-}_{GS}/dt$), the level of gate voltage present when the diode recovers is reduced, thereby reducing the peak shoot-through current level. As gate drive impedance R1 is increased, the forced recovery current rate (di/dt) is also reduced, which actually increases t_{rr} in MOSFET Q2's diode. (The total amount of charge which must recombine remains the same regardless of di/dt, and since the maximum current level is now restricted, time is increased.) Efficiency is not increased by reducing peak shoot-through current; however, potentially damaging levels of peak current will be avoided, and EMI/RFI will be reduced.

Determining the proper gate drive impedance to achieve the desired reverse-recovery characteristics and system EMI/RFI requirements must be balanced against the maximum transition times required to achieve acceptable switching losses. As a basis for understanding the impact of switching time and the resulting switching losses on overall system efficiency, we must assume some typical operating conditions. If the modulation frequency is 20 kHz, one cycle will be 50 µs. If the transition time objectives are arbitrarily set at 1% of the overall duty cycle duration (500 ns total), each transition (including worst-case t_{rr}) must be less than 250 ns. The oscilloscope photograph, Figure 4a, demonstrates that this is a reasonable goal. These transition waveforms result when the configuration shown in Figure 4 is driven directly by a CMOS logic gate. The oscilloscope photograph in Figure 4b illustrates the output current and voltage waveforms with a 500-Ω series gate resistor (R1). In both examples, Figures 4a and 4b, a CD4000 series CMOS logic device was used to drive the power MOSFET gate.

Aside from the obvious reasons for limiting di/dt during t_{rr}, extreme rates of dv_{DS}/dt can result at the end of time t3 (Figures 3a and 3b). This recovery dv_{DS}/dt (commutating dv/dt) is primarily a function of the di/dt and peak shoot-through current forced during the diode recovery time. All power MOSFETs have some sensitivity to commutating dv/dt; Figure 5 indicates what characterization data has shown to be "safe" dv/dt rates as a function of forward diode current prior to a forced recovery. This applies only if the forced voltage across the device (V+ or $V_{Battery}$) is above 85% of the $V_{(BR)DSS}$. For modern DMOS geometries, commutating dv/dt sensitivity decreases drastically and ceases to have any effect below approximately 60% of the $V_{(BR)DSS}$ rating.

Common Gate Drive

A common cause of simultaneous conduction results from connecting the p-channel and n-channel gates together and driving them from a common logic signal. While this may be a completely acceptable gate drive method for capacitive loads or for lower voltage systems, it will probably result in excessive crossover current when driving inductive loads with 12 V across the bridge. If the gates are driven in common, the correct output states will result; however, this occurs at the expense of a current spike caused by both devices being partially turned on as the common gate voltage is in transition between approximately 2 V (n-channel threshold voltage) and 8 V (12 V minus p-channel threshold voltage).

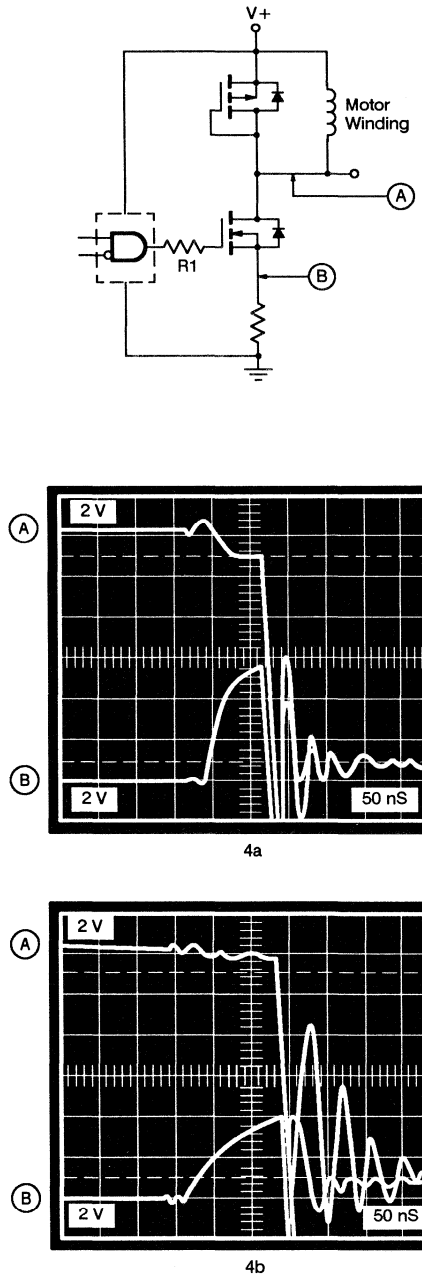


Figure 4. CMOS Gate Drive and Resulting Output Waveforms

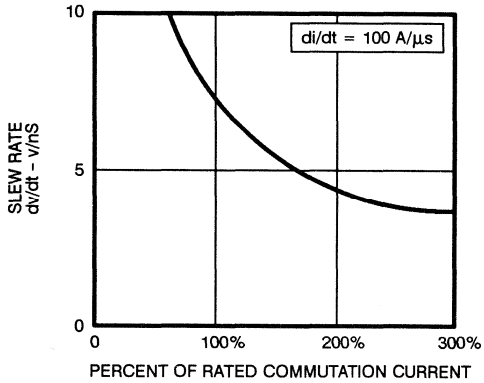


Figure 5. Reverse-Recovery dv_{DS}/dt Sensitivity

Figure 6 demonstrates the crossover current that can exist in the Si9950DY at V+ = +12 V with the gates driven by a ramp voltage. In this example, the crossover current reached a peak of 3 A, limited only by the g_{fs} of each device (with limited enhancement voltage above the threshold voltage) and by the series resistance.

In Figure 7, a pre-driver stage has been added that virtually eliminates crossover current under these same conditions. The impedance of the p-channel and n-channel buffer stage governs the turn-off times of the output devices. And R1, plus the buffer MOSFET's on-resistance, sets the turn-on times.

As will be discussed under "driving capacitive loads," it may be perfectly acceptable to tie the gates together when driving capacitive loads.

Disk Drive Applications

Using half-bridges with p-channel and n-channel devices allows the simplest gate drive circuitry to be used, since both gates can be pulled to ground or to the 12-V supply. The half-bridge used to drive each phase of the spindle motor (Figure 8) or head actuator (Figure 9) is typically driven directly by the output of a standard CMOS logic device powered from the same 12-V supply. While the relatively high output impedance of a CMOS logic device will not drive the capacitive gates of the half-bridge hard enough to attain maximum switching speeds, the combination will provide sufficiently fast transition rates to result in tolerable switching losses. Driving the power MOSFET gates with lower impedance drivers will result in faster transition rates and further reduce switching losses; however, the designer is usually forced to strike a balance between switching losses and increased EMI/RFI. This is of particular concern in rotating disk drive memories.

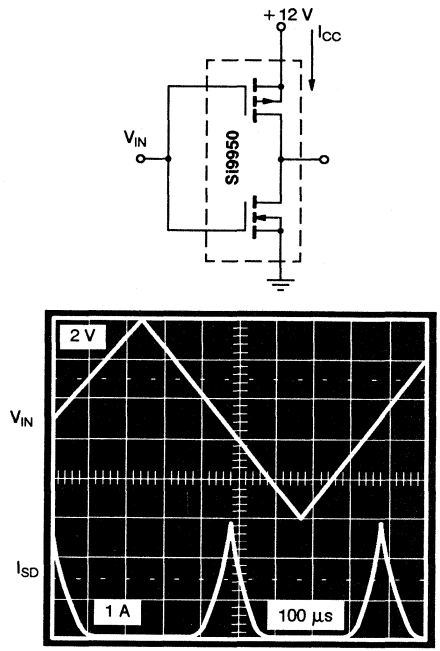


Figure 6. Crossover Current Caused by Common Gate Drive

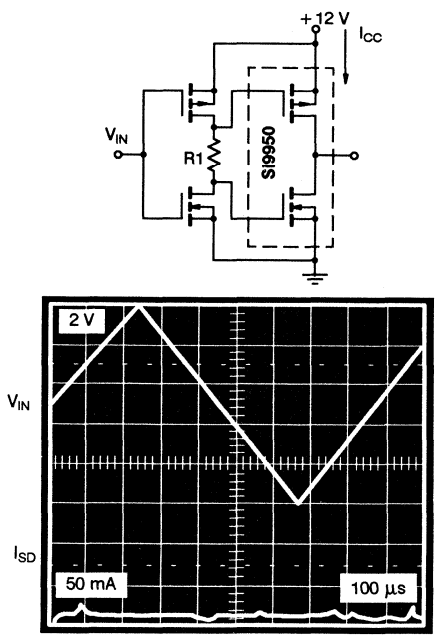


Figure 7. Complementary Buffer Stage with Shoot-Through Current Limiting

The 12-V supply provided to the peripheral function by the host computer system is usually clean and regulated to ± 10%. One of the designer's greatest tasks is to achieve the desired motor drive performance without destroying the supply's integrity. This is accomplished by managing a number of trade-offs, such as the balance previously noted between transition rates and EMI. Another prime concern is any shoot-through current caused by the simultaneous conduction of both devices in one half-bridge. One common cause of this condition is the reverse conduction of current through the body-drain diode during the diode t_{rr}, as previously discussed.

Driving Capacitive Loads

Highly efficient CMOS devices are a natural complement to the low-loss power handling capabilities of power MOSFETs. However, CMOS outputs are relatively high impedance and power MOSFET gates are highly capacitive. If high frequencies are necessary, some type of gate drive buffer must be used. Any of the surface-mount half-bridges will function perfectly in this application as a very low-impedance, complementary output stage for the CMOS device. The gate capacitances are easily driven by standard CMOS outputs, and the single-stage, complementary pair adds minimal delay.

The high-efficiency CMOS current-mode regulator illustrated in Figure 10 demonstrates a combination that takes advantage of the characteristics of each device. The Siliconix Si9100 series of current-mode controller ICs, built with CMOS/DMOS (power IC) technology, includes regulators and controllers. The regulators feature an on-board output power device, and the controllers have a CMOS output designed to drive an external power MOSFET with higher current or voltage capability. This CMOS output is capable of driving power MOSFETs up to 1000 pF (C_{iss}) at the 500-kHz maximum switching frequency. By using the controller with a CMOS output and inverted logic, a lower impedance gate-drive stage (the Si9950DY) can be added to increase the discrete power MOSFET output device size to over 5000 pF (C_{iss}). This extends the power range of the controller series to kilowatt levels.

In the oscilloscope photograph in Figure 10, voltage waveforms demonstrate the rise and fall times attained at the common gates of the Si9950DY (Trace A) and the gate of the SMM20N50 output device used in this example (Trace B). Symmetrical rise and fall times of less than 10 ns are sufficient to provide minimal transition losses, even at 500 kHz.

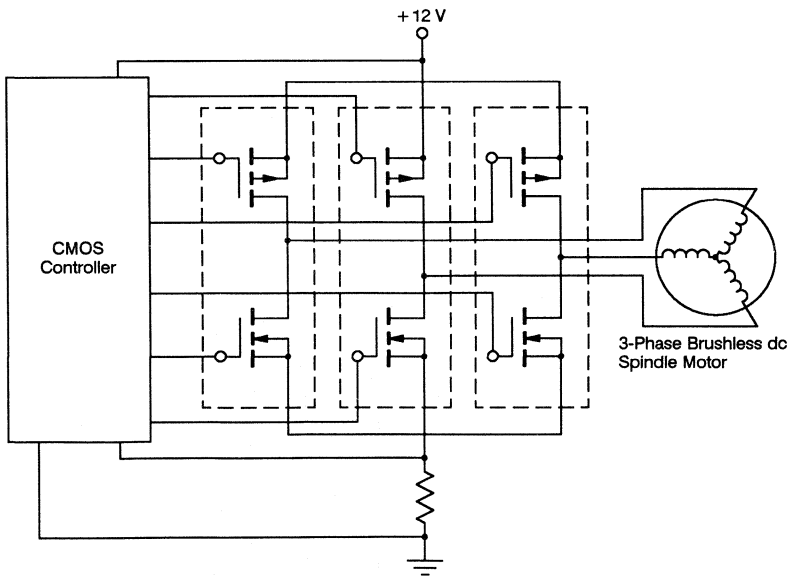


Figure 8. 12-V, 3-Phase Permanent Magnet Brushless Motor Drive

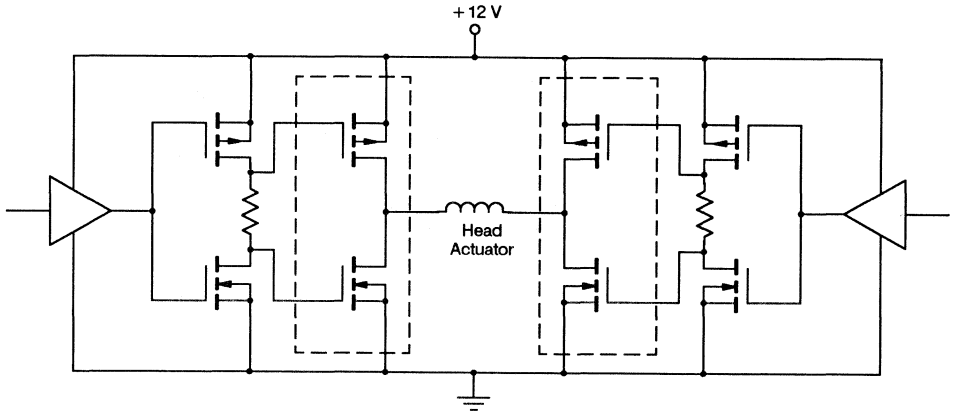
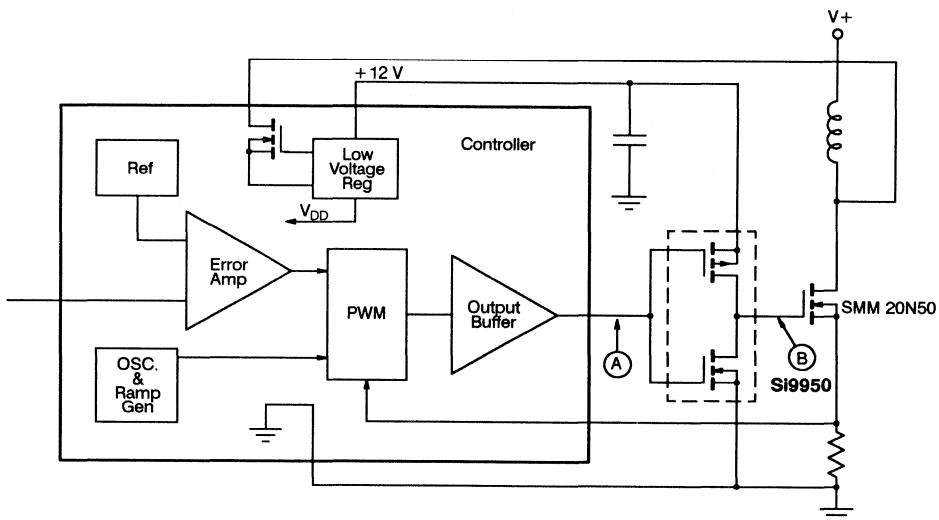


Figure 9. 12-V H-Bridge Actuator Drive



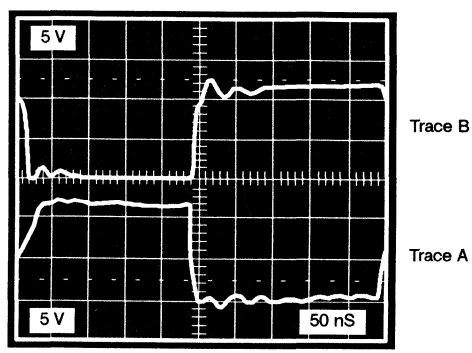


Figure 10. Very Low-Impedance Power MOSFET Gate Driver

With a capacitive load (Figure 11), the gates of the p-channel and n-channel complementary stage devices can usually be tied together and driven in common without the penalty of cross-conduction current that could be present with an inductive load. As discussed in the "driving inductive loads" section, with 12 V across the complementary stage, both devices will be partially on at the gates' transition between about 2 and 8 V. But with the capacitive load representing an essentially vertical load line during the first few nanoseconds of the transition, dv_{GS}/dt usually exceeds dv_{DS}/dt, and what would have been cross-conduction current goes into charging the load.

Summary

The Si995X series provides three complementary power MOSFET half-bridges in small-outline packaging (SO-16 for Si9950DY and Si9954DY and SO-8 for Si9951DY). The complementary p-channel and n-channel half-bridge architecture, combined with the high-impedance gate characteristics of power MOSFETs, make the devices extremely easy and efficient to drive. The rugged MOSPOWER half-bridges are designed to provide reliable, optimized performance for inductive loads such as motors, alternators, and solenoids. The power MOSFETs' intrinsic diodes are designed and specified to function reliably and efficiently as clamp diodes when driving inductive loads.

The Si9950DY, Si9951DY, and Si9954DY can also serve as very low-impedance output buffer stages to extend the range of capacitive loads driven by CMOS circuitry. The p-channel and n-channel half-bridge configuration allows the two gates to be tied together and driven directly by a common CMOS output in low-voltage applications. The single complementary stage offers minimum propagation delay and very low-impedance output, which greatly extends the output power range of high-frequency CMOS controllers.

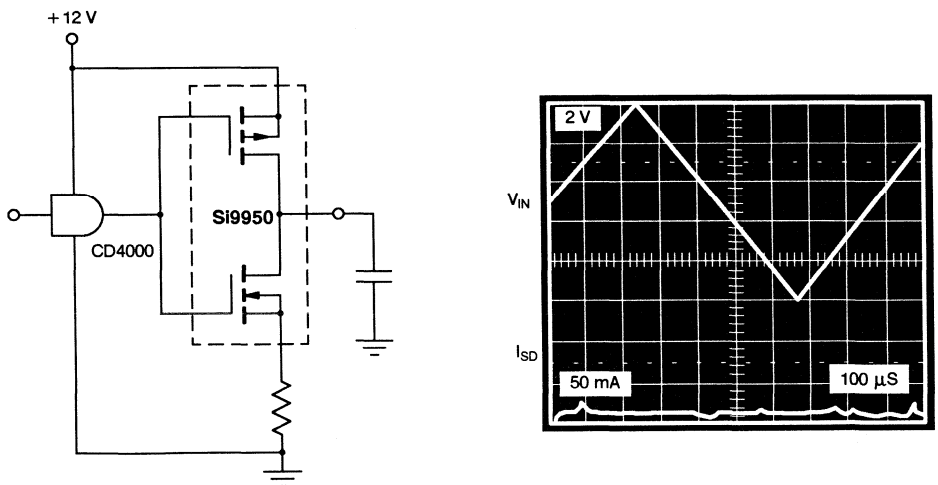


Figure 11. Common Gate Drive with Capacitive Loads

Siliconix incorporated

Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC

Craig Varga

Getting high efficiency from low-power off-line power supplies has always posed difficulties for the design engineer. Power hungry control circuits require either line frequency transformers for bias or bleeder circuits for start-up. The problem with the bleeder approach is that, to date, no provisions have been made in PWM ICs to turn off the bleeder; so several watts of power get consumed during normal operation – serving no purpose but to heat the bleed resistor. While solutions are available, they all require additional parts, which increase costs and use precious circuit board real estate.

The Si9120 from Siliconix was designed to address these problems. This current-mode control, pulse-width modulator IC is implemented with combined BiC/DMOS technology. All logic functions are implemented in CMOS to reduce the typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. Included on chip is a 450-V DMOS, depletion-mode transistor configured as a linear voltage regulator to supply operating power to the chip directly from the rectified 115-V mains. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency. Other features include a temperature-compensated buried Zener reference for less than 0.2 mV/°C drift; a latchable shutdown feature; and a dual current-limit comparator, which minimizes false tripping due to leading-edge current spikes. A major advantage of CMOS processing is speed – current-limit delays are typically under 100 ns while supply current is kept at less than 1 mA. This allows reliable operation up to 500 kHz.

FUNCTIONAL DESCRIPTION

Pre-regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (450-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{CC} to turn the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

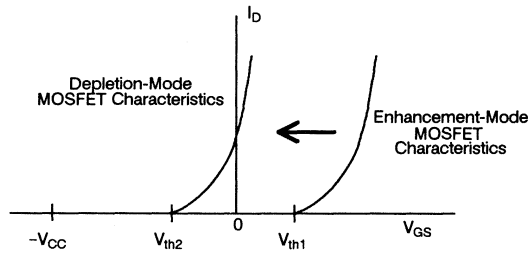


Figure 1. Depletion-mode MOSFET Characteristics

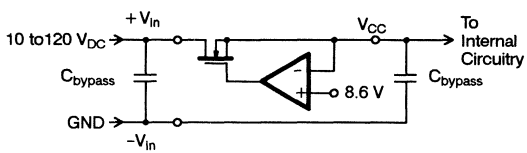


Figure 2. Pre-regulator/Start-up Circuit

For some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 7 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{in}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off.

Oscillator

A ring of inverters and internal MOS capacitors form the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$ (the CMOS logic threshold), inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter. It also causes the "bump" at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

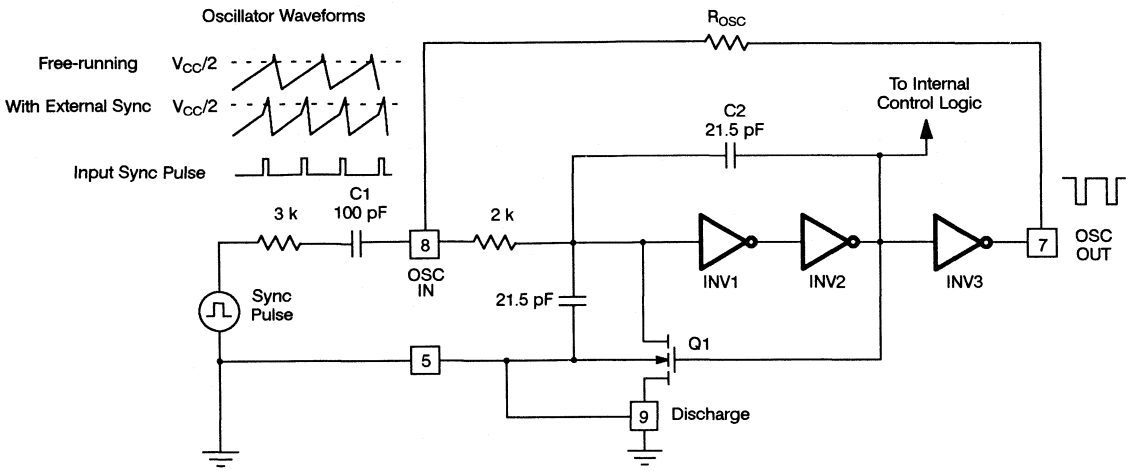


Figure 3. Si9120 Oscillator Circuit Operation

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_s.

Error Amplifier

The bias resistor, connected from pin 16 (bias) to pin 6 ($-V_{in}$), programs the current sources in the analog portion of the current-mode controller – including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9120 data sheet guarantees the performance of these functions at one value of bias current – 15 µA. It is possible to change the performance characteristics of these functions by changing the bias current. (See Siliconix Application Note AN88-3 for an explanation of how this is accomplished.)

The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2 MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

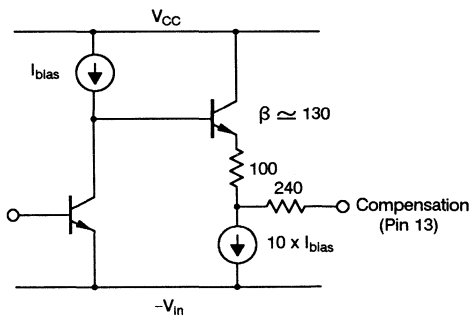


Figure 4. Error Amplifier Output Stage

The error amplifier is unity gain stable with a typical bandwidth of 1.4 MHz and 70° phase margin. Bias current values from 5 µA to 50 µA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{bias} is increased above 15 µA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

Voltage Reference

A buried Zener with merged temperature compensating diode (Patent no. 4766469) is used to achieve stability of 0.2 mV/°C.

The Si9120 voltage reference is trimmed to 4 V plus or minus 2% with a bias current of 15 μA. Note that trimming is done with the error amplifier connected for unity gain, so the effect of the offset voltage is removed. The reference voltage varies by about 1% as I_{bias} is varied from 5 to 50 μA. If 2% reference accuracy must be guaranteed, I_{bias} should be set at 15 μA.

Comparators

The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching. The total current-limit delay to output versus I_{bias} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{bias} = 5 μA, but decreases to 50 ns for I_{bias} = 30 μA. As operating frequency is increased, I_{bias} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{bias} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{bias}. The current sense resistor and I_{bias} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.

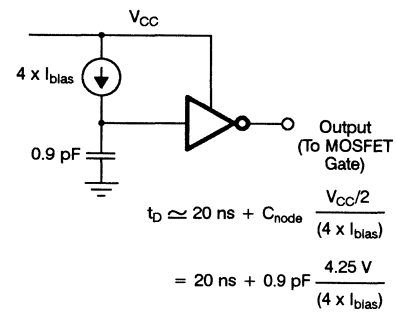


Figure 5. Current-limit Comparator Delay (Equivalent Circuit Model)

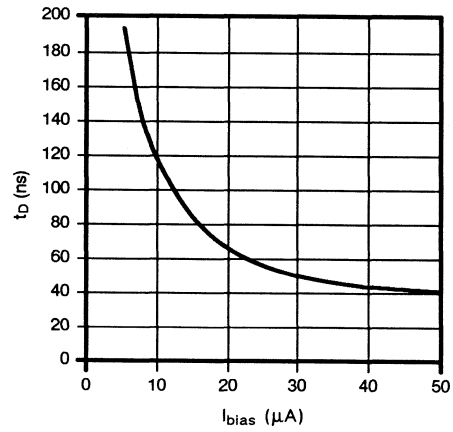
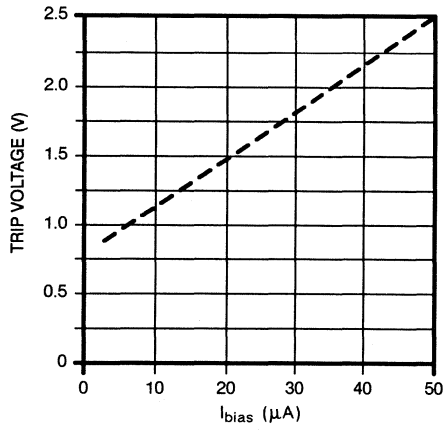


Figure 6. Current-limit Comparator Delay vs. Bias Current



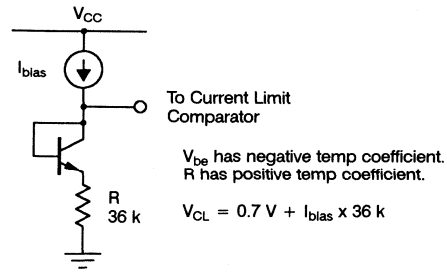


Figure 7. Current-Limit Trip Voltage vs. Programmed Bias Current

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(on)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC}$$

where

Q_g = MOSFET gate charge
f_s = switching frequency
V_{CC} = supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the SHUTDOWN and RESET inputs have internal current-source pull-ups (equal to I_{bias}), so they can be left open when unused. As long as the SHUTDOWN input is held low, the output is OFF. If the RESET input is hard wired to $-V_{in}$ (through a normally closed reset button if desired), any LOW input to SHUTDOWN will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

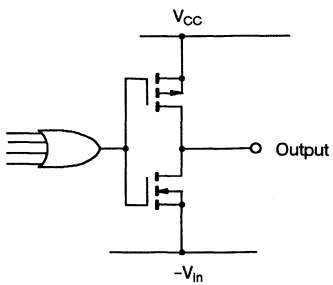
Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 15 to 20 mA. The output is disabled until V_{CC} reaches the undervoltage (UV) lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive. When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by $Q_g \times f_s$, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.6 V).

If too much current is drawn from V_{CC} (for instance, to supply other circuitry), it is possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle. Consult the factory if a minimum pre-regulator current specification above 5 mA must be guaranteed.

FLYBACK CONVERTER EXAMPLE

To illustrate the design procedure for a low-power off-line SMPS, a typical example shold be presented. But what is a "typical" 5 to 10 W supply requirment? Should the output be a single +5 V or +12 V, or should a dual output, ±5 V or ±12 V, be used? How about +5 V and ±12 V? There is no typical requirement, so a multiple-output design was chosen since cross regulation requirements



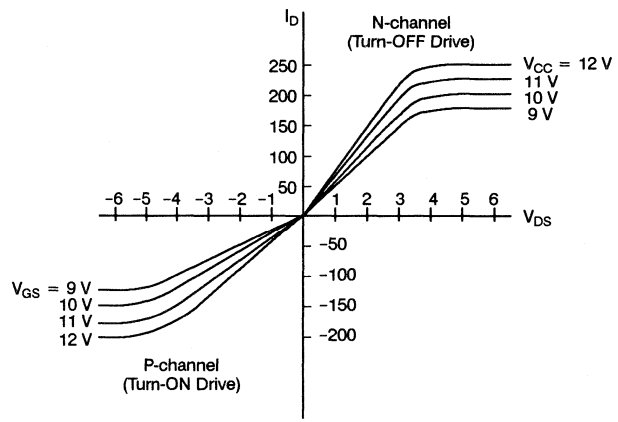


Figure 8. Output Drive Characteristics

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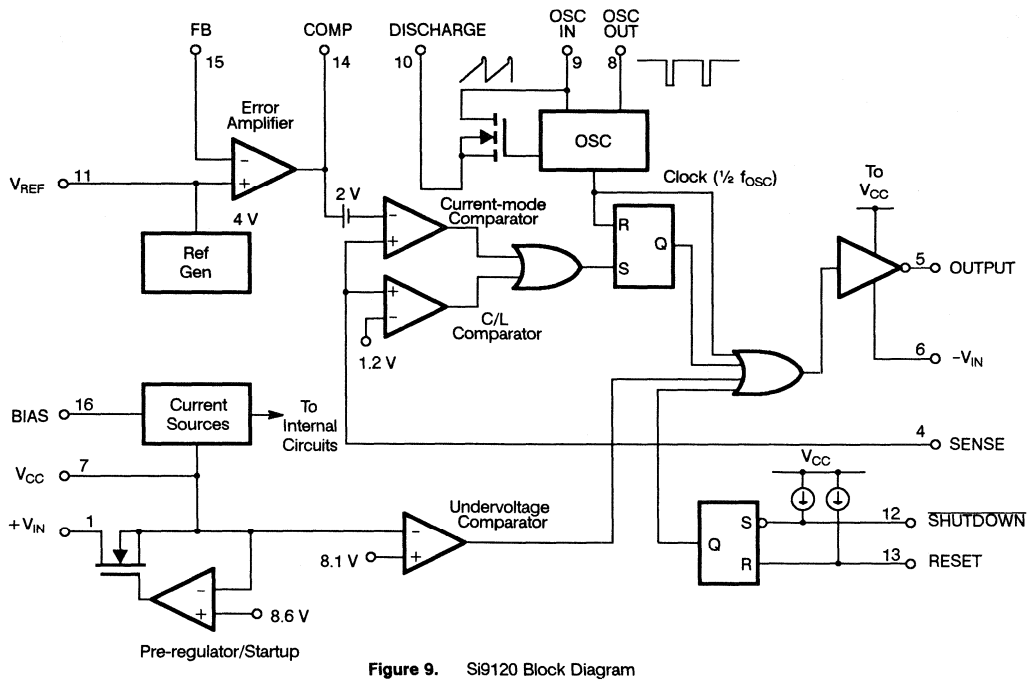


Figure 9. Si9120 Block Diagram

make this the more difficult problem. The specifications for a 5-W supply with four outputs is given below.

Specifications

Input Voltage 90 to 130 V ac, 50 to 60 Hz

Output Voltage (V)	Min. Load (mA)	Max. Load (mA)	Regulation (%)	Ripple (mV p-p)
+30	1	4	±5	200
+12	80	340	±5	200
$+5_{(Main)}$	25	110	±5	50
$+5_{(Aux)}$	20	80	±5	15

Efficiency >80% Minimum
Switching Frequency 32 kHz

Circuit Description

The flyback converter circuit, shown in Figure 10, was designed for minimum cost and parts count. Since the regulation requirements are fairly loose, it is advantageous to eliminate feedback from primary to secondary. Output voltage is controlled indirectly by regulating a bootstrap auxilliary winding on the primary side. (Strictly speaking, the auxillary winding is not required, as the chip will run directly from line power; but another feedback scheme would obviously be necessary.) All outputs are isolated from one another. Also, the primary-to-secondary isolation is designed to meet VDE safety requirements.

The power switching transistor (Q1) is an IRF820 rated at 500 V and 2.5 A. On-resistance is specified at 3 Ω. While this device may appear to be overkill for a 5 W output, it is the smallest 500 V die available, and it allows operation without a heatsink.

The flyback inductor (T1) is designed to operate in the discontinuous conduction mode. This makes loop compensation simple since there is no right half plane zero in DCM flyback converters. Also, since the power level is so low, the higher peak currents associated with this mode of operation pose no significant problems. The Si9120 provides all necessary control functions with only a handful of passive components.

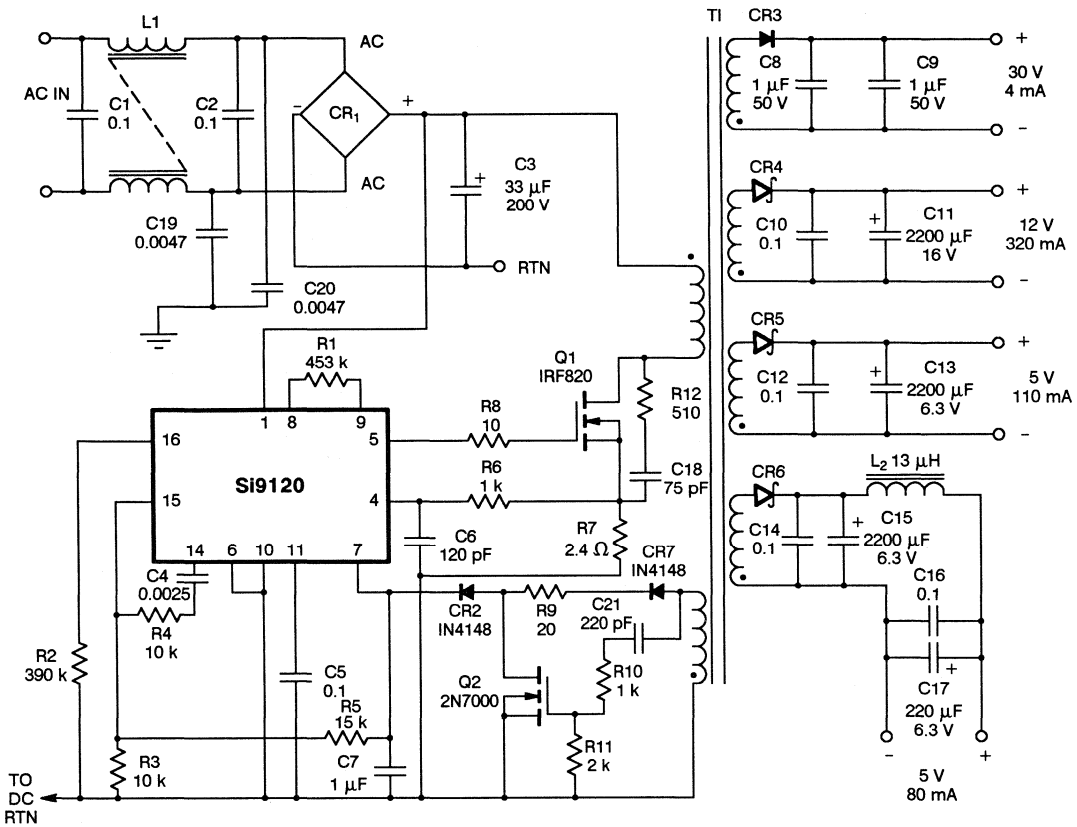


Figure 10. 5-W Offline Flyback Converter

FLYBACK FUNDAMENTALS

The flyback circuit works by storing energy in the flyback inductor during the switch's on-time and releasing this energy to the secondary circuits during the switch's off-period. The power transformer, in the case of a flyback converter, is not a transformer at all. Transformers work by coupling energy from primary to secondary, storing as little energy as possible. The flyback, however, stores all the energy for one cycle of operation in what is properly an inductor.

It is widely believed that current in an inductor cannot be changed instantaneously. This is not quite true. Ampere-turns are what cannot change instantaneously. If you could somehow change the turns, you could change the current on demand. This is what happens in the flyback inductor. During the switch-on time, some number of ampere-turns are developed in the primary winding. The power switch is then turned off in essentially zero time, forcing the ampere-turns to appear at the secondary windings. Thus, turns have changed, and amperes scale accordingly. Autotransformer action between the various windings forces the output voltages to track in proportion to the turn ratios of the windings. This forces the output capacitors to peak charge to the respective winding voltages and, thereby, provides regulation between windings. The better the coupling between windings, the better the cross regulation.[1] Hence, all four outputs are wound closely together with no additional insulation between windings. By controlling the peak current through the primary winding during the on-time, the total energy per cycle, hence the total throughput power, can be controlled. By making this current a function of the output voltage error, voltage regulation is achieved.

On initial application of power to the supply, the high-voltage DMOS transistor in the Si9120 begins to charge the V_{CC} supply capacitor, C7. When approximately 8.1 V appears on the bias supply, the Si9120 undervoltage lockout enables the output driver. All internal bias voltages are stable at this point, and clean operation is assured. When V_{CC} reaches 8.6 V, the DMOS linear regulator reduces the charging current to maintain this voltage. Within a few cycles of operation, the bootstrap winding raises V_{CC} beyond the point at which the linear regulator tries to hold the bias supply. The DMOS transistor is forced to cut off. Now the V_{CC} supply is totally independent of the power line and draws no current from it.

A cycle is initiated by the Si9120 clock toggling the output driver on. The driver turns on power switch Q1, causing current to begin ramping up linearly in T1's primary winding. The current is sensed by R7 and filtered by R6 and C6. When the Si9120's current-sense comparator detects that the primary current has reached the control loop's programmed level, the power switch is shut off and energy stored in T1 begins to discharge into the secondary circuits.

To close the regulator loop, the voltage of the V_{CC} supply winding on the primary side is sensed and compared to a reference. The difference is multiplied by a high-gain amplifier. These functions are all performed by the Si9120. R3 and R5 divide the bias voltage down to the 4 V reference level. R4 and C4 provide for loop compensation, and C7 filters V_{CC}.

A major problem exists in any converter with a large input-to-output isolation voltage -- leakage inductance of the flyback inductor. A portion of the energy stored in this inductance will appear as a voltage spike on the feedback winding. The V_{CC} supply tends to charge to the peak of the spike, forcing the control loop to regulate all of the output voltages substantially below the desired values.

Spike suppression and proper operation of the regulator loop are provided by a blanking circuit (consisting of R9, R10, R11, C21, CR7, and Q2). At the instant Q1 turns off, a positive-going voltage appears at the anode of CR7. C21 forms a differentiator with R10 and R11 that produces a positive voltage on the gate of Q2. This turns on Q2 and clamps the anode of CR2 to ground, back-biasing CR2 and preventing the spike from passing through to the V_{CC} supply. A substantial portion of the energy contained in the voltage spike is shunted to ground through CR7 and R9 (the circuit is behaving, to some degree, like an active snubber). When the spike energy has been dissipated, the voltage drops to the nominal level. R11 then pulls Q2's gate voltage back down, turning off Q2 and allowing the remainder of the pulse to pass through to the V_{CC} supply. Figure 11 shows details of the blanking circuit in operation.

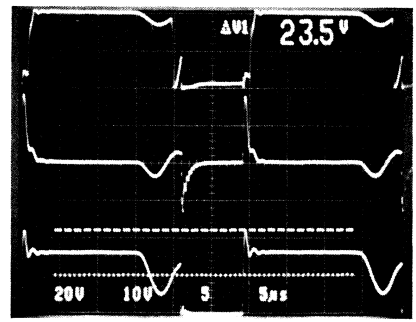


Figure 11. Top Trace - Anode of CR2
Center Trace - Gate of Q2
Bottom Trace - Anode of CR7
Note spike amplitude of 23.5 V.

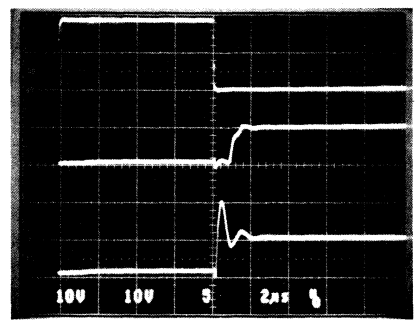


Figure 12. Top Trace - Gate Drive Q1
Center Trace - Anode of CR2
Bottom Trace - Cathode of CR7

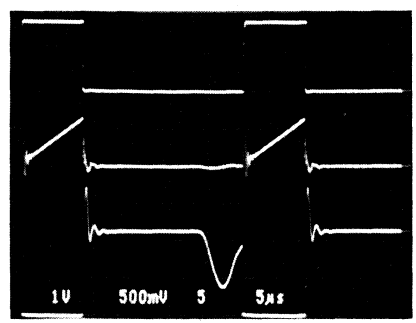


Figure 13. Top Trace - Gate Drive Q1
Center Trace - Voltage Across R7
Bottom Trace - Drain Voltage of Q1 (100 V/div)

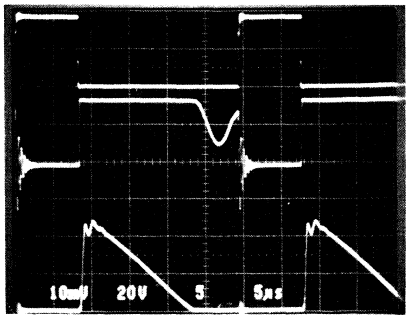


Figure 14. Top Trace - Gate Drive Q1
Center Trace - Anode of CR4
Bottom Trace - CR4 Current (500 mA/div)

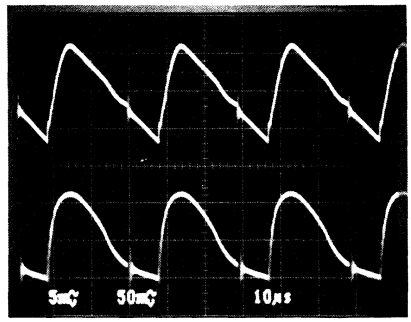


Figure 15. Top Trace - 30-V Output Ripple
Bottom Trace - 5-V, 80-mA Ripple

Actual measured outputs tabulated at various line and load conditions ($5_{(Main)}$ = 5 V, 110 mA, $5_{(Aux)}$ = 5 V, 80 mA):

Table I: 5-W Off-Line Flyback Test Data

Full Load Outputs (V)				
AC Input (V RMS)	**12 V**	**30 V**	**$5_{(Main)}$ V**	**$5_{(Aux)}$ V**
80	11.00	28.50	5.019	5.058
100	11.05	28.60	5.046	5.080
115	11.08	28.70	5.060	5.095
130	11.11	28.77	5.072	5.111
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Output Ripple (mV Pk-Pk)				
	90	125	23	12

Full Load Drop Out Voltage = 64-V RMS
Efficiency = (P_{out}/P_{in}) 100% = (4.98/5.86) 100 = 85%

Figures 12-15 show details of the power supply operation. The input voltage for all photos was 115 V RMS and all loads are at maximum. Table 1 gives the line and load regulation of the circuit along with output ripple and efficiency data. At 85% efficiency, absolutely no heatsinks are required.

CIRCUIT DESIGN DETAILS

Selecting the Input Capacitor

For a 90-V ac input, the bus voltage is

$$90\ \sqrt{2} = 127\ \text{V dc}$$

If 20 V of ripple is allowed, the lowest input voltage is 107 V dc. For some margin, use 100 V dc. For a 5-W output with 80% efficiency, $\eta = 0.8$;

$$P_{in} = P_{out}/\eta = 5/0.8 = 6.25\ \text{W}$$
$$I_{in} = P_{in}/V_{in} = 6.25/100 = 62.5\ \text{mA}$$

Input ripple is assumed to be 20 $V_{p\text{-}p}$. The low frequency limit is 50 Hz; thus, the ripple frequency is 100 Hz.

$$C = I \times \Delta T/\Delta V = (0.0625)\ (0.01)/20$$
$$= 31.25\ \mu\text{F}$$

33 µF is a standard value.

Finding the Peak Switch Current

At 100 V dc in, the maximum duty factor D = 45%.

$$I_{pk} = 2 \times I_{avg}/D_{max}$$
$$= 2\ (0.0625)/0.45$$
$$= 0.28\ \text{A}$$

The RMS switch current is

$$I_{RMS} = I_{pk}\sqrt{D/3} = 0.28\sqrt{0.45/3} = 0.11\ \text{A}$$

Switch Voltage Rating and Temperature Rise

The transformer primary voltage during the off-time will be independent of input line voltage but must be equal to or greater than the dc input voltage at low line. The maximum switch off-voltage equals the dc input at high line plus the transformer off-voltage. If the transformer off-voltage is assumed to be 125 V (the peak of the rectified sine wave at low line), then

$$V_{off(max)} = V_{in(max)} + 125\ \text{V}$$
$$= 130\sqrt{2} + 125 = 308\ \text{V}$$

Allowing approximately 100 V for the leakage inductance spike, $V_{DS(max)} \leq 408$ V. A 500 V FET gives a good safety margin. The IRF820 is rated 500 V, 3 Ω. For $T_J = 100°C$, the $r_{DS(on)}$ scale factor = 1.6, so the worst case on-resistance is

$$r_{DS(on)} = 3\ \Omega\ (1.6)$$
$$= 4.8\ \Omega$$

Conduction loss is

$$(0.11\ \text{A})^2\ (4.8\ \Omega) = 0.058\ \text{W}$$

Assuming switching losses are equal to conduction losses, total dissipation in the FET equals 0.116 W. With no heatsink,

$$\Delta T_J = (R_{\Theta JA})\ (P_{DISS})$$
$$= (80°C/\text{W})\ (0.155\ \text{W})$$
$$= 9.3°C$$

Primary Inductance

Operating frequency was selected at approximately 32 kHz to permit synchronization to a television horizontal scan if needed. Period $T_S = 31.25\ \mu\text{s}$, so

$$t_{on(max)} = (0.45)\ (31.25)$$
$$= 14\ \mu\text{s}$$

I_{pk} was calculated at 0.28 A and is also invariant with line voltage. At low line,

$$V_{in(min)} = 100\ \text{V and}$$
$$L_P = \frac{V\Delta t}{\Delta I} = \frac{100\ (14\mu\text{s})}{0.28} = 5\ \text{mH}$$

where

L_P = Primary Inductance
$\Delta t = t_{on(max)}$
$\Delta I = I_{pk}$

Flyback Inductor Design

Using the area product method,

$$A_cA_e = \frac{(25.32\ L_P I_{pk} D^2)10^8}{B_{max}} \qquad \text{(REF-2)}$$

where

D	= wire diameter in inches
B_{max}	= maximum flux swing in gauss
A_c	= core cross sectional area in cm^2
A_e	= effective window are in cm^2
A_cA_e	= core-window area product in cm^4

Assuming 400 cir/mil/A and 0.11 A RMS, #32 AWG is adequate. Use #31 for cool operation; the diameter of #31 AWG is 0.0108 inches. Allow B_{max} = 2000 gauss.

$$A_cA_e = \frac{(25.32)\ (5\ mH)\ (0.28\ A)\ (0.0108)^2\ (10^8)}{2000}$$

$$= 0.207\ cm^4$$

PQ 42020 size core has A_cA_e = 0.238 cm^4, so it should handle the power.

Find the air gap, l_g, as:

$$l_g = \frac{1.26\ L_P\ I^2_{pk} \times 10^8}{A_c\ B^2_{max}} = \frac{(1.26)\ (5.0\ E\text{-}3)\ (0.28)^2\ (10^8)}{(0.58)\ (2000)^2}$$

$$= 0.213\ cm$$
$$= 8.4\ mils$$

8 mils is a standard air gap.

Calculate primary turns, N_P. For the chosen core with an 8 mil air gap, the inductance factor, A_L = 363 mH/1000 turns.

$$N_P = 1000\sqrt{\frac{L_P}{A_L}}$$

$$N_P = 1000\sqrt{\frac{5.0}{363}} = 117\ \text{turns}$$

Solve for secondary turns, N_S. Based on the feedback winding,

$$N_S = N_P\frac{(V_O + V_f)\ (1 - D_{max})}{V_{in(min)}\ D_{max}} \quad \text{[See REF. 2]}$$

$$= \frac{(117)\ (10.0 + 0.7)\ (1 - 0.45)}{(100\ V)\ (0.45)} = 15.3\ \text{turns}$$

where

V_f	= diode forward voltage
V_O	= output voltage
D_{max}	= maximum duty factor
$V_{in(min)}$	= dc bus voltage at low line

Use 15 turns. This must be less than or equal to the calculated number of turns to ensure current reseting to zero during the off time.

Scaling voltages for other outputs:

$$10.7\ V/15\ \text{turns} = 0.7133\ V/\text{turn}$$

For all outputs:

$$V_{pk} = V_O + V_f$$

where V_{pk} is transformer secondary voltage.

$$N_S = V_{pk}/0.7133\ V/\text{turn}$$

After calculating all turn numbers and scaling slightly to optimize output voltage balances, the following turns resulted:

+30 V	43 turns
+12 V	17 turns
+5 V	8 turns
10 V bias	15 turns

9

Choose Wire Sizes. Core window area A_e = 0.384 cm^2. Allowing about a 50% fill factor results in a winding area of

$$0.5\ (0.384) = 0.192\ cm^2$$

#31 AWG was assumed for primary. The wire chart lists 1072 turns/cm^2 for #31 AWG.

$$117/1072 = 0.1091\ cm^2$$
$$0.192 - 0.1091 = 0.083\ cm^2 \text{ left for secondaries}$$

Scaling for the percentage of power output and allotting window area accordingly, the following wire gauges result:

30 V, #40 AWG. (This is about the smallest wire gauge one would use for reliable design and ease of manufacture.)

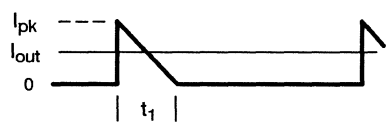
12 V, #25 AWG

5 V, #31 AWG both outputs

Feedback, #40 AWG for same reasons as +30 V output

Calculating Output Currents

To determine the peak and RMS output currents, the following equations apply:



Output Current Waveform

$$t_1 = \left(\frac{2\ (I_{out})\ A_L}{f(V_{out} + V_f)(10^9)} \right)^{1/2}$$

$$I_{pk} = \frac{2\ (I_{out})}{t_1 f}$$

$$I_{RMS} = \sqrt{\frac{t_1 f}{3}}$$

Where:

t_1 = current decay time
I_{out} = average load current
A_L = core inductance constant in mH/1000 turns
I_{pk} = peak secondary current
f = operating frequency

Results are as follows:

	I_{pk} (A)	t_1 (µs)	I_{RMS} (A)
12 V	1.60	12.85	0.59
30 V	0.11	2.34	0.017
$5_{(Aux)}$ V	1.08	4.60	0.24
$5_{(Main)}$ V	1.28	5.39	0.31
10 V bias	0.16	1.2	1.8

Selecting Output Diodes and Capacitors

Armed with the above data, selection of diode current ratings is possible using the RMS currents calculated. Also, the output capacitors can be sized based on the peak currents. The peak-to-peak ripple will be approximately equal to $(I_{pk})(ESR)$. On the 5 V, 80 mA output, due to a very low ripple specification, a two stage filter to minimize capacitor size was easiest to use. The inductor is a small ferrite core with a few turns of wire. The 30-V output needs only a couple of microfarads of capacitance if ESR = 0. A 2-µF ceramic capacitor fills the bill.

The timing resistor was initially selected at 500 kΩ (from the graph on the Si9120 data sheet) and was optimized empirically at 453 kΩ. Be sure to measure operating frequency on pin 5, as the scope probe capacitance on pin 9 will substantially alter the operating frequency.

Calculating the Primary Current Sense Resistor Value

The minimum current limit threshold is specified at 1 V. The calculated peak primary current is 0.28 A. Allowing approximately 25% over current,

$$I_{pk} = (0.28)\ (1.25) = 0.35\ A$$
$$R_{cs} = E_s/I_{pk} = 1.0/0.35 = 2.86\ \Omega$$

2.7 Ω is the nearest standard value. R6 and C6 set a 120 ns time constant on the current sense to filter noise spikes.

The blanking circuit differentiator time constant was selected at approximately 0.5 μs. R10 and R11 reduce the gate voltage amplitude to an acceptable level. R3 and R5 divide the feedback voltage down to 4.00 V. R5 was made adjustable for test purposes, and should be approximately 15 kΩ.

Loop Compensation

A frequently asked question is "How can I close the loop without a $40K analyzer?" Well, a number of techniques exist – some tedious, others not quite as bad. The most reliable approach is to apply a pulsed load to the output and empirically adjust the RC compensation for a well-damped exponential output-voltage recovery. With a little practice, this can be done expeditiously. It also has the advantage of showing any problems which may arise when one or more circuit elements are driven non-linear, as can occur during a large transient. This information is missing in a small-signal response plot. Be aware, however, that a load-pulse test lacks the quantitative information of a good Bode plot and fails to permit an accurate assessment of design margins. But with a little hands-on experience, it will be easy to get a good feel for when it's right.

Proceed as follows: Set C4 to approximately 0.1 μF. This sets the error amplifier to unity gain at approximately 100 Hz (Xc = R5 @ 100 Hz). Set R4 to zero. Set up the circuit shown in Figure 16. This allows a load step to be applied to the highest power output. If a bootstrap winding is not used for feedback, apply the step load to the regulated output. The amplitude of the step should be 25% to 50% of the full load current. The repetition rate should be low, around 100 Hz. Monitor the voltage on the V_{CC} pin of the Si9120, as this is controlled by the feedback loop, and watch the recovery characteristics. Gradually increase R4 and decrease C4 to obtain a good response.

Figure 17 shows the step response to several combinations of RC compensation. A small capacitor across R5 will also speed up the response, but may not be required. In addition, it may be desirable to add a small (100 to 1000 pF) capacitor directly across pins 14 and 15 of the Si9120 to roll off the error amplifier's high frequency gain. Be sure to repeat the above procedure for low and high input line voltages. When the response looks like line D in Figure 17, you're done.

CONCLUSION

Using the Si9120, the design of low-power, high-efficiency, switching power supplies for off-line applications becomes straightforward. By running a DCM flyback topology under current-mode control, a reliable, easily compensated design is achieved. The leakage inductance spike-blanking circuit presented here makes for a well-regulated supply while allowing VDE voltage-isolation requirements to be met.

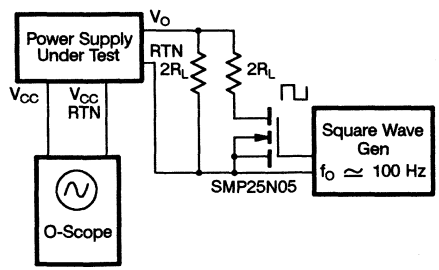


Figure 16. Pulse Load Test Setup

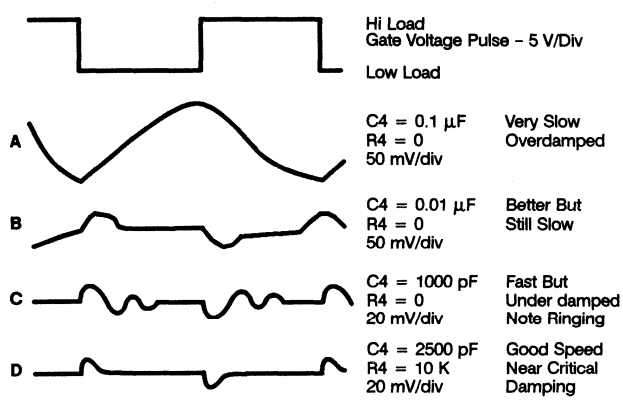


Figure 17. Step Response to Combinations of RC Compensation

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FLYBACK CONVERTER PARTS LIST

C1, C2 ..... 0.01 µF, 250 V ac, class X2
C3 ..... 33 µF, 200 V United Chemicon SL200VB33RU16X31LL
C4 ..... 2500 pF, 50 V ceramic
C5, C10, C12, C14, C16 ..... 0.1 µF, 50 V ceramic
C6 ..... 120 pF, 50 V ceramic
C7, C8, C9 ..... 1 µF, 50 V ceramic
C11 ..... 2200 µF, 16 V United Chemicon SXC16VB222M18X35LL
C13, C15 ..... 2200 µF, 6.3 V United Chemicon SXC6.3VB222M16X25LL
C17 ..... 220 µF 6.3 V United Chemicon SXC6.3VB221M10X12LL
C18 ..... 75 pF, 500 V (mica or ceramic)
C19, C20 ..... 0.0047 µF, 250 V ac, class Y
C21 ..... 220 pF, 50 V (ceramic)
CR1 ..... Bridge rectifier 600 V, 1 A
CR3 ..... MUR110
CR4 ..... 1N5822
CR5, CR6 ..... 1N5819
IC1 ..... Si9120DJ
L1 ..... Common-mode choke 8 mH
L2 ..... 13 µH: core: Magnetics Inc J40401TC with 6 turns # 26 AWG
Q1 ..... IRF820
Q2 ..... 2N7000
R1 ..... 453 kΩ .... 1% .... 1/4 W
R2 ..... 390 kΩ .... 5% .... 1/4 W
R3 ..... 10 kΩ ..... 1% .... 1/4 W
R4 ..... 10 kΩ ..... 5% .... 1/4 W
R5 ..... 15 kΩ ..... 1% .... 1/4 W
R6, R10 ..... 1 kΩ ..... 5% .... 1/4 W
R7 ..... 2.7 Ω ..... 5% .... 1/4 W
R8 ..... 10 Ω ..... 5% .... 1/4 W
R9 ..... 20 Ω ..... 5% .... 1/4 W
R11 ..... 2 kΩ ..... 5% .... 1/4 W
R12 ..... 510 Ω ..... 5% .... 1/4 W
T1 ..... Schott Corp #6712244

REFERENCES

1) Liu, K.H., *"Effects of Leakage Inductance on the Cross Regulation in a Discontunuous-Mode Flyback Converter,"* Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., *"High Frequency Switching Power Supplies,"* McGraw Hill 1984.

New Fast-Recovery Power MOSFETs Increase High-Voltage Motor Drive Efficiency

Jim Harnden

A new line of 500-V fast-recovery power MOSFETs from Siliconix contain stable and reliable intrinsic diodes with characteristics that rival ultra-fast-recovery discrete diodes with comparable voltage and current ratings. Reduced diode recovery time results in dramatically reduced switching losses, which – combined with standard power MOSFET advantages – are opening variable speed, off-line motor controls to a range of cost-sensitive applications that have previously been limited to simple "on-off" operation.

In low-voltage motor drive applications, power MOSFETs offer many benefits, including fast switching speeds, low forward and reverse leakage losses, and efficient gate drives. Furthermore, power MOSFETs offer another clear advantage when their intrinsic diodes can be used to eliminate discrete, fast-recovery power diodes which are used to "free-wheel" inductive flyback energy. Until now, however, as the breakdown voltage of the power MOSFET increased, the recovery time of its intrinsic diode stretched out proportionally. Thus, the same power MOSFETs used at switching rates above 1MHz in popular power conversion topologies (which do not require diode conduction) were often limited to operation at tens of kilohertz when their intrinsic diodes were used in high-voltage motor drives.

The only alternative to sacrificing the power MOSFET's inherently high switching rate was to isolate its intrinsic diode with a discrete series-blocking diode and a parallel high-voltage, ultra-fast recovery diode (Figure1). For low-voltage motor drives (where the fast-recovery times of some manufacturers' power MOSFETs allow their use without discrete fast-recovery diodes), several low-cost alternatives exist. But for 500-V drives, ultra-fast, high-current diodes often cost as much, and occupy as much heatsink space, as the power MOSFET. Early attempts to design semiconductor processes that provide high-voltage power MOSFETs with fast-recovery diodes yielded inconsistent results, which were directly reflected in increased component costs.

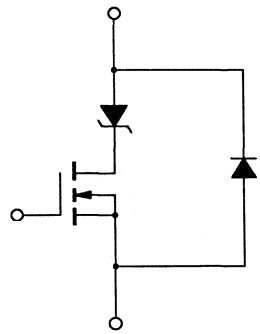
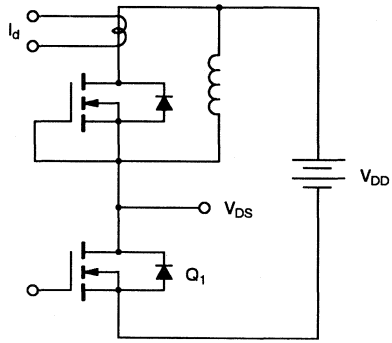


Figure 1. Circuit for Disabling a MOSFETs Intrinsic Diode

Siliconix New SMXXXN50F "Fast" Series

Four part numbers make up the new line of fast-recovery MOSFETs. The SMP3N50F, SMP5N50F, and SMP8N50F are, respectively, 3-A, 5-A, and 8-A, 500-V MOSFETs in TO-220 packages. The SMW14N50F is a 14-A, 500-V MOSFET offered in an industry-standard TO-247 package. Accompanying these new devices are data sheets with expanded characteristic curves that provide data which directly supports their use in high-voltage motor drives. These curves include reverse-recovery time vs. di/dt (T_j = 25 and 125°C), peak reverse-recovery current vs. di/dt (T_j = 25 and 125°C), commutating safe operating area, and dv/dt vs. di/dt.

The oscilloscope photographs in Figure 2 show the diode reverse-recovery characteristics (t_{rr}) of the standard IRF840 (2a) and the new SMP8N50F (2b). The multiple trace exposures record performance at 25, 50 and 75°C with an 8-A forward (diode) current and with recovery forced at 100 A/μs. As indicated, the new SMP8N50F recovers in approximately half the time and at half the peak current value. In both cases, t_{rr} increases by approximately 20 ns for each 25°C temperature change (valid up to 125°C).



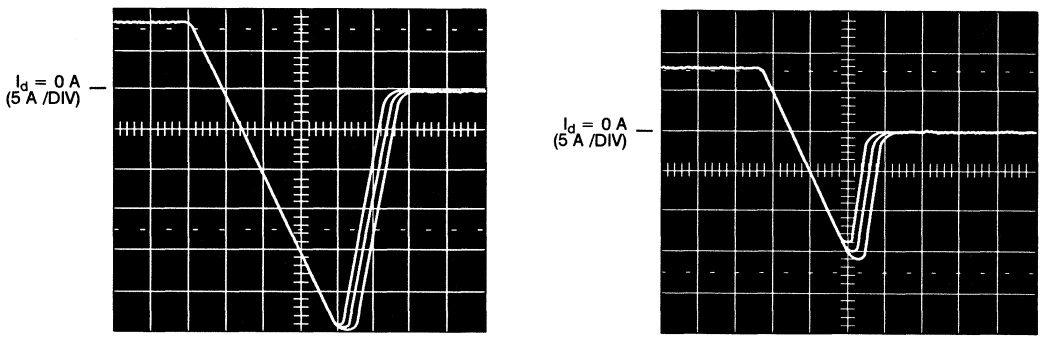


Figure 2. IRF840 vs. SMP8N50F t_{rr} Characteristics

Power Switching Efficiency

For any power switching circuit topology and load, the choice of switching devices and switching (modulation) frequency can significantly affect overall system efficiency. For resistive loads, the power MOSFET's losses can be grouped into three general categories (1 through 3 below). The other three categories (4 through 6 below) are specifically associated with the MOSFET's intrinsic diode and are only relevant for inductive loads.

1) Conduction (forward) losses (i.e., on-state losses or $r_{DS(on)}$ x current squared)

2) Switching losses (turn-on and turn-off)

3) Off-state losses (leakage)

4) Turn-on (diode recovery) losses

5) Diode forward conduction losses [V_d (diode forward voltage) x I_d (diode current)]

6) Diode switching losses (Q_{rr})

When driving resistive loads, power MOSFET off-state losses are confined to negligible leakage currents. With resistive loads, conduction losses are simply the power MOSFET's on-resistance ($r_{DS(on)}$) times the load current squared.

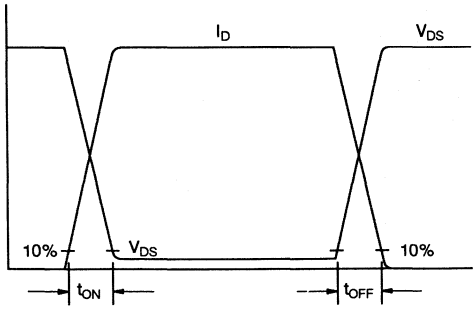


Figure 3. Resistive Load Switching Waveforms

With resistive loads (see Figure 3), switching times and, therefore, switching losses are primarily a function of the gate drive impedance, which is often limited by EMI/RFI considerations rather than power MOSFET limitations.

Integrating the product of current and voltage over the switching interval yields switching losses of

$$P_{on} + P_{off} = 1/6\,(V_{DS}\, I_D\, t_{on})\, f_o + 1/6\,(V_{DS}\, I_D\, t_{off})\, f_o \quad (1)$$

where

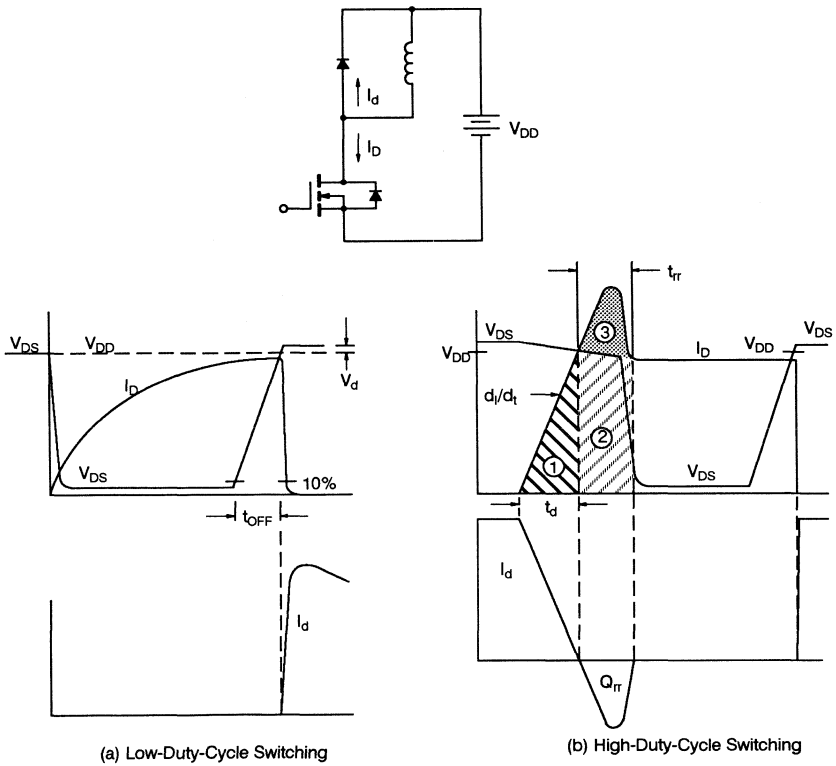
V_{DS} = voltage across the power MOSFET's drain-source

I_D = power MOSFET drain current

t_{on} = power MOSFET voltage turn-on transition time

t_{off} = power MOSFET voltage turn-off transition time.

When driving inductive loads, additional losses must be considered. Figure 4 illustrates a unipolar drive configuration with a discrete diode which clamps the inductor's flyback energy, preventing excessive voltage when the power MOSFET is switched off.



(a) Low-Duty-Cycle Switching

(b) High-Duty-Cycle Switching

Figure 4. Inductive Load Switching Circuit

With low-duty-cycle switching (Figure 4a) and/or low inductance values, the flyback energy has time to dissipate before the power MOSFET is switched back on. Inductor current increases slowly, compared to the power MOSFET's turn-on time, which results in negligible P_{on} losses. At turn-off, however, the drain voltage rises to its clamped (maximum) value before the drain current falls to zero. This rise results in increased peak power at turn-off compared to resistive load drives.

$$P_{off} = 1/2(V_{DS}\, I_D\, t_{off})\, f_o \qquad (2)$$

With higher inductance values (Figure 4b) and/or higher duty cycles (as is often the case in motor drive circuits), the MOSFET is turned on before the inductive flyback energy has reset to zero. In this case, the power MOSFET will be switched on in opposition to the forward diode current. Switching the power MOSFET on reverses the direction of current, which (when it exceeds flyback current) reverses the voltage across the diode. Any time the diode's voltage is reversed, some recombination time (t_{rr}) will be required before the diode recovers and blocks reverse current. This leads to the fourth category of losses in the power MOSFET which must be considered: turn-on (diode recovery) losses.

The power MOSFET's switching losses, when turned-on while the diode is conducting forward current (see Figure 4b), can be calculated as

$$P_{on} = \underbrace{1/2(V_{DS}\, I_D\, t_d\, f_o)}_{\text{(Region 1)}} + \underbrace{(V_{DS}\, I_D\, t_{rr}\, f_o)}_{\text{(Region 2)}} + \underbrace{(V_{DS}\, Q_{rr}\, f_o)}_{\text{(Region 3)}} \qquad (3)$$

where

V_{DS} = power MOSFET drain-to-source voltage

I_D = power MOSFET drain current

I_d = diode forward current

t_d = turn-on delay time

f_o = switching frequency

t_{rr} = diode reverse-recovery time

Q_{rr} = diode reverse-recovery charge.

As demonstrated, the reverse-recovery time dominates the losses that occur during this portion of the switching cycle. Until recovery occurs, the diode is free to conduct reverse current with the same low impedance it exhibits when conducting forward current. During this short-circuit condition, the peak "shoot-through" current level is primarily a function of the diode impedance and the power MOSFET's forward-transfer conductance (g_{fs}) times its applied gate-to-source voltage (V_{GS}).

The Half-Bridge Power Switching Configuration

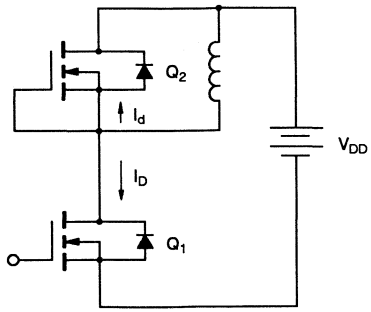
In the half-bridge configuration shown in Figure 5, the upper power MOSFET's gate has been shorted to its source to demonstrate the clamp diode portion of its function. Using the intrinsic diode to clamp the inductor's flyback energy contributes the fifth and sixth categories of power MOSFET losses: diode forward conduction losses [V_d (diode forward voltage) x I_d (diode current)] and diode switching losses (Q_{rr}).

The oscilloscope photographs in Figure 5 illustrate the diode reverse-recovery differences between the standard IRF840 and the new SMP8N50F used in the half-bridge configuration. V_{DS} (trace A) and I_D (trace B) are at 50 V/div and 5 A/div, respectively. The operating temperature is (approximately) 75°C, V_{DD} = 250 V, the time base is 200 ns/div, and the repetition rate is 20 kHz. At the 20-kHz rate, the recirculation current (I_d) is still effectively 5 A at turn-on.

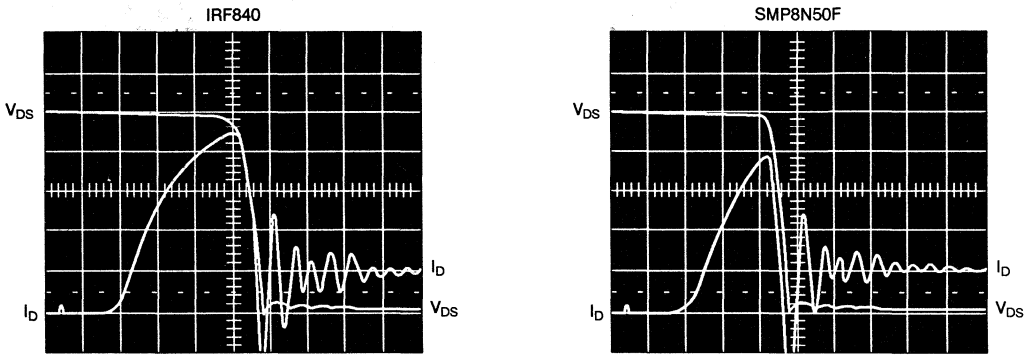
Using Equation 3 to calculate MOSFET Q1's turn-on switching losses for each case indicates 22 W for the IRF840 vs. 11 W for the SMP8N50F. These losses would increase approximately 5% at 100°C, where the absolute maximum power dissipation for both parts is rated at 50 W. The 11 W saved accounts for a full 22% of the maximum dissipation allowed in the power MOSFET at 100°C.

But this 22% savings is only part of the total t_{rr}-related power losses. In the case of the IRF840, the gate drive of MOSFET Q1 had to be limited to yield a di/dt rate of 50 A/ μs to prevent the peak current (during t_{rr}) from exceeding the power MOSFET's peak current rating (32 A). Maximum t_{rr} occurs with the maximum load current and, therefore, the maximum flyback current (5 A in this example).

At lower current levels and correspondingly faster recovery times, the system is forced to operate with less than optimal rise and fall times to attain safe operation under worst-case conditions.



(a) Half-Bridge Inductive Switching Circuit



(b) Half-Bridge Intrinsic Diode Recovery Waveforms

Figure 5.

Total system losses can be influenced substantially by optimizing the drive to allow maximum transition rates over the full range of motor currents. To address this, Siliconix is also introducing the Si9910 adaptive power MOSFET gate driver. One feature of the Si9910 is its ability to sense and limit the peak current during diode reverse recovery by regulating the turn-on rate (of MOSFET Q1). In this example, under low motor current conditions, the Si9910 and MOSFET Q1 could operate at much higher di/dt rates (limited only by system RFI/EMI considerations) and still not exceed the maximum peak recovery current under worst-case operating conditions.

Summary

Most inductive loads require clamping to prevent flyback energy from developing voltage levels that can damage the circuit. Traditionally, fast-recovery discrete diodes have been used for this purpose; however, since the advent of high-efficiency MOSFETs in motor drives, designers have searched for ways to reliably use the MOSFETs' intrinsic diodes in place of discrete diodes. In low-voltage motor drives, use of the MOSFET's fast-recovery intrinsic diodes has been commonplace, but at higher voltages, increased t_{rr} has resulted in increased losses. With the new Siliconix fast-recovery MOSFETs, the intrinsic diodes now rival the recovery times of ultra-fast recovery discrete diodes, offering efficiency without the added cost, area, and increased component count.

Siliconix incorporated

The Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications

Jim Harnden

The Si9910 is the first of a new generation of "adaptive" power MOSFET gate drivers. These adaptive drivers provide protection for the power MOSFET switching element while allowing direct control of high-voltage switching from logic signals. To achieve this protection, the Si9910 monitors the power MOSFET's operating conditions through feedback loops and alters its output characteristics.

The Si9910 adaptive driver allows the system designer to take full advantage of the increased performance and efficiency of power MOSFETs. Previous gate-drive techniques required designing a system for safe operation under worst-case conditions, even those which occur infrequently. Thus, these systems operated most of the time under less than optimum conditions with considerable performance and efficiency penalties. The Si9910, however, prevents power MOSFET destruction under worst-case operating conditions without compromising system performance and efficiency during normal operation.

Si9910 Circuit Description

The Si9910 is a single-channel, non-inverting CMOS driver with a low-impedance, emitter-follower output and a Schmidt trigger input (see Figure 1). To take full advantage of the efficiency offered by the power MOSFET's capacitive input impedance characteristic, the Si9910 was designed to have extremely low quiescent current and low output gate-drive impedance.

New "power IC" processes incorporating CMOS, DMOS, and bipolar device technologies are employed to optimize the Si9910 driver characteristics. The driver's CMOS logic section requires a maximum quiescent current of 1 μA (with the output high and the power MOSFET turned on), while the emitter-follower output stage is capable of delivering 1 A of peak current to quickly charge and discharge MOSFET gate capacitance. Using a bipolar emitter-follower output eliminates shoot-through and quiescent bias current losses in the low-impedance output stage.

High-Performance, High-Voltage Motor Drives

One potently damaging characteristic of a high-voltage motor-drive circuit is inductive flyback energy. Damaging voltages can result when inductor drive current is interrupted, unless some method is used to clamp the voltage and "free wheel" the inductive flyback energy (see Figure 2). For example, in unipolar motor-drive techniques, the flyback voltage is often clamped with a discrete diode to the motor supply or with a Zener diode to ground. One benefit that power MOSFETs offer is their intrinsic diodes which can serve as reliable and efficient voltage clamps.

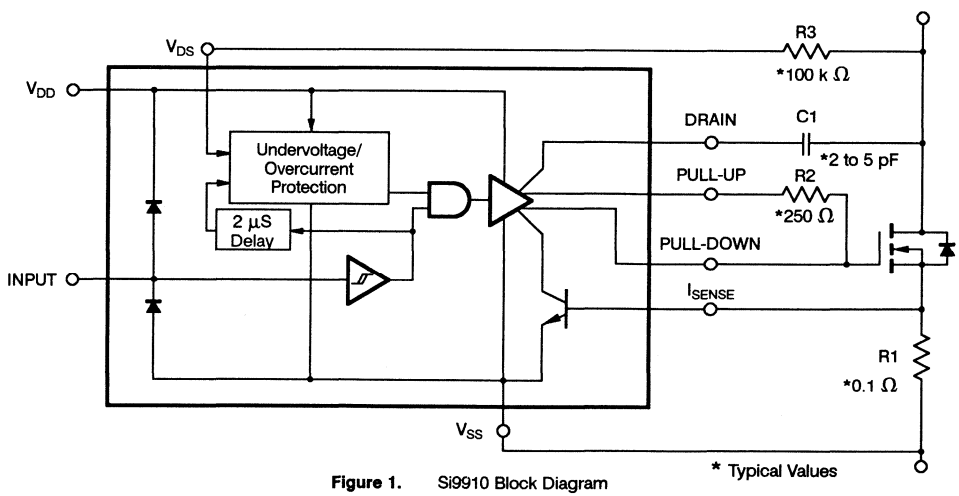


Figure 1. Si9910 Block Diagram

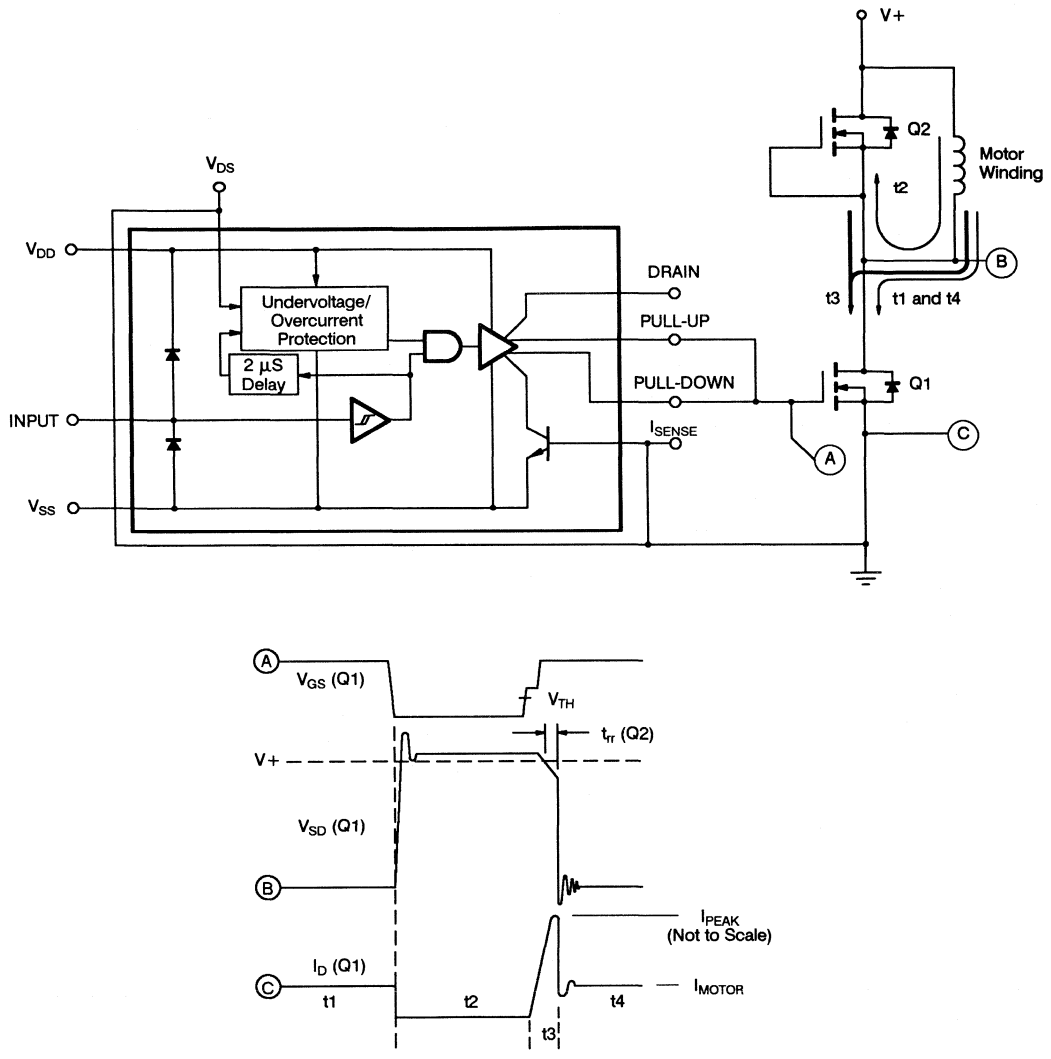


Figure 2. Clamping Inductive Flyback Energy

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Most high-performance motor drives require bipolar drive techniques (not to be confused with bipolar semiconductor technology). The power switching arrangement most commonly used is the half-bridge configuration. In a half-bridge, each motor winding is connected to a common node between switching devices that can connect it to either the motor supply voltage or to the motor supply return. In half-bridge drives, the MOSFET's intrinsic diode characteristics (especially reverse recovery time, t_{rr}) become very important[1] any time a motor winding's drive is interrupted and then re-enabled in the same path while flyback current is recirculating in an opposing clamp diode.

Protecting the Power MOSFET in Motor-Drive Applications

The half-bridge configuration shown in Figure 2 will be used throughout this article to demonstrate the problems associated with power MOSFET protection. The gate of the upper power MOSFET is shorted to its source so the MOSFET functions only as a clamp diode. The motor winding (inductive load) is shorted to V_{motor} at one end and switched by the lower power MOSFET at the other end. In an actual motor-drive circuit, both power MOSFETs in the half-bridge would be active and the other end of the motor's winding would be tied to another half-bridge. Depending on the modulation technique employed, any of the half-bridge power MOSFETs can be used to clamp flyback energy and can be exposed to reverse-recovery current spikes by being turned on in opposition to a conducting diode. The problems demonstrated by this simplified circuit are indicative of those exhibited by either the upper or lower MOSFETs in the half-bridge.

As shown in Figure 2, during time t1 the lower MOSFET (Q1) is turned on and load current is conducted through the inductor to ground. At the leading edge of time t2, Q1 is turned off and flyback current from the inductor recirculates through the intrinsic diode in MOSFET Q2. Shoot-through current occurs during time t3 when Q1 is switched back on. As Q1 turns on, it begins to conduct load current as well as reverse current through the diode of Q2. When enough reverse current has been conducted to sweep out the minority carriers in the diode of Q2, it begins to recover. Duration of the shoot-through current spike is dependent on t_{rr} (which is, in part, a function of the diode's previous forward current and the forced di/dt during recovery). The magnitude of the current spike depends on the gate-drive voltage and forward transfer conductance (g_{fs}) of Q1 at the time of Q2 diode recovery and can be many times greater than the motor current.

Limiting the MOSFET's di/dt

As mentioned above, the current spike duration is dependent on the power MOSFET t_{rr} which is, in turn, a function of the diode forward current (motor flyback current) and di/dt during the forced recovery. Most commercial power MOSFETs have t_{rr} ratings specified with a recovery di/dt of 100 A/μs. Recovering at higher or lower di/dt rates will not change the amount of charge which must be "swept" out of the bipolar junction before recovery. Recovering at a higher di/dt rate results in higher peak currents of less duration. The only MOSFET failure mode *directly* triggered by excessive di/dt arises when it results in a peak current that is sufficient to force the MOSFET outside of its safe operating area (SOA).

Until now, limiting di/dt has often been a technique used to limit the maximum rate of dv/dt (and its associated failure modes of commutating dv/dt and SOA).[2] In a half-bridge that uses the adaptive controls of the Si9910, both the maximum recovery current and associated commutating dv/dt, which only occur when the system is delivering maximum motor current, are directly controlled.

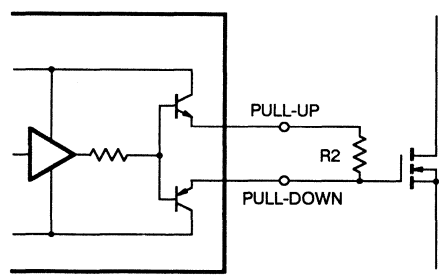


Figure 3a. Simplified "Split" Emitter-Follower Output Circuit

[1] Addressing this issue in high-voltage (500 V) applications is a new line of MOSPOWER transistors from Siliconix with intrinsic diode recovery times rivaling discrete fast-recovery diodes. However, even these fast-recovery diodes don't solve all the problems associated with flyback energy and diode recovery. Power MOSFETs are capable of extremely fast voltage transitions and no commercially available 500-V diode (discrete or intrinsic) will be fast enough to allow the system switching losses to be absolutely minimized without regard to potentially damaging shoot-through currents.

[2] To recap, commutating or recovery dv/dt is proportional to the peak current level at the point of recovery. Peak recovery current is directly related to di/dt and t_{rr}. And a power MOSFET's t_{rr} increases as the diode's forward current increases, which is a direct function of the motor's winding current.

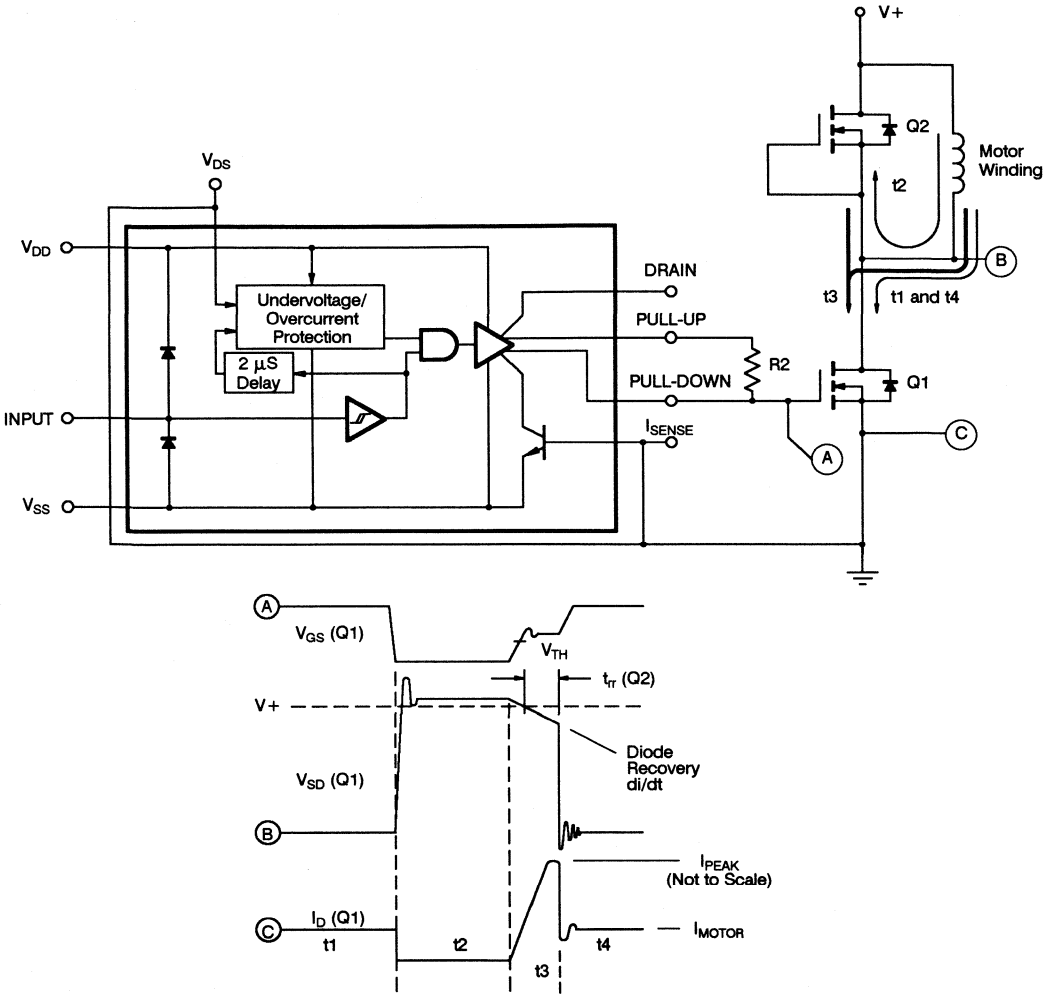


Figure 3b. Controlling di/dt via MOSFET Gate Drive Impedance

The "split" emitter-follower output (Figure 3a) of the Si9910 allows the addition of a single external resistor to set the maximum rate of system di/dt during MOSFET turn-on (Figure 3b). This is a system parameter that is independently set and is not effected by variations in load current or operating conditions. With power MOSFETs, di/dt is a function of total gate capacitance during an "on" transition and the gate driver's pull-up resistance. Once a gate drive impedance and gate capacitance is established, di/dt will vary only as a result of dv/dt variations which reduce the amount of charge coupled to the MOSFET gate through the device's reverse transfer capacitance (Miller feedback capacitance).

As the value of gate-drive resistance (R2 in Figure 3b) is increased, the dv_{GS}/dt of Q1 (during time t3) is reduced. The MOSFET's conducted current is a direct function of its gate voltage and transconductance (g_{fs}). Therefore, restricting dv_{GS}/dt directly reduces di/dt.

With the Si9910 adaptive MOSFET driver, the pull-up gate-drive resistance (R2) can be calculated based on a safe system di/dt level, without regard to peak current or dv/dt protection of the power MOSFETs.

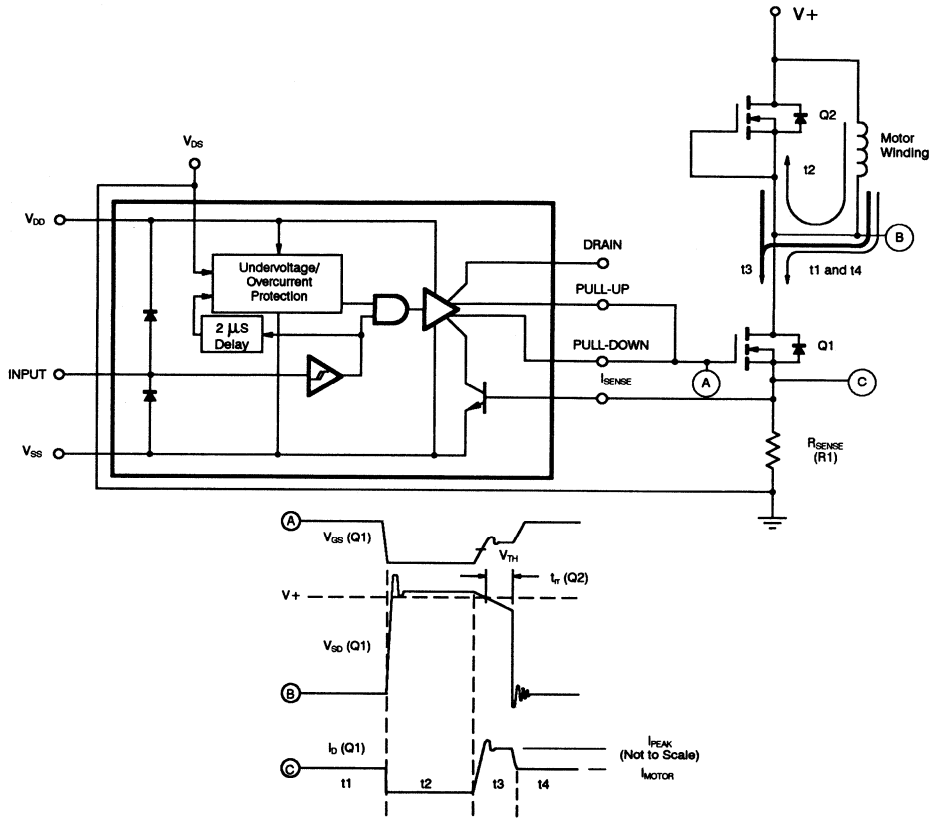


Figure 4. Limiting Peak Current

Limiting the t_{rr}-Induced Shoot-Through Current Level

The Si9910 I_{SENSE} input can be used in conjunction with a very low-value external sense resistor to directly limit the maximum peak current (Figure 4). Figure 5 illustrates a simplified schematic of the Si9910's peak current limiting circuit. When the voltage drop across the external sense resistor (R_{SENSE}) exceeds the V_{BE} of internal transistor Q3, it begins to turn-on, shunting further increases in voltage at the common base of the output emitter-follower and, therefore, the MOSFET's gate-drive voltage (during time t3 in Figure 4).

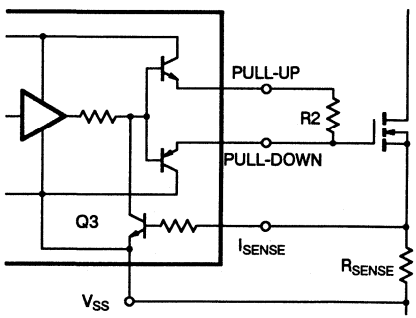


Figure 5. "Simplified Peak Shoot-Through Current Limiting Circuit

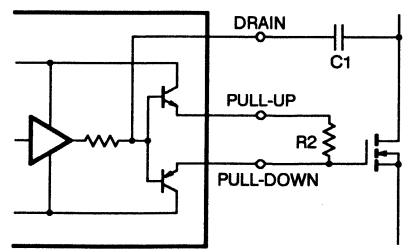


Figure 6. Simplified dv/dt Feedback Circuit

The value of external resistor R_{SENSE} should be calculated to limit the maximum shoot-through current level. The I_{SENSE} feedback is not intended to limit motor current since it restricts the MOSFET's dv_{GS}/dt, leaving the MOSFET in transition for a longer period of time. R_{SENSE} should be sized to limit current at a level approximately four times greater than the peak motor current.

$$R_{SENSE} = \frac{0.8\ V}{4 \times \text{Peak Motor Current}}$$

This transient current level is consistent with the power MOSFET's peak current rating which (in most commercially available power MOSFETs) is four times the continuous current rating.

Directly Limiting the MOSFET's dv/dt

Figure 6 is a simplified schematic of the Si9910's feedback circuit used to sense and limit maximum half-bridge dv/dt. As the common base of the emitter-follower stage changes from a low to a high level, the output follows, turning the power MOSFET on. As the power MOSFET switches on, the voltage across its drain-source decreases rapidly. The rate of dv/dt will depend on all of the conditions described earlier that are associated with diode reverse recovery. When a switching transition occurs, it will couple charge through the external capacitor (C1) which decreases the rise time of the emitter-follower's common base and, in turn, limits the dv_{GS}/dt of the power MOSFET. In a typical motor-drive circuit, maximum dv/dt will only occur during worst-case motor current, which is a transient condition. This technique permits faster switching (and higher efficiency) during normal operation and provides dv/dt protection for the MOSFETs when it is required.

The drain input must be limited to low voltage, which requires connection to the MOSFET's drain via a capacitor capable of withstanding the full motor-drive voltage (Figure 7).

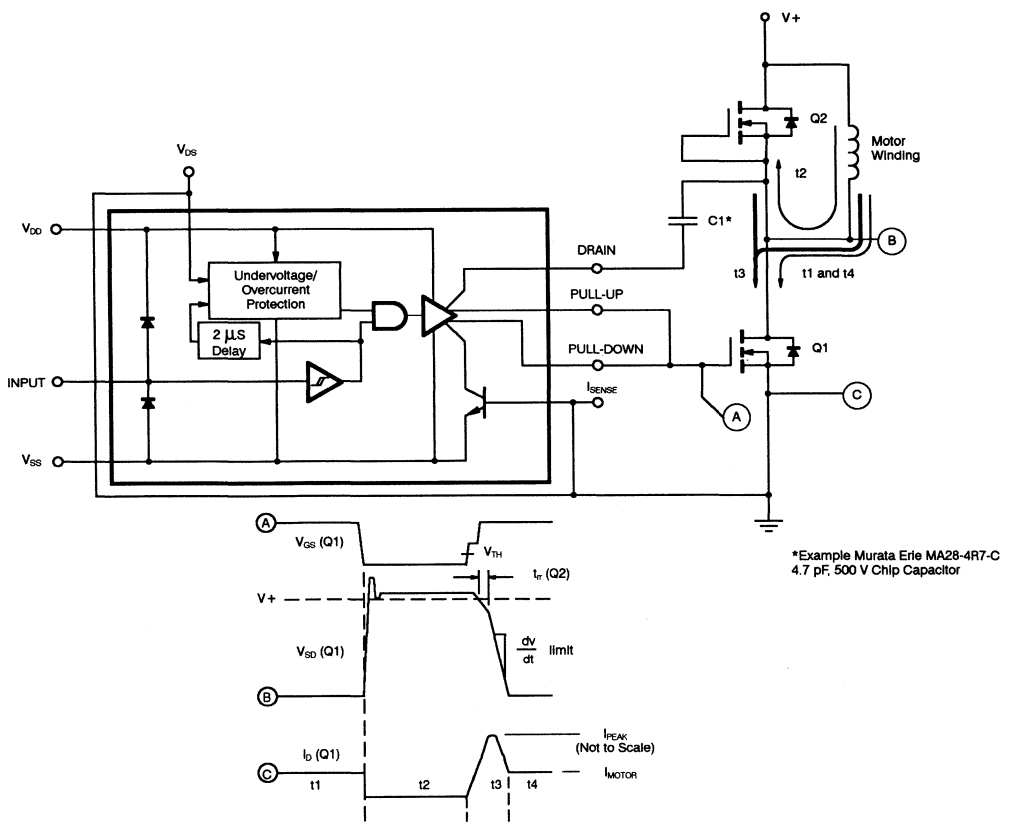


Figure 7. Direct dv/dt Limiting

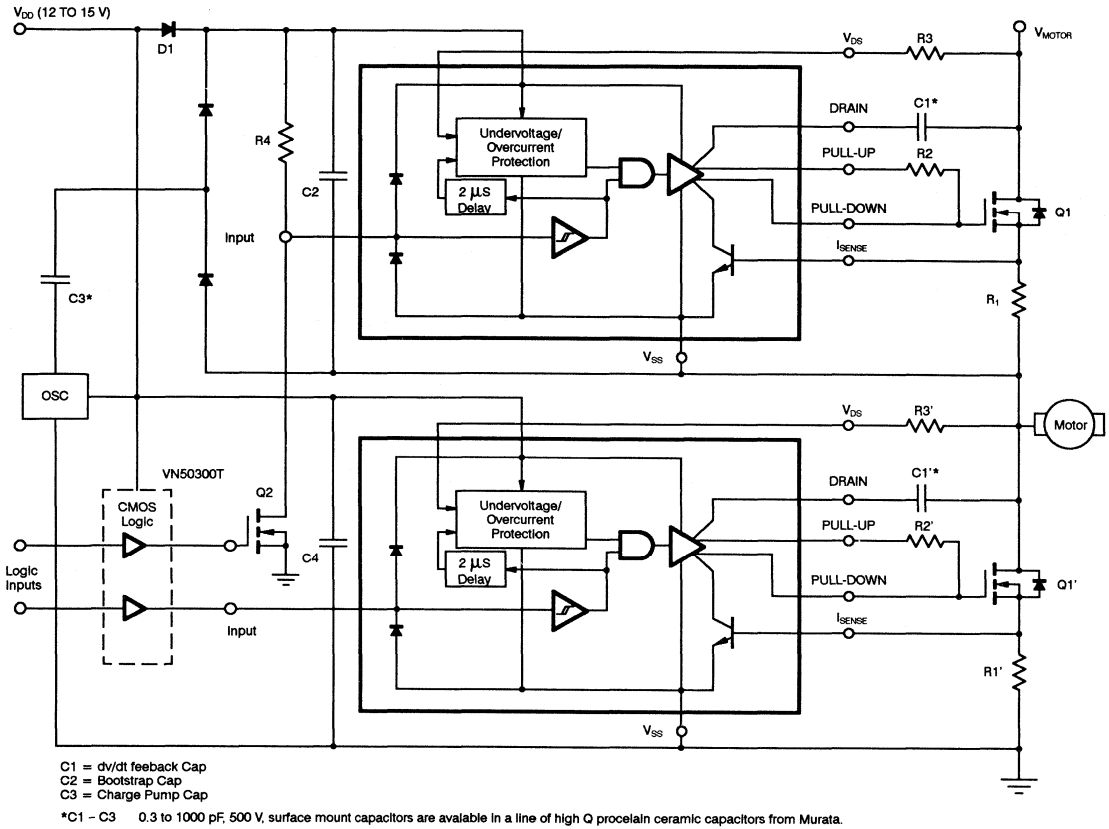


Figure 8. High-Voltage Half-Bridge with Si9910 Drivers

The Si9910 in "Floating" High-Side Drive Applications

As demonstrated in Figure 8, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 facilitate its use in half-bridge high-side drive applications.

The Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses, but it does not provide static (100% duty-cycle) drive. Eventually the bootstrap capacitor's charge will be depleted by system leakages, resulting in reduced (potentially damaging) levels of gate-drive voltage. A charge pump circuit can provide static operation but usually yields increased gate-drive impedance, which ultimately results in slower transition rates and increased switching losses. As the charge pump capacitance is increased to provide faster transition rates, the oscillator circuit is subjected to higher peak currents in the presence of the dv/dt rates that exist in half-bridge motor drives. This limits the extent to which the charge pump capacitor can be increased.

The Si9910 is configured to take advantage of either floating supply technique, (if the application is not sensitive to their particular limitations), or a combination of both techniques (if switching losses must be minimized and static operation is necessary). Figure 8 illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

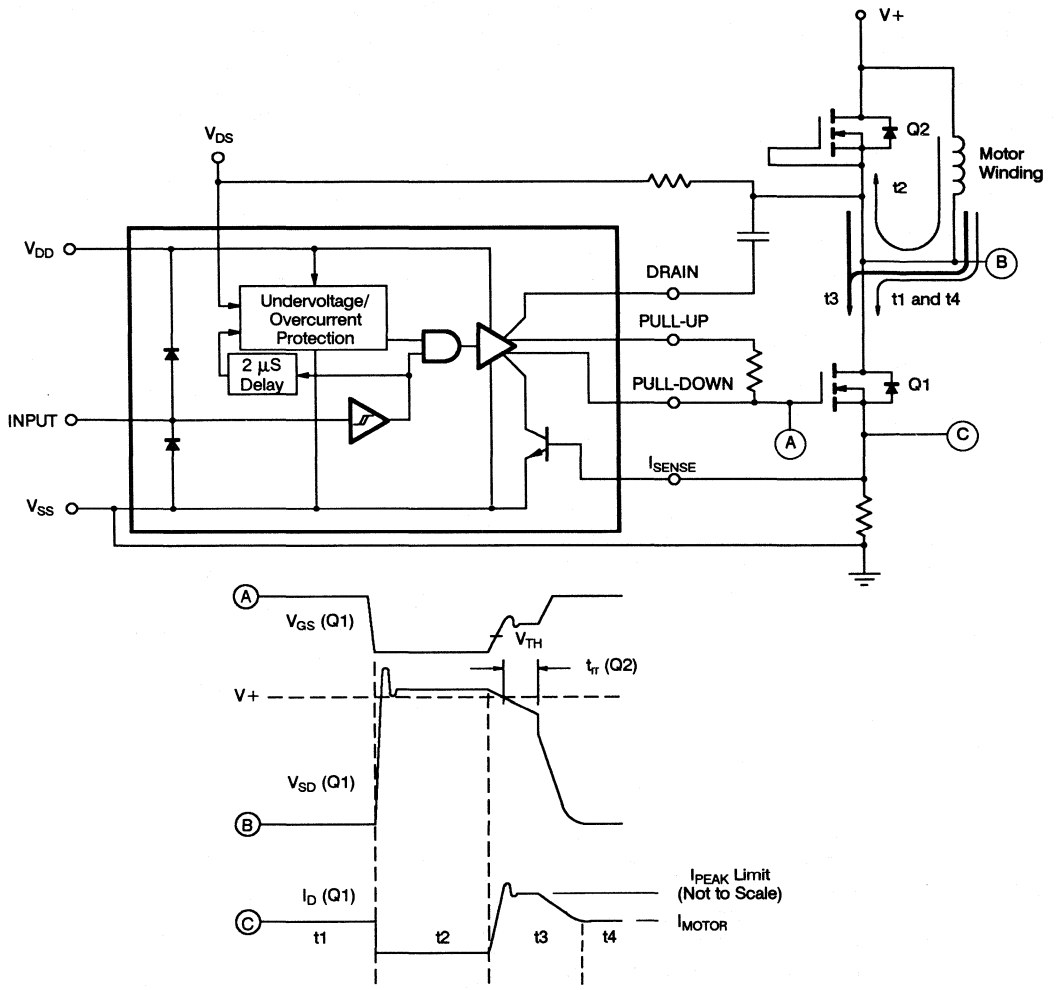


Figure 9. All Feedback Options Active

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, sufficient time must be allowed to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As protection against catastrophic transient conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate.

Maximum V_{DS} Monitor

The Si9910 V_{DS} input monitors the source-drain voltage drop across the MOSFET in the "on" state. Excess V_{DS} can occur as a result of high on-resistance ($r_{DS(ON)}$) at increased temperature, insufficient gate enhancement voltage, or excessive current. Regardless of the cause, the effects can be catastrophic. The first priority of the Si9910 is to protect the power MOSFET. Therefore, a maximum V_{DS} monitor is enabled 2 µS after each positive-going input transition. Voltage exceeding the V_{DS} maximum (data sheet limit) will cause the gate driver to go to a low state and to wait for the next positive-going input command.

The V_{DS} pin is a low-voltage input which must be isolated from the high voltages at the power MOSFET's drain by an external resistor. The value of the external resistor is not critical to the operation of the maximum V_{DS} shutdown circuit. A 100-kΩ resistor is sufficient to isolate the high-voltage with minimum power losses and still drive the low capacitance input with tolerable response times.

Input Level Translation

Input logic signals must be level shifted to control the driver in the high-side of a half-bridge application. The circuit illustrated in Figure 8 uses a simple passive pull-up (R4) and a high-voltage, small-signal MOSFET (Q2) for level translation. The VN50300 was selected for its extremely low drain capacitance (1.8 pF typical). The drain capacitance of Q2 is important because of the direct effect it has on the value of R4.

The value of R4 should be sufficient to provide an RC time constant that is faster than the turn-on rate of Q1. The capacitance that must be driven is the total at the Si9910's input node (2 pF typical for the Si9910 plus 1.8 pF typical for the VN50300 plus any stray wiring and board capacitances).

R4 must also have a value that is high enough (relative to the on-resistance of Q2) to maintain a logic level of zero (3 V maximum) when the low-side device is turned on.

The minimum value of R4 necessary to achieve a safe RC time constant depends on the turn-on rate of Q1, which can be altered by adjusting the value of R2. (For most mid-sized MOSFETs [1000–3000 pF C_{iss}] typical values are 250 Ω for R2, 5 pF for the input-node capacitance, and 10 kΩ for R4.) Observing the half-bridge's positive-going output-voltage transition with an oscilloscope will reveal any "input-laging-output" imbalance as a sawtooth voltage waveform. Trying to observe the input-voltage transition directly is difficult since addition of any scope probe capacitance can significantly alter the node's switching characteristics.

Some applications will require current limiting of Q2. It is common, for instance, in brushless, three-phase motor drives to encounter a condition where both the high and low-side MOSFETs (Q1 and Q1') are off for some period during each cycle. During this time, for a particular phase, Q2 will be on, but since the lower output MOSFET is not on, the output voltage from the bridge is defined by the back EMF of the motor (which may be as much as 80 to 90% of V+ at maximum velocity). If Q2 is a VN50300, inherent protection results from the device's low saturation current capability (see the VN50300 characteristic curves in Siliconix Low Power Discretes Data Book). If level-shift devices that have higher-saturation current capability are substituted, measures may have to be implemented (such as series resistance in the source or drain of Q2) to protect the level-shift device and/or the input of the Si9910.

Flexible Feedback Options

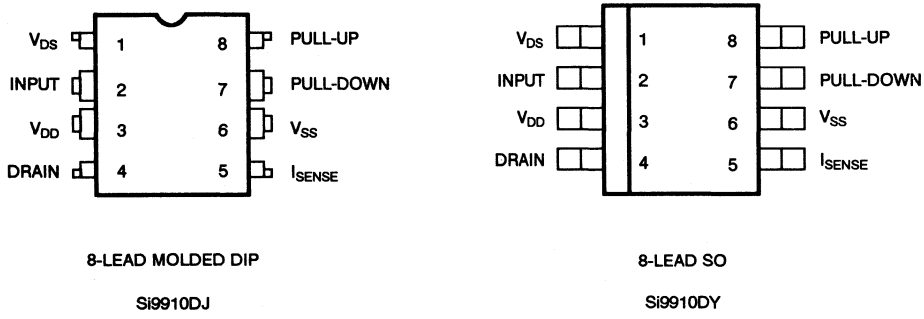
Each of the feedback options – dv/dt limiting, peak current limiting and maximum V_{DS} – may be used separately or in any combination. Figure 9 shows all the external feedback options connected and the resulting voltage/current waveforms. If the designer chooses not to use the V_{DS} input to monitor maximum V_{DS}, it should be tied to V_{SS}. When the drain input is not in use, it must be left open. When the I_{SENSE} input is not in use, it should be shorted to V_{SS}.

Packaging Concept: Using Surface-Mount Si9910s with Power MOSFET Chips

Using surface-mount driver ICs, such as the Si9910DY shown in Figure 10, on a substrate with power MOSFET chips holds great promise for next-generation motor drives. The power MOSFET can be mounted directly on a substrate with good thermal transfer characteristics, thus solving the density and power dissipation problems commonly associated with motor controllers. Power MOSFETs are relatively easy to handle in die form and can be tested prior to packaging. Handling ICs in die form, however, presents problems which can be avoided with low-cost, compact surface-mount packages such as the Si9910DY.

Summary

The Si9910 introduces a new generation of "adaptive" power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. The Si9910's first priority is to protect the power MOSFET that it drives. When all of its protective options are enabled, the Si9910 is capable of controlling the power MOSFET dv/dt, di/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop. The Si9910 allows the system designer to take full advantage of the increased performance and efficiency characteristics of power MOSFETs by designing the system with optimized switching losses and efficiency, while leaving worst-case system protection to the driver.



8-LEAD MOLDED DIP

Si9910DJ

8-LEAD SO

Si9910DY

Figure 10. Si9910DY and Si9910DJ Package Pin-Outs

Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals

James Blanc

Integrated Services Digital Network (ISDN) standards are a major step towards the realization of a worldwide information grid. Just as power system standards allow the connection of either a microwave oven or a television set into a power recepticle, so ISDN will allow information appliances, such as fascimile machines, computer terminals, and telephones to plug into a standard socket. It will be possible to move office equipment either down the hall or around the world and immediately "plug in" to the information grid. ISDN will allow the travelling worker to communicate (using portable computers and fascimile machines) with customers or manufacturing sites worldwide. And this will be accomplished without modems, which slow data transmission rates.

One of the larger technical problems in achieving such a powerful information network is that the existing telephone system was designed over eighty years ago for the more limited purpose of reliably transmitting voice signals. Plain old telephone service, or POTS, has such an excellent reliability record that the general public takes for granted that the phone still works when the lights go out. But the simple power feeding method (a central office battery connected to the telephone via a pair of copper wires) is inadequate for ISDN. Nonetheless, ISDN must not achieve upgraded data communication capability at the expense of voice communication reliability. That is, when the lights go out, the new digital telephones must still operate.

The Deutsche Bundespost (DBP) took the lead several years ago[1] in defining a methodology for feeding power to ISDN terminals which is compatible with the data transmission requirements of ISDN and the reliability requirements of POTS. The DBP proposals have been incorporated into the CCITT standard I.430, which defines the physical characteristics of the ISDN interfaces. [The Consultative Committee for International Telegraph and Telephone (CCITT) is part of the International Telecommunications Union of the United Nations.] The standard calls for galvanic isolation in terminal equipment (TE) connected to the subscriber- or S-bus. This requires the use of an efficient switchmode dc/dc converter in each TE. Also, while the older analog telephony circuits can get by on about 100 mW, the new digital telephones (D-phones) require approximately 300 mW.

Up to eight D-phones or other TEs can be connected to each S-bus, but the CCITT recommendation allows that only one terminal be operational during restricted power conditions. When the network terminal (NT) senses the loss of normal power, it reverses the polarity of the dc feeding voltage on the S-bus. Non-emergency-designated terminals have a reverse polarity diode which effectively removes their loads from the S-bus during the outage. The emergency-designated terminal uses a diode bridge at the input, so that it remains connected across the bus at all times. This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc/dc converter which conforms to the international standard.

CCITT Standard I.430

Table I summarizes the CCITT document as it applies to dc/dc converters in emergency-designated TEs. During normal-mode operation, terminals may have multiple power sources, including up to 1 W from the S-bus (Power Source 1), whose dc voltage must be between 24 and 42 V measured at the input to the TE. During the restricted power condition the designated TE in the active state must draw less than 380 mW from Power Source 1 (PS1), and the input voltage magnitude must be 32 to 42 V. Eighty percent efficiency has previously been demonstrated for dc/dc converters at these power levels[2].

The difficult problem presented by the CCITT specification occurs when the phone is on-hook (deactivated state) during the restricted power condition. In order that the terminal be capable of receiving incoming calls, the line activity detection circuitry in the TE must continue to operate while the total power consumption must be maintained below 25 mW. Also, the "Terminal Endpoint Identifier (TEI)" must be retained, which means that some power is required for memory holdup. These functions require approximately 13 mW, and the input voltage is still in the 32- to 42-V range.

Needless to say, off-the-shelf +40-V to +5-V dc/dc converters with 55% worst-case efficiency at an output power level of 13 mW do not exist today. They can, however, be designed using readily available off-the-shelf components,but the methodology for their design is different from that of conventional power supplies.

Table I. Power Source 1 Requirements Emergency – Designated ISDN TE's

Power Mode	TE State	Voltage Range	Max Power to TE
Normal	Active	+ 24 to +42 V	1 W
Normal	Deactivated	+24 to +42 V	100 mW
Restricted	Active	-32 to -42 V	380 mW
Restricted	Deactivated	-32 to -42 V	25 mW

Design Methodology

A flyback converter topology provides galvanic isolation while requiring only one magnetic energy storage device. This minimizes cost since inductors and transformers are the most expensive components in switch mode power converters. Selection of the primary inductance value was discussed in a previous Siliconix Application Note, AN87-2, which analyzes the start-up constraints of dc/dc converters fed from high-impedance sources. The result of that analysis was a primary inductance of 3.75 mH. Since the S-bus is relatively short compared to the subscriber loop, and it is fed from a dc/dc converter in the NT, the source impedance seen by the dc/dc converter in the TE is relatively low. This indicates that a lower primary inductance, L_P, can be chosen, which allows the inductor to be smaller.

There is, however, another reason to utilize a high inductance value. The energy transferred to the inductor during each cycle is given by Equation 1.

$$E = \tfrac{1}{2} L_P I_{PK}^2 \quad (1)$$

I_{PK} is the peak inductor current, and it is assumed that the initial current is zero. The same amount of energy transfer can be achieved with a small L_P and large I_{PK}, or vice versa. But the RMS value of the current is less for the case of large L_P and small I_{PK}. This reduces the conduction losses in the primary winding, MOSFET, and sense resistor, which is essential to achieving high efficiency at the milliwatt power level. With a total power budget of only 25 mW, every milliwatt lost causes a four percent reduction in efficiency.

To minimize dynamic losses, defined as those dependent upon operating frequency, it is advantageous to use the smallest switching frequency, f_S, which is practical. If possible, this frequency should be above the audible range. 18 kHz was selected for the nominal switching frequency when the oscillator is free-running (36 kHz for the oscillator, which includes a divide-by-two). This occurs during start-up or under restricted power conditions. For operating conditions other than the deactivated state in the restricted power mode, a system clock should be available. It is desirable to synchronize the dc/dc converter to a signal derived from this clock to minimize noise coupling into the A/D and D/A converter (CODEC) circuits. The synchronization frequency should be 10 to 20% above the free-running frequency.

Another choice must be made which has a large impact on the dc/dc converter cost, light load efficiency, and output voltage regulation. Voltage feedback must be implemented while at the same time maintaining galvanic isolation. There are two possible approaches. The first is to use optical isolation and place the error amplifier and voltage reference on the secondary side. This gives the best result in terms of load regulation, but it costs more and it decreases light load efficiency. The error amp and reference generator could be eliminated from the primary side controller and put into a separate IC on the secondary side. For these components, the power losses thus remain approximately the same. But the optical isolator consumes some additional power and increases total converter cost.

The second option, which is used here, is to employ an auxiliary winding to indirectly sense the output voltage. This winding is essentially free, since it must be used anyway to provide the bootstrap supply for the switchmode regulator IC. Using this technique, the output voltage regulation is dependent upon the coupling between the secondary and auxiliary windings as well as upon the switching frequency. The total variation in output voltage as the load current is varied from the minimum (3 mA at +5 V, 0 mA at -5 V) to the maximum level (100 mA at +5 V, 30 mA at -5 V) was 10%. This should permit a specified regulation range of ±7% at the converter output. If tighter regulation is required for a given application, then the opto-isolation approach will be required.

Circuit Description

The complete schematic for the dc/dc converter is given in Figure 1, and the block diagram of the Si9105 switchmode regulator IC is shown in Figure 2. The Si9105 is a variation of the original Si9100 switchmode regulator which was introduced in March, 1987. It includes an oscillator, an error amplifier, a pre-regulator/start-up circuit, a trimmed voltage reference, low-power CMOS logic and comparators, undervoltage lockout and current-limit protection circuitry, and a high-voltage MOSFET transistor -- all on a single chip in a 14-pin DIP or 20-pin PLCC for surface-mount assembly.

The block diagram of the Si9105 is the same as that for the Si9100, but several key specifications are upgraded. The most important specification here is the maximum power dissipation of the chip. The supply current, I_{CC}, is 0.5 mA maximum (0.35 mA typical), giving P_D = 5 mW maximum for V_{CC} = 10 V. The start-up circuit shuts off the 120-V rated pre-regulator transistor after start-up so that I_{CC} is taken from the auxiliary 10-V output rather than from the 40-V input bus. The power saved is approximately

$$P_{Saved} = (40\ V)(0.35\ mA) - (10\ V)(0.35\ mA)$$
$$= 14\ mW - 3.5\ mW = 11.5\ mW \quad (2)$$

Without such an auxiliary supply, it is easy to see from Equation 2 that 55% efficiency with 25 mW at the input is not possible.

The 4-V reference of the Si9105 is a temperature compensated buried Zener, which is trimmed to 1% initial accuracy at a specified bias current of 7.5 µA. This is one-half of the bias current specified for the Si9100, and a bias resistor equal to 820 kΩ from pin 1 to ground is all that is required to program I_{BIAS}. Finally, the MOSFET switching transistor in the Si9105 has been rated at a higher breakdown voltage, 200 V versus 150 V, at the same time its $r_{DS(ON)}$ has been maintained at 5 Ω maximum.

The other key component in the converter circuit is the coupled inductor, L1. Pulse Engineering* has provided a cost-effective inductor design, part number PE65451, specifically designed for this ISDN terminal application. L1 has an isolation voltage specification of 1750 V_{RMS}.

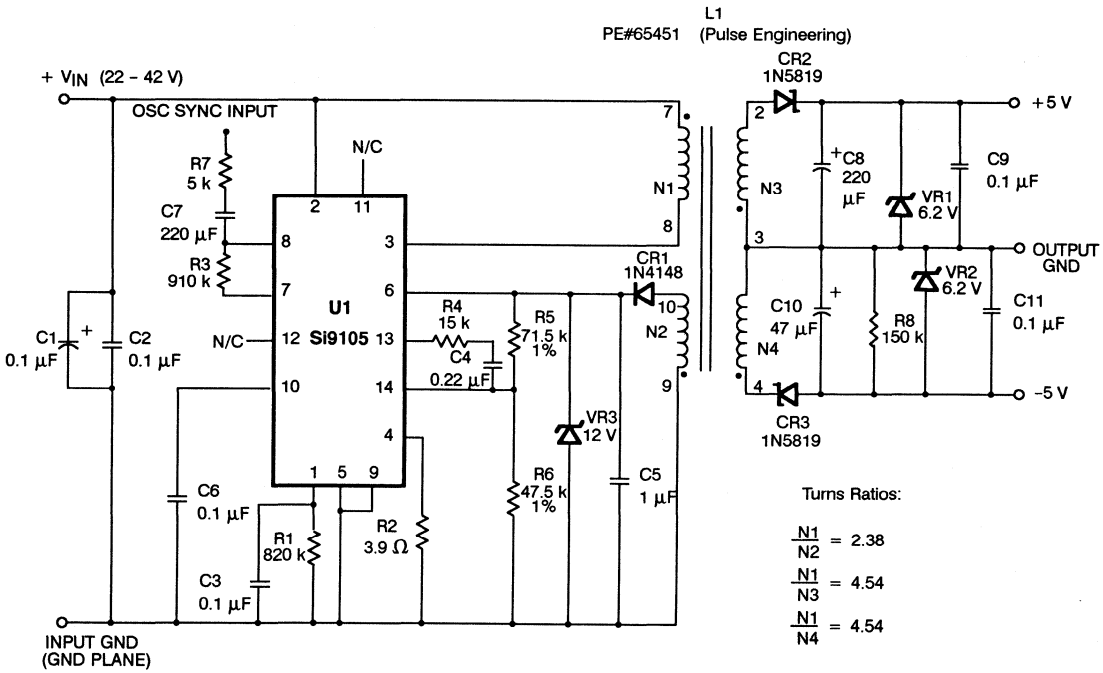
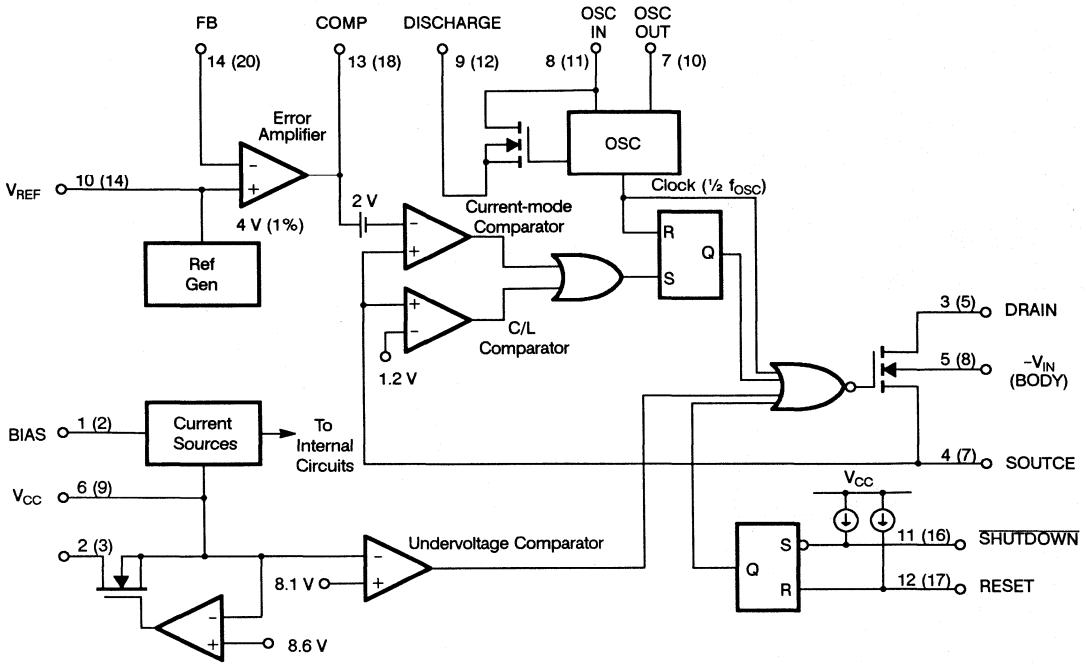


Figure 1. dc/dc Converter Schematic for Emergency - Designated ISDN Terminals

* Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, (619) 268-2400



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

Figure 2. Si9105 Block Diagram

Measured Circuit Performance

Figure 3 shows an oscilloscope photograph of the primary side voltage and current waveforms for operation under the emergency load conditions. The calculated peak current is

$$P_{IN} = 25\ mW = \tfrac{1}{2} L_P I_{PK}^2 f_S$$

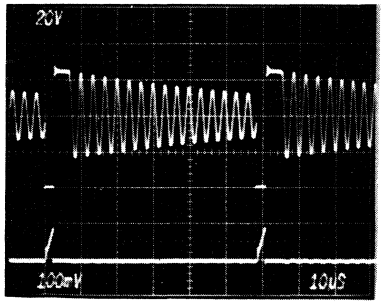
For $L_P = 3.8$ mH and $f_S = 18$ kHz, I_{PK} equals 27 mA. The MOSFET conduction time is calculated from

$$\frac{V_{IN}}{L_P} = \frac{I_{PK}}{t_{ON}} \qquad (4)$$

For $V_{IN} = 40$ V, $L_P = 3.8$ mH, and $I_{PK} = 27$ mA, t_{ON} is equal to 2.6 µs and the duty cycle is (2.6 µs)•(18 kHz) = 0.046 (or about 5%). Figure 4 shows the corresponding waveforms during full load operation.

An efficient power supply which self-destructs when its output is shorted to ground is of limited value. Some additional components are needed to protect the power supply and its loads from overcurrent and overvoltage transients. Figure 5 shows the converter waveforms with the output terminals shorted to ground. Note that the converter goes into the continuous conduction mode of operation (the current waveform is trapezoidal), but the dc input current was measured at 10.5 mA. The power dissipation of (10.5 mA) • (40 V) = 420 mW can be sustained indefinitely without damage to the converter.

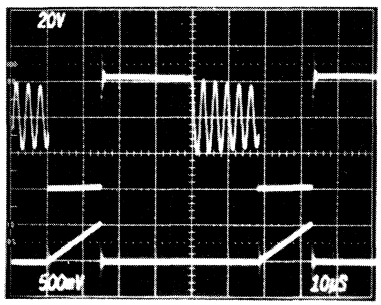
When the short circuit is removed from the converter output, the control loop forces the duty ratio to increase to its maximum value since the error amplifier output will be near the positive rail. The control loop has been made purposely slow to prevent it from being susceptible to noise when operating at very light loads. This causes the recovery time from the short circuit condition to be long, and the output and auxiliary winding voltages become excessive unless clamped by Zener diodes VR1, VR2, and VR3. As a final note, the recommended procedure for oscillator synchronization is to feed a positive going SYNC pulse through an R-C network to pin 8. The recommended values are 5 kΩ and 220 pF.



V_{DS} (20 V/div) U1 pin 3

V_{SENSE} (0.1 V/div) U1 pin 4

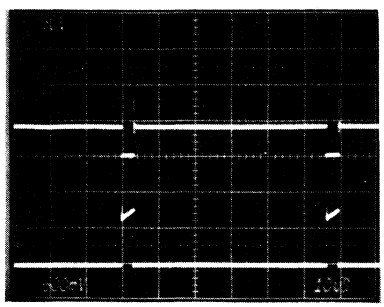
Figure 3. MOSFET drain voltage and current waveforms for emergency-power operation



V_{DS} (20 V/div) U1 pin 3

V_{SENSE} (0.5 V/div) U1 pin 4

Figure 4. MOSFET drain voltage and current waveforms for full-load operation



V_{DS} (50 V/div) U1 pin 3

V_{SENSE} (0.5 V/div) u1 pin 4

Figure 5. MOSFET drain voltage and current waveforms for the output short circuit condition.

A summary of the dc/dc converter specifications is given in Table II for reference.

Table II

Input Voltage Range	Max. Load Min. Load	22 - 42 V 30 - 42 V
Output Load Current	Min. Load Max. Load	3 mA @ +5 V 0 mA @ -5 V 100 mA @ +5 V 30 mA @ -5 V
Regulation	±7% worst case	(±5% typical)
Output Ripple	100 mV Max. at full load (60 mV typical) at full load	
Conversion Efficiency	Max. Load 80% min (85% typical) Min. Load 55% min.(67% typical)	
Isolation Voltage	1750 V_{RMS} primary to secondary	

Circuit Analysis

It is instructive to calculate the converter losses for the restricted power condition in the inactive state to gain some insight as to the relative importance of the design parameters. In other words, how important are MOSFET $r_{DS(ON)}$ and output capacitance, leakage inductance, switching frequency, etc. to the converter efficiency? The exercise of "counting the milliwatts" was performed and is included in Appendix A for reference. The summary appears in Table III. Power losses are sorted in two different ways: 1) according to whether or not they should be expected to vary with the choice of operating frequency (dynamic vs. static losses) and 2) according to whether or not they vary with the output load current. The power consumption of the Si9105 is divided into two components: one which is frequency dependent (logic gates plus oscillator plus MOSFET drive) and the other which is constant (voltage reference plus analog circuits).

Several interesting conclusions can be drawn from Table III. An observation which may well have been expected is that most of the losses are not load dependent at the 25 mW power level. But one may not have expected that the MOSFET conduction and sense resistor losses should be nearly negligible. These losses, together with the rectifier losses, totally dominate for the full load condition. A final observation is that MOSFET and transformer parasitic capacitances, which cause negligible losses at higher power levels, have significant effect at such low current levels.

Table III. Power Loss Calculations (Emergency Power-Down State)

Source of Loss	Dynamic Losses (freq. dep.)	Static Losses (not freq. dep.)	Load-Dependent Losses	No-load losses
MOSFET + R_{sense} (conduction)		0.09	0.09	
Feedback Voltage Divider Network		0.84		0.84
Rectifier Conduction		1.58	1.58	
-5 V Pre-Load		0.18		0.18
Si9105 Controller (REF Gen + Analog)		2.85		2.85
Si9105 Controller (Logic + OSC + Driver)	0.50			0.50
Turn-On (½ CV^2f_s)	1.08			1.08
TOTAL	**1.58 mW**	**5.54 mW**	**1.67 mW**	**5.45 mW**

7.12 mW 7.12 mW

Measured: P_{IN} = 22.92 mW, P_O = 15.25 mW, η = 66.6%, P_{loss} = 7.67 mW

As a final summary of the power converter efficiency, Figure 6 plots the measured efficiency as a function of output power. It should be noted that these efficiencies do not include losses in the input rectifier bridge to the emergency-designated terminal. The worst-case input current is given by Equation 5.

$$I_{IN(max)} = \frac{P_{IN(max)}}{V_{IN(min)}} = \frac{25\ mW}{32\ V} = 780\ \mu A \qquad (5)$$

Assuming two diode drops at 0.6 V each gives a power loss of

P_D = (1.2 V) (780 µA) = 940 µW.

If the worst case for the Si9105 power consumption is taken into account, then an additional 1.5-mW loss is possible. The 7.7-mW measured loss plus 1.0 mW for the rectifier bridge, 1.5 mW for the regulator IC, and 1.0 mW for other miscellaneous circuit losses gives a worst-case power dissipation of 11.2 mW. Output power is a minimum of 13.8 mW, and the minimum efficiency is 55%.

Conclusion

Worst case efficiency of 55% is a realizable goal for dc/dc converters in ISDN terminals which meet CCITT specifications. The Si9105 switchmode regulator is the first fully-integrated solution which has been demonstrated to provide the required efficiencies over the 13 mW to 650 mW output power range.

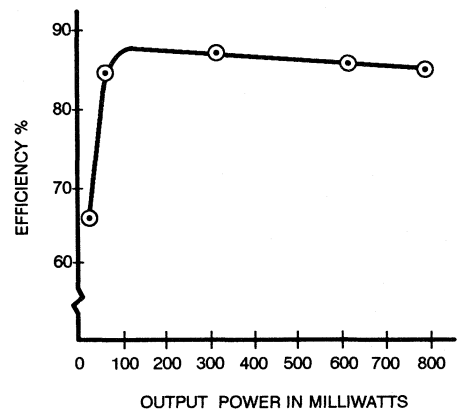


Figure 6. Measured Efficiency vs. Output Power

References

1) Rosenbaum, D. and Stolp, K., "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct 14-17, 1985, pp. 505-512.

2) "A One-Watt Flyback Converter Using the Si9100",Siliconix Application Note, AN87-1, March 1987.

9

APPENDIX A

Calculated Power Losses

1. MOSFET conduction losses –

RMS current is given by

$$I_{RMS} = I_{PK}\sqrt{\frac{D}{3}} = 27\text{ mA}\ \sqrt{\frac{0.046}{3}} = 3.34\text{ mA}$$

$$P_{COND} = I_{RMS}^2 \cdot r_{DS(ON)}$$
$$= (3.34\text{ mA})^2 \cdot 4\ \Omega = 45\ \mu W$$

2. Current sense resistor –

$$P_{SENSE} = (3.34\text{ mA})^2 \cdot 3.9\ \Omega = 44\ \mu W$$

3. Feedback divider resistor network –

$$P_{DIV} = \frac{V_{CC}^2}{R_5 + R_6} = \frac{(10\text{ V})^2}{71.5\text{ k}\Omega + 47.5\text{ k}\Omega} = 840\ \mu W$$

4. Rectifier conduction –
The inductance of the +5 V winding is

$$L_5 = L_P \left(\frac{N_3}{N_1}\right)^2 = 3.8\text{ mH}\ \left(\frac{1}{4.54}\right)^2 = 184\ \mu H$$

Peak secondary current is

$$I_S = \left(\frac{N_1}{N_3}\right) I_{PK} = \left(4.54\right)\left(27\text{ mA}\right) = 123\text{ mA}$$

The diode conduction time is

$$t_{cond} = \frac{\Delta I}{di/dt} = \frac{I_S}{V/L} = \frac{123\text{ mA}}{\left(\frac{5.5\text{ V}}{184\ \mu H}\right)} = 4.10\ \mu s$$

$$T_S = \frac{1}{f_s} = \frac{1}{18\text{ kHz}} = 55.5\ \mu s$$

The duty ratio for rectifier condition is

$$D_R = \frac{4.10\ \mu s}{55.5\ \mu s} = 0.074$$

Assuming a constant diode drop, V_F, of 0.35 V at this current level gives

$$P_{RECT} = \left(\frac{I_s}{2}\right)\left(V_F\right)\left(D_R\right)$$
$$= \left(\frac{123\text{ mA}}{2}\right)\left(0.35\text{ V}\right)\left(0.074\right) = 1.58\text{ mW}$$

5. Pre-load resistor on –5 V output –

$$P_{PL} = \frac{V_O^2}{R} = \frac{(-5.25)^2}{150\text{ K}} = 184\ \mu W$$

6. Turn-on losses –
$P_{ON} = ½\ C_{STRAY} V_{DS}^2 f_S$, where C_{STRAY} includes the transformer winding capacitance plus the MOSFET output capacitance.

$$C_{STRAY} = C_{DS} + C_{WIND}$$
$$\approx 35\text{ pF} + 40\text{ pF} = 75\text{ pF}$$
$$P_{ON} = ½\ (75\text{x}10^{-12})(40)^2(18\text{x}10^3) = 1.08\text{ mW}$$

7. Quiescent power for PWM IC –

Reference generator $(60\ \mu A)(10\text{ V}) = 0.6\text{ mW}$

Analog Circuits $(7.5\ \mu A)(30)(10\text{ V}) = 2.25\text{ mW}$

(30 internal current sources at 7.5 µA each)

Logic plus oscillator

$$\left(\frac{1.5\ \mu A}{\text{kHz}}\right)\left(18\text{ kHz}\right)\left(10\text{ V}\right) = 0.27\text{ mW}$$

MOSFET Driver –

$$P_{DRIV} = C_{GS} \cdot V_{GS}^2 \cdot f_S$$
$$= \left(125\text{ pF}\right)\left(10\text{ V}\right)^2\left(18\text{ kHz}\right) = 0.225\text{ mW}$$

Total quiescent power of Si9105 = 3.35 mW

Designing DC/DC Converters with the Si9110 Switchmode Controller

James Blanc

In distributed power systems and battery-powered equipment, the advantages of MOS over bipolar technology for pulse-width modulation (PWM) controllers are significant. First, by using a BiC/DMOS power IC process, a high-voltage DMOS transistor can be integrated with a CMOS PWM controller to serve as a pre-regulator stage. This reduces the number of external components by permitting the power controller IC to interface directly to the power bus.

The second advantage of MOS is speed. Bipolar PWM controllers can be made fast, but only with a significant increase in supply current. Logic gate delays of 5 ns are readily achievable using 5-μm CMOS, comparator propagation delays are in the 50- to 100-ns range, and the supply current is maintained *below 1 m*A.

How does speed translate into power supply performance? The answer is first in reliability and second in power density. If the delay time is long between the sensing of an overcurrent condition in the power switch and the turn-off of the switch, then the peak and RMS current values reach excessive levels and the switch fails. A well-designed power supply should tolerate a continuous short circuit on any output. To accomplish this with a slow controller IC, extra protection circuitry or an oversized switching transistor and heatsink are required. But that costs money.

Power supply density (often expressed as output power in watts divided by volume in cubic inches) has steadily been increasing over the past 5 to 10 years. By increasing the switching frequency, the size of magnetics and filter capacitors has been reduced, allowing smaller and less expensive power supplies to be built. To increase the switching frequency to the 100- to 500-kHz range and still achieve high reliability requires that the current limit delay time be kept under approximately 100 ns.

The first BiC/DMOS switchmode controller IC to meet these requirements is the Si9110. Its 500-kHz rating for maximum switching frequency is fully usable, thanks to the high-speed current limit comparator and the efficient output driver stage, which essentially eliminates the shoot-through current found in bipolar totem-pole circuits. The DMOS transistor in the input pre-regulator has a breakdown voltage rating of 120 V, which provides ample headroom for operation from typical bus voltages in distributed power systems (where 12, 24, 48, and 60 V are frequently encountered).

The appeal of such distributed power processing systems is in their flexibility and reliability. By bussing power at a higher voltage, smaller conductors can be used, as well as fewer connector pins to get the power to where it is needed – on the circuit card. An on-card power supply can then provide the voltages needed in that part of the system. The power bus voltage is usually chosen to be low enough to eliminate the need for safety agency approvals, and a battery can be connected through a diode to the power bus to provide emergency back-up. The distributed power approach is employed in telecom systems, large minicomputers, and in other applications where reliability is a primary concern.

To illustrate some of the performance capabilities of this BiC/DMOS switchmode controller IC, a 15-W forward converter design is presented. The converter provides +5-V and ±12-V outputs from a 9- to 36-V input range. This permits the power supply to operate from 12-V or 24-V batteries, or from a 28-V aircraft power source. Before describing the forward converter example, it is instructive to review the operation of each of the Si9110 switchmode controller's functional blocks.

FUNCTIONAL DESCRIPTION

Pre-regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (120-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{IN} to turn the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

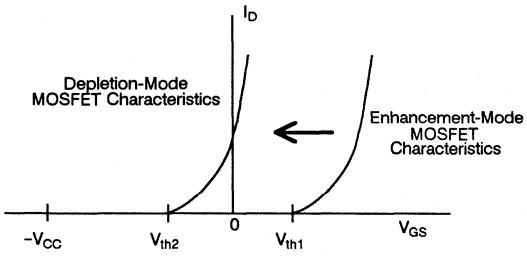


Figure 1. Depletion-mode MOSFET Characteristics

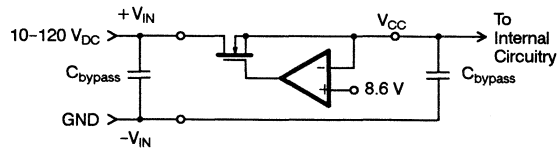


Figure 2. Pre-regulator/Start-up Circuit

In some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 6 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{IN}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off.

Oscillator

A ring of inverters and internal MOS capacitors forms the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$, the CMOS logic threshold, inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter. It also causes the "bump" at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_s.

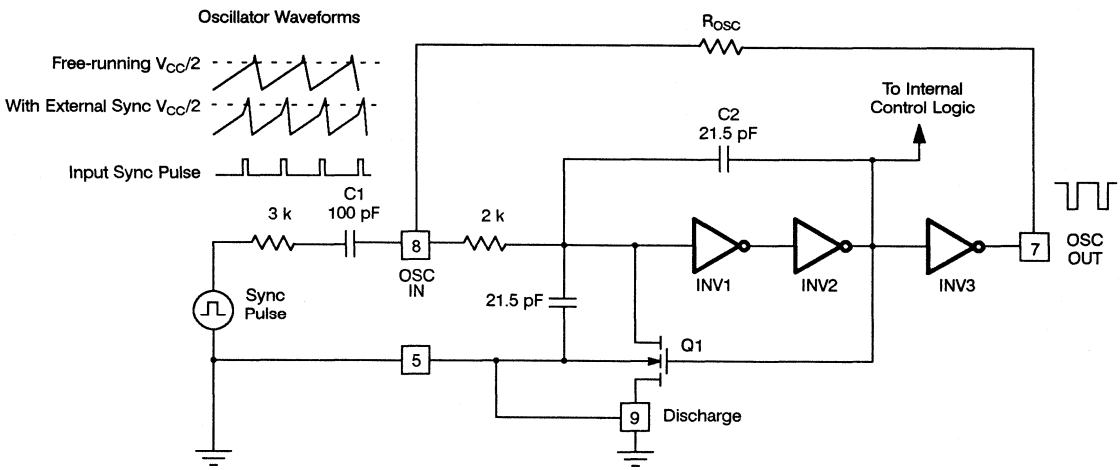


Figure 3. Si9110 Oscillator Circuit Operation

Error Amplifier

The bias resistor connected from pin 1 (BIAS) to pin 5 ($-V_{IN}$) programs the current sources in the analog portion of the current-mode controller – including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9110 data sheet guarantees the performance of these functions at one value of bias current – 15 μA. It is possible to change the performance characteristics of these functions by changing the bias current, and Appendix A explains how this is accomplished.

The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2 MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

The error amplifier is unity gain stable with a typical bandwidth of 1 MHz and 60° phase margin. Bias current values of from 5 μA to 50 μA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{BIAS} is increased above 15 μA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

Voltage Reference

A buried zener with merged temperature compensating diode (patent pending) is used to achieve stability of 0.25 mV/°C.

The Si9110 voltage reference is trimmed to 4 V plus or minus 1% with a bias current of 15 μA . This voltage varies by about 1% as I_{BIAS} is varied from 5 to 50 μA. If 1% reference accuracy must be guaranteed, I_{BIAS} should be set at 15 μA.

For circuits employing an external reference on the secondary side, such as those used with optically coupled feedback, the Si9111 is an economical approach. Its voltage reference provides a dc bias point at the input to the error amplifier where its 10% accuracy is more than sufficient. The reference accuracy is the only difference between the Si9110 and Si9111.

Comparators

The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching. The total current-limit delay to output versus I_{BIAS} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{BIAS} = 5 μA, but decreases to 50 ns for I_{BIAS} = 30 μA. As operating frequency is increased, I_{BIAS} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{BIAS} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{BIAS}. The current sense resistor and I_{BIAS} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.

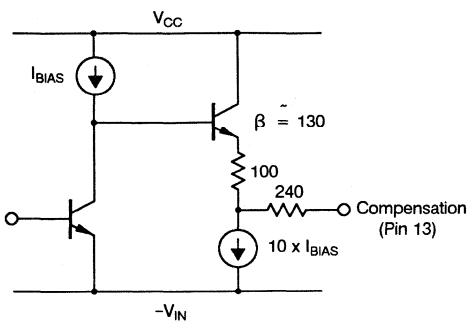


Figure 4. Error Amplifier Output Stage

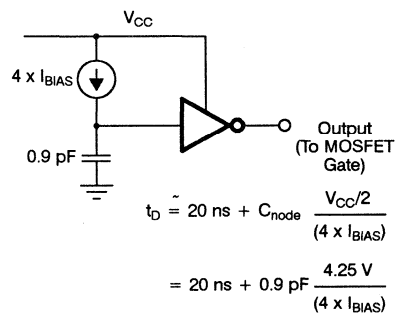


Figure 5. Current-limit Comparator Delay (Equivalent Circuit Model)

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(ON)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

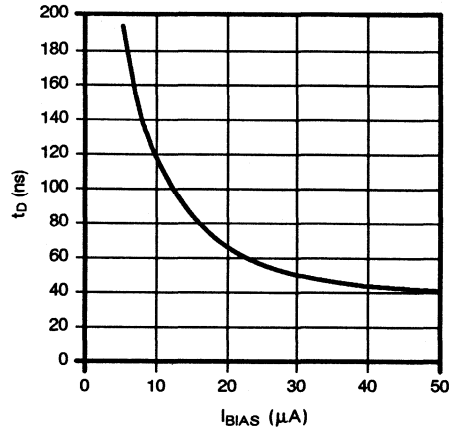
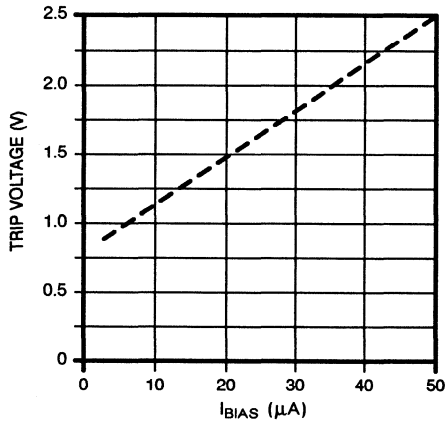


Figure 6. Current-limit Comparator Delay vs. Bias Current



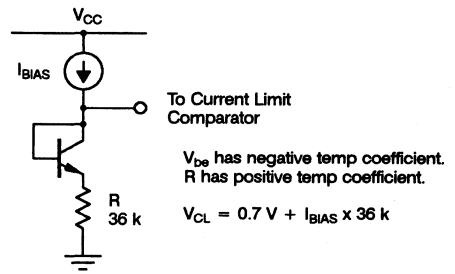


Figure 7. Current-Limit Trip Voltage vs. Programmed Bias Current

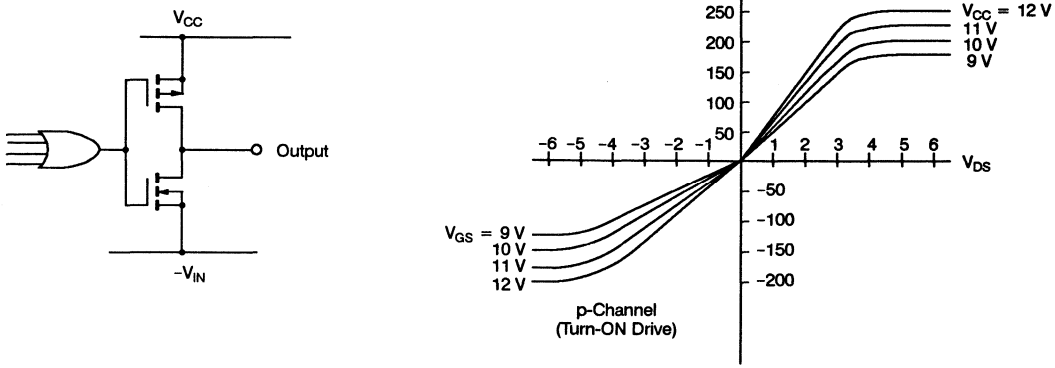


Figure 8. Output Drive Characteristics

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC} \quad (1)$$

where

$Q_g \equiv$ MOSFET gate charge
$f_s \equiv$ switching frequency
$V_{CC} \equiv$ supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the SHUTDOWN and RESET inputs have internal current-source pull-ups (equal to I_{BIAS}), so they can be left open when unused. As long as the SHUTDOWN input is held low, the output is OFF. If the RESET input is hard wired to $-V_{IN}$ (through a normally closed reset button if desired), any LOW input to SHUTDOWN will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 18 mA. The output is disabled until V_{CC} reaches the UV lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive (see Appendix B). When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by $Q_g \times f_s$, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.5 V). If too much current is drawn from V_{CC}, for instance to supply other circuitry, it may be possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle.

FORWARD CONVERTER

Specifications

Input Voltage ..... 9 to 36 V

Output Voltages

	Minimum Load (mA)	Maximum Load (A)	Regulation (%)	Ripple (mV_{p-p})
+5	50	1.5	2	150
+12	50	0.310	5	40
-12	20	0.310	5	40

Efficiency
V_{IN} = 12 V, Full Load . 78% typical, 76% minimum
V_{IN} = 12 V, ½ Load .. 82% typical, 80% minimum

Switching Frequency ..... 100 kHz

Circuit Description

The forward converter schematic is shown in Figure 9, and a block diagram of the Si9110/Si9111 controller IC appears in Figure 10 for easy reference. The circuit employs a TL431C voltage reference/amplifier to drive the LED of the opto-isolator, U3. This maintains galvanic isolation between input and output voltages. Since a reference is needed on the secondary side, external to the PWM controller IC, it is not necessary to have a precision reference on the primary side. The voltage reference of the Si9111 is specified at 4 V ±10%, which is accurate enough to establish a dc bias point for the collector current of U3. If galvanic isolation is not required, then the feedback circuitry in the box can be replaced by a voltage divider network, and the input and output grounds must be tied together. In this configuration, the reference accuracy of the PWM controller IC limits the accuracy of the output voltages, and the Si9110 with its 1% reference should be specified. The two ICs are identical in all other respects.

The SMP25N06 switching transistor (Q1) is a 25-A, 60-V MOSFET in a T0-220 package. The breadboard was operated without a heatsink on Q1, even with the power supply output shorted. Three secondaries on the transformer, T1, provide isolated voltages of +5 V and ±12 V. The output inductors are wound on a common core. This reduces the size and cost compared to separate output chokes, as well as improves the response to dynamic loads. The same core size is used for the transformer and the output inductor, the only difference being the air gap required by the inductor to sustain a dc flux. The transformer does not require a gap since the winding, N2, resets the core flux to zero during the "off" time of Q1.

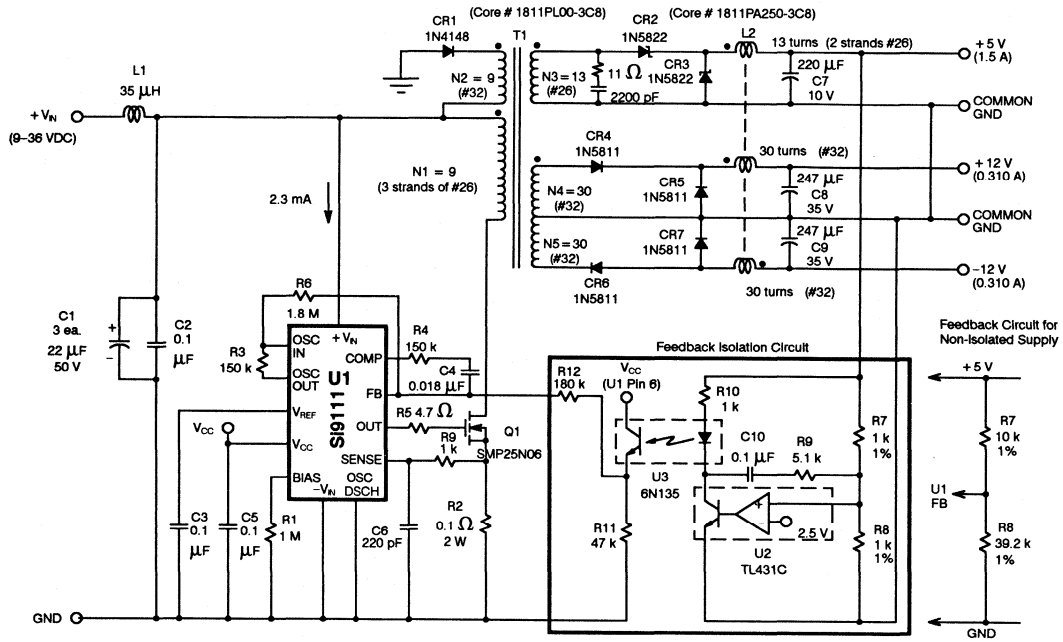


Figure 9. Multiple Output Forward Converter

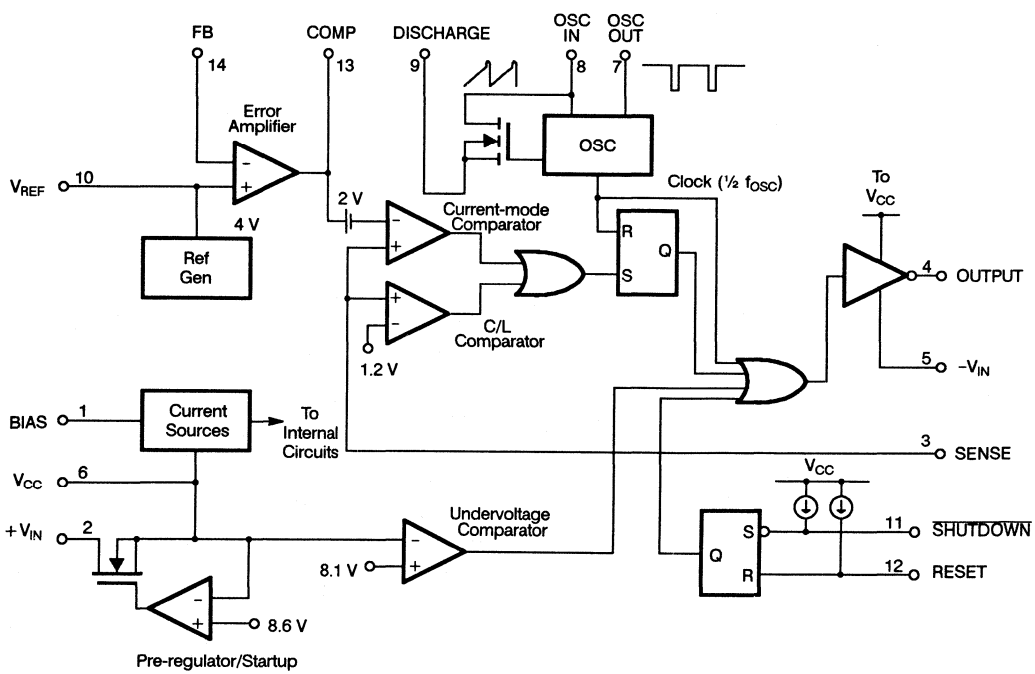


Figure 10. Si9110/Si9111 Block Diagram

Forward Converter Principle

The operating principle of forward converters is illustrated in Figure 11. When the switch, Q1, is on, the input voltage is applied across the primary winding, N_P. If, for example, the input voltage minus the voltage drop across Q1 and R2 is equal to 9 V, then 1 V per turn is applied across the primary. Since the same magnetic flux links all of the windings, the volts/turn is constant by Faraday's Law [$V = -N(d\phi/dt)$].

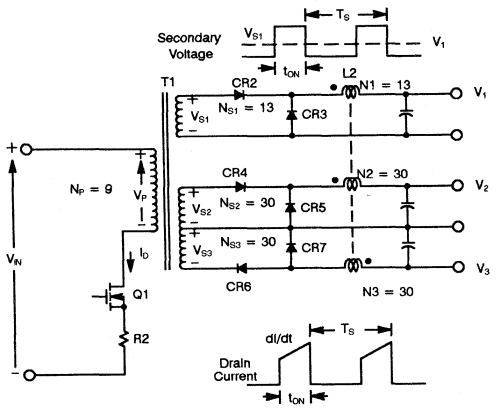


Figure 11. Forward Converter Operating Principle

Therefore, V_{S1} equals 13 V, and V_{S2} and V_{S3} equal 30 V. The LC filter has a cut-off frequency well below the switching frequency, so that the average value of the pulsed secondary voltage appears at the output. For V_1 to equal 5 V, the duty ratio, neglecting diode drops, is given by

$$D = \frac{V_1}{V_{S1}} = \frac{5\ V}{13\ V} = 0.385 \qquad (2)$$

The control loop will force the duty ratio to the value required to make the regulated output equal to 5 V. If the duty ratio equals 0.385, the secondary voltages V_2 and V_3 are given by

$$V_2 = V_3 = V_{S2} \times D = (30)\ (0.385) = 11.5\ V \qquad (3)$$

This is the ideal case. The diode drops cause the duty ratio to be higher, and V_2 and V_3 are very close to 12 V. (The measured value was 12.1 V.) When Q1 turns off, the free-wheeling diodes CR3, CR5, and CR7 carry the inductor currents. Again, if diode drops are neglected, each output voltage appears across its corresponding inductor winding. Since the volts per turn must be constant on each winding of L2, the number of turns must be proportional to the output voltage. Therefore, the number of turns and the inductance of each winding cannot be arbitrarily assigned as they can be for individual output chokes. The ratio of turns on L2 must be an integer multiple of the T1 secondary windings. In this case, the integer is 1. The amount of inductance is then determined by the core gap, specified as inductance per 1000 turns; 250 mH per 1000 turns was used, giving an inductance for the 5-V inductor as determined from

$$L_{5V} = 250\ mH \left(\frac{13}{1000}\right)^2 = 42\ \mu H \qquad (4)$$

Therefore, the current slope during the "on" time of Q1 (referred to the primary side of T1) is given by

$$\frac{di}{dt} = \left(\frac{13}{9}\right)\left(\frac{13\ V - 5\ V}{42\ \mu H}\right) = 0.275\ A/\mu S \qquad (5)$$

This current ramp is sensed by R2 to give a voltage ramp input to pin 3 of the Si9111. The current-mode comparator changes states and turns the MOSFET switch off when this sense voltage exceeds the control voltage, V_C, from the output of the error amplifier. Thus, the peak inductor current is controlled on a cycle-by-cycle basis. The same current sense signal is also compared to an internally-generated reference of 1.2 V by the current-limit comparator. This comparator is made four times faster than the current-mode comparator to minimize the delay time required to turn the MOSFET off when an overcurrent condition exists: Such dual-threshold current sensing enables power supply designs that can tolerate shorted outputs for an indefinite period. If the short is removed, then the converter returns to normal operation.

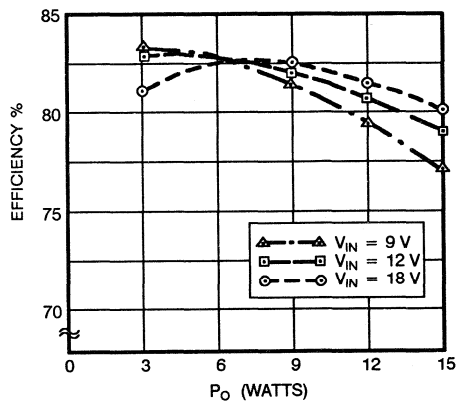


Figure 12. Percent Efficiency vs. Load Current

Measured Circuit Performance

Figure 12 shows how the power supply efficiency varies with load. Under the low-line condition (V_{IN} = 9 V), the full load efficiency is 77%. At higher input voltages, the conduction losses in the MOSFET and sense resistor are reduced, permitting full-load efficiency to exceed 80%. High efficiency at light loads is permitted by the CMOS controller's low supply current. At V_{IN} = 9 V, only 2.3 mA • 9 V = 20.7 mW are required by the Si9111.

The circuit operation at V_{IN} = 18 V with a 80% load is illustrated by the waveforms in Figure 13. The control voltage out of pin 13 is ac-coupled and shown above the current sense voltage. The downward slope of V_C is due to the slope compensation resistor connected between pin 8 and pin 14. Slope compensation is explained below in the section on loop analysis and in References 1 and 2.

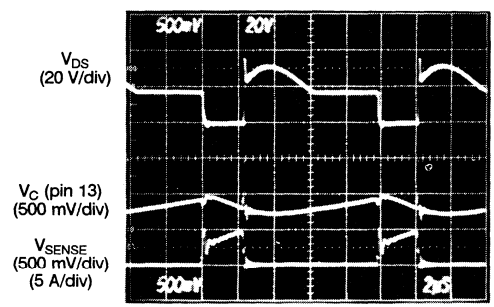
When the +5-V output is shorted to ground, the waveforms appear as in Figure 14. The error amplifier output, V_C, goes to the positive rail, so the current-mode comparator would allow the duty ratio to increase to 50%. However, the faster current-limit comparator trips at about 9 A, and the duty ratio is limited to less than 10%.

CONTROL LOOP ANALYSIS

Current-Mode Control

Current-mode control of switching power converters offers several advantages over voltage-mode control. The reliability improvement offered by fast cycle-by-cycle current limiting was discussed above. A second major advantage of current programming is improved dynamic response of the regulator loop while at the same time requiring simpler error amplifier compensation.

The basic objective of current-mode control is to make the power stage behave as a voltage-to-current converter (transconductance amplifier), as shown in Figure 15. To regulate the output voltage, a feedback loop is employed. The control voltage, V_C, is generated by an error amplifier which compares the output voltage to a precision reference, just as in voltage-mode control.



Loads: 1.2 A @ +5 V
0.25 A @ ± 12 V
V_{IN} = 18 V

Figure 13. Forward Converter Waveforms

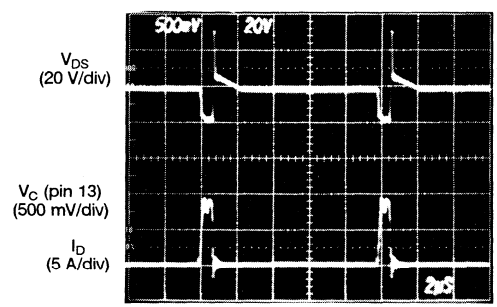


Figure 14. Forward Converter Waveforms with +5 V Output Shorted to GND (V_{IN} = 18 V)

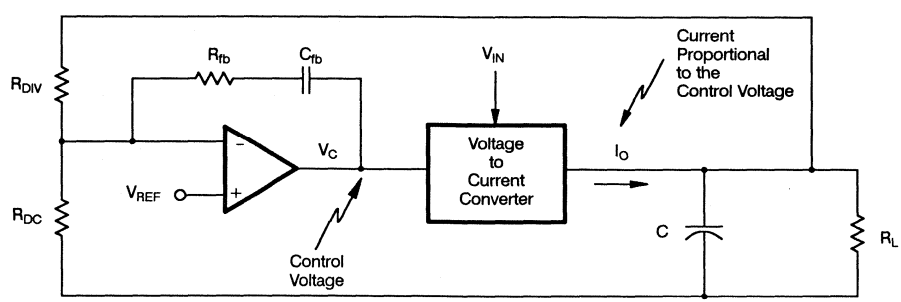


Figure 15. Power Converter with Current-mode Control

There are several methods for implementing the transconductance power amplifier function -- all of them employ an inner current feedback control loop. The most common method uses a constant frequency clock and peak current sensing, as shown in Figure 16. A clock pulse initiates turn-on of the MOSFET switch, and current ramps up in the output inductor. This current, reflected through the transformer turns ratio, is sensed by the resistor in the MOSFET source to produce a voltage analog of the inductor current. When the voltage ramp reaches the control voltage, V_C, the current-mode comparator sets the latch and turns off the switch. In this way the inner current control loop programs the inductor current in proportion to the control voltage.

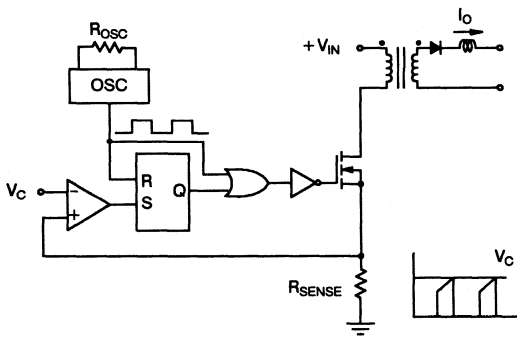


Figure 16. Voltage-to-Current Converter

To achieve the same loop bandwidth as a current-programmed power converter, a voltage-mode PWM converter requires an error amplifier with compensation as shown in Figure 17a. Current-mode control requires fewer compensation components, as shown in Figure 17b, and the error amplifier has a simpler transfer function. The simplified compensation is due to the elimination of the double pole of the output LC filter, which must be compensated by the double zero at f_1. If the inner current-programmed loop were perfect, then the inductor would behave as a controlled current source, and the power stage would be a single-pole system. This doesn't happen. What does occur is a splitting of the two poles. One is shifted down in frequency to approximately $f_{p1} = \frac{1}{2\pi R_L C}$, which is the dominant low-frequency pole. The second pole in the voltage regulator loop occurs at the unity gain crossover frequency, $\omega_C/2\pi$, of the inner current-control loop. The inner current-control loop has less gain than the voltage loop but has more bandwidth.[1] The wide bandwidth of the current loop enables the power converter to respond more rapidly to step changes in load current, even if the small-signal loop bandwidth is the same. It must be realized that step load changes are large signal perturbations between two different small-signal operating points. With inductor current as a controlled parameter, the wideband current loop changes more rapidly between two operating points of load current. The measured response to a step change in load is given in Figure 18. The switch current and output voltage recover to steady-state within about 50 µs, or five switching cycles. Voltage-mode control generally yields a response which is slower by a factor of 5 to 10.

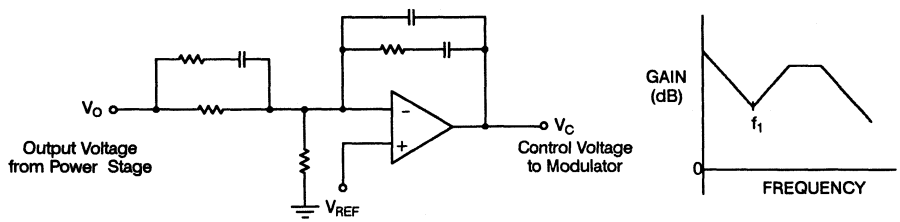


Figure 17a. Error Amplifier Compensation for Maximum Bandwidth Using Voltage-Mode Control

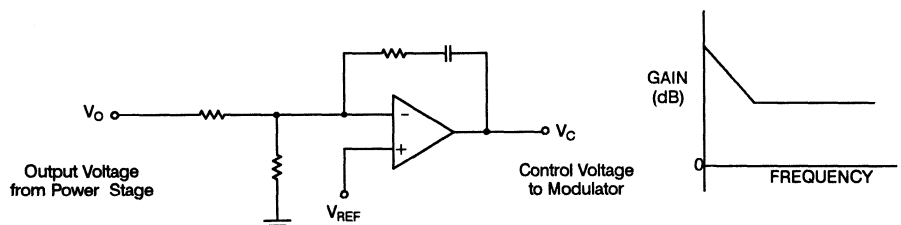


Figure 17b. Error Amplifier Compensation for Maximum Bandwidth Using Current-Mode Control

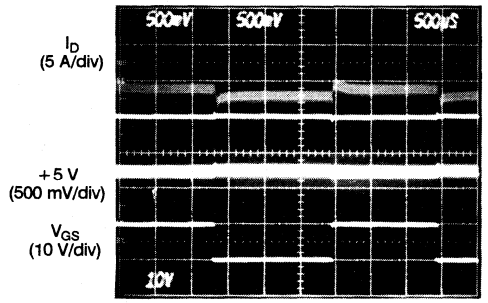


Figure 18. Step Load Response

Small-Signal Analysis

A very concise presentation of small-signal analysis of current-mode control loops can be found in Reference 1. In that paper, the Y-parameter model, shown here in Figure 19, is developed for current-programmed power stages since Y-parameters give an output current for a unit of control voltage input. The inner current loop is demonstrated to be stable, as long as slope compensation is employed for D > 0.5, and therefore, the current loop can be absorbed into the new power stage model. This has the advantage of allowing us to analyze the stability of only one (voltage) control loop.

The derivations will not be presented here, but the resulting control-to-output voltage transfer function of the buck regulator is shown in Figure 20. R_{22} is the low frequency value of the inverse of the output admittance, Y_{22}. It is a measure of how effectively current programming makes the power stage behave as a current source and, consequently, depends heavily upon the gain of the inner current loop. More inductance yields higher current loop gain and larger R_{22}. Smaller R_{22} causes the low frequency gain to be diminished, since R_{22} appears in parallel with the load, R_L. R_{22} also decreases the low-frequency pole by the same factor. In this case, R_{2C} is simply the sense resistance value of 0.1 Ω. For buck-derived converters, it is the ratio of voltage at the current-mode comparator input to inductor current, and it accounts for current amplifier gains and current transformer ratios. The second pole at $\omega_C/2\pi$ depends upon the switching frequency, the amount of slope compensation, and the duty ratio at the dc operating point (remember that this is a small-signal analysis of variations around a dc operating point); it does not depend on the load current.

An easy way to work through the calculations is to form a table, as shown in Figure 21. The voltage-control loop bandwidth, f_{vc}, and phase margin, ϕ_m, are calculated at full load for three different input voltages. The same symbols are used as in reference 1, with the exceptions that the current ramp slopes m_1, m_2, and m_3 are referenced to the current-mode comparator input. The result is the same as long as the current scale factor, R_f, is taken into account.

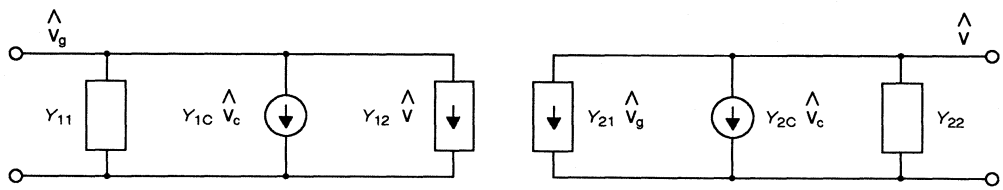


Figure 19. Y-parameter Model for Current-mode Regulators

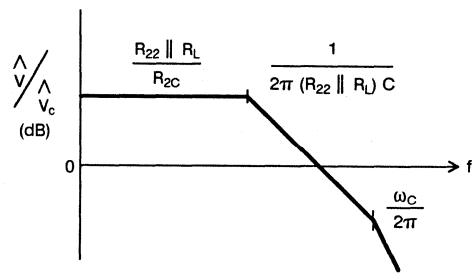


Figure 20. Small-signal Control to Output Transfer Function of Current-programmed Buck Regulators

V_{IN}	D'	M_1 (V/μs)	n	R_{2C}	R_{22}	f_p* (Hz)	$A_{cm} = \frac{R_{22} \parallel R_L}{R_{2C}}$	ω_C (krad/s)	f_{VC} (kHz))	ϕ_m (deg)
9	0.59	0.044	1.6	0.1	7.6	141	7.5 (17.5dB)	2 π (33.7)	15.76	52
18	0.78	0.089	1.3	0.1	5.1	147	7.2 (17dB)	2 π (31.4)	15.77	50
32	0.88	0.158	1.16	0.1	4.5	152	7.0 (17dB)	2 π (31.2)	15.85	50

$$*f_p = \frac{1}{2\pi (R_{22} \parallel R_L) C}$$

Figure 21. 15-W Forward-converter Stability Analysis

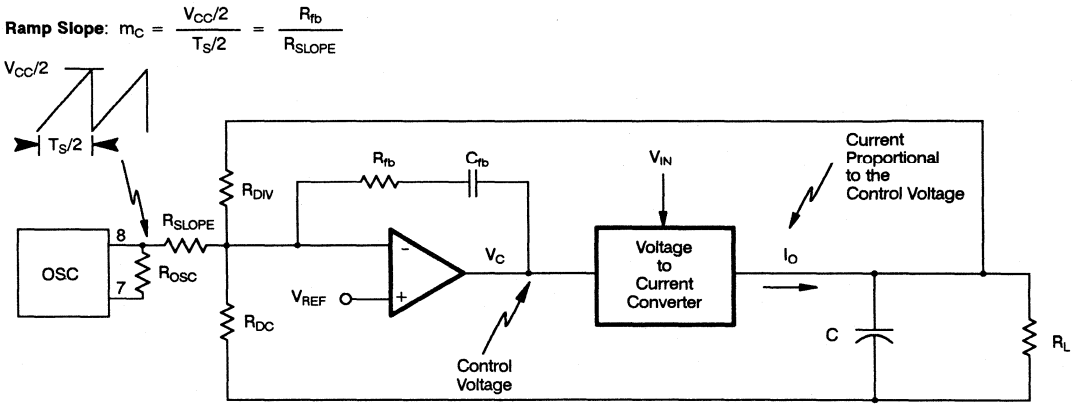


Figure 22. Implementation of Slope Compensation Using the Si9110.

The forward converter is a transformer-isolated derivative of a buck regulator. Therefore, the Y-parameter model for the buck regulator applies here, but the R, L, and C values used must be reflected through the transformer turns ratios. The resulting circuit parameters are

$$R = \frac{5\text{ V}}{1.5\text{ A}}\left(\frac{9}{13}\right)^2 \left\| \frac{12\text{ V}}{0.31\text{ A}}\left(\frac{9}{30}\right)^2 \right\| \frac{12\text{ V}}{0.31\text{ A}}\left(\frac{9}{30}\right)^2$$

$$= 1.6\Omega \parallel 3.5\,\Omega \parallel 3.5\,\Omega = 0.83\,\Omega \qquad (6)$$

$$L = A_L\left(\frac{N_2}{1000}\right)^2\left(\frac{N_1}{N_2}\right)^2 = 20.3\,\mu\text{H} \qquad (7)$$

$$C = 220\,\mu\text{F}\left(\frac{13}{9}\right)^2 + (47\,\mu\text{F} + 47\,\mu\text{F})\left(\frac{30}{9}\right)^2 \qquad (8)$$

$$= 1500\,\mu\text{F}$$

Slope compensation is achieved by feeding the oscillator ramp voltage into the inverting input of the error amplifier, as shown in Figure 22.

The amount of slope compensation is given by

$$m_C = \frac{V_{CC}}{T_S} \times \frac{R_{fb}}{R_{SLOPE}} = \frac{8.5\text{ V}}{10\,\mu\text{s}} \times \frac{150\text{ k}\Omega}{1.8\text{ M}\Omega}$$

$$= 0.071\text{ V}/\mu\text{s} \qquad (9)$$

This calculation does not take into account the effect of ripple feedback upon slope compensation. For a buck regulator, during the "on" time of the switch, the output ripple voltage is ramping upward due to capacitor ESR. This ramp voltage is amplified and inverted by the error amplifier to provide additional slope compensation. If lower ESR capacitors are used, this effect is diminished. For film or ceramic filter capacitors, the ripple is also phase shifted, since ripple voltage is determined more by C than by ESR.

9

The slope compensation parameter, n, is given by

$$n = 1 + \frac{2\,m_C}{m_1} \qquad (10)$$

where m_1 is the current ramp slope (times the sense resistance) during t_{ON}, which is calculated from

$$m_1 = \frac{V_{IN}}{L} \times R_f = \frac{V_{IN}}{20.3\ \mu H} \times 0.1\ \Omega \qquad (11)$$

For a buck converter, R_{2C} is simply equal to R_f, the sense resistance.

The conduction parameter K is a measure of how far into continuous conduction the converter is operating. At full load

$$K = \frac{2L}{RT_S} = \frac{2\,(20.3\ \mu H)}{(0.83)\ (10\ \mu s)} = 4.86 \qquad (12)$$

This converter operates heavily into the continuous conduction mode and has a fairly high current-loop gain.

The output resistance parameter is

$$R_{22} = \frac{KR}{nD' - D} \qquad (13)$$

which varies with both input voltage and load. The frequency, f_P, of the power stage low-frequency pole is

$$f_P = \frac{1}{2\,\pi\,(R_{22} \parallel R_L)\,C} \qquad (14)$$

The low-frequency gain of the power stage is

$$A_{CM} = (R_{22} \parallel R_L)/R_{2C}$$

and the high-frequency pole is given by $\omega_C = \omega_S/\pi n D'$.

Once the gain of the power stage has been determined and plotted, as shown in Figure 23, the objective is to establish values for the error amplifier compensation to provide good loop bandwidth and phase margin. Some typical "rule-of-thumb" numbers are to use a bandwidth of one sixth to one fifth of the switching frequency and a phase margin of 45° to 60°. A series RC network in the feedback of the error amp gives a pole at the origin and a zero at $f_Z = \frac{1}{2}\,\pi\,R_{fb}C_{fb}$.

The error amplifier gain remains constant at

$$A_{1M} = \frac{R_{fb}}{R_{div}} = \frac{R_4}{R_7} = \frac{150\ k\Omega}{10\ k\Omega} = 15\ (\text{or } 23.5\ dB) \qquad (15)$$

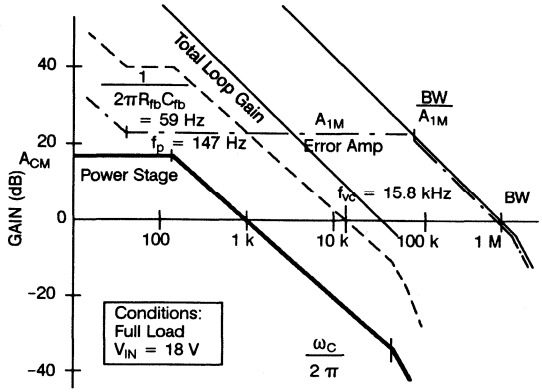


Figure 23. Bode Plot of Small-signal Loop Gain

between f_Z and the point where the open-loop gain of the error amplifier takes over. This occurs at $A_{OL1} = BW/A_{1M}$, where BW is the error amplifier bandwidth. The gain of the loop is decreased to unity below the poles at $\omega_C/2\pi$, and A_{OL1}, but each can contribute significant phase shift. The voltage loop crossover frequency is calculated from

$$f_{VC} = A_{CM} \times A_{1M} \times f_P \qquad (16)$$

The feedback divider resistor, R_7, was first arbitrarily chosen to be 10 kΩ. (This is for the non-isolated configuration. For analysis of the optical-isolator circuit, see Appendix C.) To achieve $f_{VC} \simeq f_S/6 = 16$ kHz, A_{1M} was calculated from Equation 15. This requires

$$R_{fb} = A_{1M} \times R_{div} = 15 \times 10\ k\Omega = 150\ k\Omega$$

A standard capacitance value is then chosen such that f_Z falls somewhat below f_P. $C_{fb} = 0.018\ \mu F$ places the zero, f_Z, at about 60 Hz.

The phase margin, ϕ_m, of the ideal current-mode converter is 90°. Phase lags due to poles at $\omega_C/2\pi$ and A_{OL1} diminish the phase margin according to

$$\phi_m \simeq 90° - \tan^{-1}\left(\frac{f_{VC}}{\omega_C/2\pi}\right) - \tan^{-1}\left(\frac{f_{VC}}{A_{OL1}}\right) \qquad (17)$$

A more accurate analysis should account for the zero of the capacitor ESR. The tantalum capacitors used here (type 550D from Sprague) will cause a zero at approximately 30 to 50 kHz. This will just about cancel the pole at $\omega_C/2\pi$, and increase the phase margin. Higher ESR will cause the extra zero to fall below f_{VC}, and the loop bandwidth will be increased somewhat.

MAGNETICS DESIGN

Transformer Core Selection

The core selection method used here employs the core geometry parameter, K_g, as proposed by McLyman.[3] Pot cores were chosen for both the transformer and the coupled inductor, but another design approach using toroids is recommended for applications requiring either the lower profile or the resilience to thermal shock that toroids provide.

Begin by calculating the output power of the transformer.

$$P_O = \Sigma (V_O + V_D) I_O \quad (18)$$

where

$V_O \equiv$ Output Voltage
$V_D \equiv$ Diode Drop
$I_O \equiv$ Output Current

$$P_O = (5\text{ V} + 0.5\text{ V})(1.5\text{ A}) + 2(12\text{ V} + 0.7\text{ V})(0.31\text{ A}) = 16.1\text{ W} \quad (19)$$

The apparent power, P_t, for a single-ended forward converter is

$$P_t = P_O (\sqrt{2}/\eta + \sqrt{2}) \quad (20)$$

where η transformer efficiency

$$P_t = (16.1)(\sqrt{2}/0.99 + \sqrt{2}) = 45.8\text{ VA} \quad (21)$$

The electrical conditions parameter, K_e, is given by

$$K_e = 0.145\, K_e^2 f^2 B_m^2 \times 10^{-4} \quad (23)$$

where

$K_f \equiv$ Waveform Factor ($\sqrt{2}$ for the forward converter)
$f \equiv$ Operating Frequency
$B_m \equiv$ Maximum Flux Density (0.15 tesla was chosen)

$$K_e = 0.145(\sqrt{2})^2(10^5)^2(0.15)^2 \times 10^{-4} = 6525 \quad (23)$$

Finally, the core geometry, K_g, is

$$K_g = \frac{P_t}{2 K_e \alpha} \quad (24)$$

where $\alpha \equiv$ percent regulation (use 1%)

$$K_g = \frac{45.8}{2\ (6525)\ (1)} = 3.5 \times 10^{-3}\text{ cm}^{-5} \quad (25)$$

This K_g calculation is based upon an assumed window utilization factor, K_u, of 40% or 0.4. This is difficult to achieve using small pot cores. Assuming a 25% window area, the core geometry is adjusted by

$$K_{g(new)} = (0.4/0.25)(3.5 \times 10^{-3}) = 5.6 \times 10^{-3}\text{ cm}^5 \quad (26)$$

The closest pot core is number 1811PL00 from Ferroxcube, for which $K_g = 6.0 \times 10^{-3}\text{ cm}^5$.

The toroidal cores which most nearly meet the transformer requirements are numbers T8-16-8 and T10-20-5 from TDK. Their K_g's are 0.007456 cm^5 and 0.007536 cm^5, respectively.

Transformer Winding Design (First Iteration)

Refer to Figure 11 for the nomenclature used here. The number of primary turns is calculated from Faraday's Law, which states that $V = -N(d\phi/dt)$.

$$\frac{V_p}{N_p} = A_C \frac{B_{max}}{t_{ON}} \quad (27)$$

$$N_p = \frac{V_p \times t_{ON}}{B_{max} \times A_C} \quad (28)$$

where

$A_C \equiv$ Cross-sectional Area of Core
$B_{max} \equiv$ Maximum Flux Density
$t_{ON} \equiv$ MOSFET On-time ($t_{ON} = D \times T_S$)

Design for $D_{max} = 0.475$ at $V_{IN} = 9$ V. V_p is calculated from

$$V_p = V_{IN} - I_D \times (r_{DS(ON)} + R_{SENSE}) \quad (29)$$

$$I_D \simeq \frac{(P_O/\eta)}{V_{IN} \times D} = \frac{(15\text{ W}/0.8)}{(9\text{ V})(0.475)} = 4.4\text{ A} \quad (30)$$

$$V_p = 9 - 4.4\,(0.08 + 0.10) = 8.2\text{ V} \quad (31)$$

and

$$N_p = \frac{(8.2\text{ V})(4.75\ \mu\text{s})}{(0.15\text{ T})(0.433 \times 10^{-4}\text{ m}^2)} = 6\text{ turns} \quad (32)$$

Calculate the secondary turns as follows:

$$V_O = [(V_p)(N_S/N_p) - V_D] \times D \quad (33)$$

If $V_O = V_1 = 5$ V, $D = 0.475$, and $V_p = 8.2$ V, then $N_{S1} = 8.07$. (Assume the diode drop is 0.5 V for Schottky diodes and 0.7 V for fast recovery P-N diodes.)

9

Eight turns is close enough. Now find the number of turns for the 12-V secondary. During the off-time, the output voltages appear across each coupled inductor winding, which must have the same turns ratios as the transformer secondaries. Therefore,

$$\frac{5\text{ V} + 0.5\text{ V}}{N_{S1}} = \frac{12\text{ V} + 0.7\text{ V}}{N_{S2}} \quad (34)$$

$N_{S1} = 8$ gives $N_{S2} = 18.5$ turns; 18 turns give $V_2 \simeq 11.65$ V, and 19 turns give $V_2 \simeq 12.35$ V. Another option is to set $N_{S1} = 16$ and $N_{S2} = 37$. This will more closely achieve the desired turns ratios, but copper losses will be greatly increased. Remember that if the number of turns is doubled, then the copper cross section must be halved. Resistance, and copper losses, increase by a factor of four. If it doesn't matter that the 12-V output is off a bit, then use $N_p = 6$, $N_{S1} = 8$, and $N_{S2} = 19$.

Inductor Core Selection

The power handling capability of the core is independent of the number of windings used. The simplest approach is to refer all outputs to the 5-V winding and assume that

$$I_O = P_O/V_O = 15\text{ W}/5\text{ V} = 3\text{ A} \quad (35)$$

To operate well into continuous conduction choose $K = 2L/RT_S \geq 4$.

Therefore, $L \geq (4/2)(5\text{ V}/3\text{ A})10^{-5} = 33\ \mu\text{H}$.

This is a ball park number; 25 μH is acceptable, and so is 50 μH. However, if L is larger, a larger core is required for the same core losses.

The peak inductor current, at maximum load, is

$$I = I_{O(MAX)} + \frac{\Delta I}{2} \quad (36)$$

ΔI is approximately given by

$$\frac{V_1 + V_D}{L_{S1}} = \frac{\Delta I}{t_{OFF}} \quad (37)$$

and the maximum ΔI occurs at maximum V_{IN} where $D \simeq 0.11$, $t_{OFF} = (1 - D)10\ \mu\text{s} = 8.9\ \mu\text{s}$.

$$\frac{5\text{ V} + 0.5\text{ V}}{33\ \mu\text{H}} = \frac{\Delta I}{8.9\ \mu\text{s}} \quad (38)$$

The inductor energy storage requirement is

$$E = \tfrac{1}{2}(LI^2) = \tfrac{1}{2}(33\ \mu\text{H})(3.75)^2 = 232\ \mu\text{J} \quad (40)$$

The electrical conditions are

$$K_e = 0.145\,(P_O)\,(B_m)^2\,10^{-4} = 0.145\,(15)\,(0.3)^2\,10^{-4} = 19.6 \times 10^{-6} \quad (41)$$

The core geometry requirement is

$$K_g = \frac{(E)^2}{K_e \alpha} = \frac{(232\ \mu\text{J})^2}{(19.6 \times 10^{-6})\,(1)} = 0.00275\text{ cm}^2 \quad (42)$$

for 1% regulation. Adjust this for a 25% window utilization, and you get

$$K_g = \frac{0.4}{0.25}\,(0.00275) = 4.4 \times 10^{-3}\text{ cm}^5 \quad (43)$$

We can use an 1811 pot core with a standard A_L value (160, 250, or 400 mH/10^3). For a toroid, use a number 55206 molypermalloy powder core, for which $K_g = 0.007274$ cm^5. The pot core was chosen here.

Inductor Winding Design

The transformer design was left with $N_{S1} = 8$ and $N_{S2} = 19$, which causes the 12-V output to be about 12.35 V. If $A_L = 400$ mH/1000 turns is used,

$$L_{S1} = (8/1000)^2\,(0.4) = 25.6\ \mu\text{H} \quad (44)$$

This gives

$$K = \frac{2L}{RT_S} = \frac{2\,(25.6\ \mu\text{H})}{(1.67)\,(10^{-5})} = 3.1 \quad (45)$$

which is still well into continuous conduction ($K_{crit} = D' = 1 - D$ for buck converters).

It could be done this way, but to make the 12-V output come out closer to 12 V, try some other turns ratios. $N_{S1} = 13$ and $N_{S2} = 30$ gives:

$$V_2 = (5.5/13)30 - 0.7 = 11.99\text{ V} \quad (46)$$

$A_L = 250$ mH/1000 turns gives

$$L_{S1} = (13/1000)^2\,(0.25) = 42\ \mu\text{H} \quad (47)$$

The maximum flux density is found from

$$L = \frac{\lambda}{I} = \frac{N\Phi}{I} = \frac{NB_m A_C}{I} \quad (48)$$

$$B_m = \frac{LI}{NA_C} = \frac{(42\ \mu\text{H})\,(3.75\text{ A})}{(13)\,(0.433 \times 10^{-4})} = 0.28\text{ T} \quad (49)$$

Saturation occurs above 0.3 T = 3000 gauss, so this flux level is acceptable. Apportion the window area according to the output power of each winding. Total copper area is 0.25 W_A, where W_A = 0.285 cm^5 is the total window area. The copper cross section for the 5-V winding is

$$A_{CU} = \frac{(0.25)\ (0.285\ cm^2)}{30\ \text{turns}} \times \frac{(5\ V)\ (1.5\ A)}{15\ W} \qquad (50)$$

$$= 2.74 \times 10^{-3}\ cm^2$$

Use two strands of AWG26 magnet wire, for which the copper area is

$$A_W = (2)\ (1.28 \times 10^{-3}\ cm^2) = (2.56 \times 10^{-3}\ cm^2) \qquad (51)$$

for the 12-V winding,

$$A_{CU} = \frac{(0.25)\ (0.285\ cm^2)}{30\ \text{turns}} \times \frac{(12\ V)\ (0.31\ A)}{15\ W} \qquad (52)$$

$$= 0.59 \times 10^{-3}\ cm^2$$

Use one strand of AWG30, for which A_W = 0.507 x 10^{-3} cm^2.

Transformer Winding Design (Revisited)

As shown in the above analysis, the transformer and inductor designs are interdependent when coupled inductors are used. Calculations are made based upon some reasonable assumptions, and the results may not give the desired outcome (such as a fractional turn or a saturated core). Then choices must be made which are consistent with the requirements of the end application. The choice made here was to set the output voltages as close as possible to 5 and ±12 V.

The transformer secondary turns are N_{S1} = 13 and N_{S2} = 30. The primary turns are found from

$$V_S = V_O/D + V_D = V_p\ (N_S/N_p) \qquad (53)$$

$$V_S = \frac{5\ V}{0.475} + 0.5 = 11\ V = 8.2\ V\left(\frac{13}{N_p}\right) \qquad (54)$$

$$N_p = 9.67\ \text{turns}$$

Set N_p = 9 turns so that the converter will continue to regulate down to V_{IN} = 9 V. Again, apportioning the copper according to power level (and equally split between primary and secondary) gives the following winding configuration.

Winding	Turns	Wire Size
Primary	9	3 Strands AWG26
RESET	9	1 Strand AWG32
+ 5 V	13	1 Strand AWG26
+12 V	30	1 Strand AWG32
-12 V	30	1 Strand AWG32

The primary and RESET windings were wound together (multifilar) over the bobbin, followed by the 5-V output. The ±12-V windings were wound bifilar over the 5-V winding.

Prototyping Hints

A schematic and a parts list do not provide sufficient information to enable a CAD operator to lay out a switching power supply. Parasitic inductances and capacitances, which do not appear on the schematic, can cause major differences in performance. The number of layout iterations can be reduced (down to one with experience) if the following guidelines are followed.

1) Use a ground plane. However, do not assume that the ground plane impedance is zero so that you can ignore the need for good component placement. Every component cannot be placed near every other component. Know which components should be grouped closely together and when close proximity is unnecessary.

2) Keep loop areas small where the current changes rapidly. Loop inductance is proportional to loop area. Inductive voltage spikes are proportional to inductance, i.e, V = Ldi/dt. For example, the loop from C1, through the T1 primary, Q1, R2, and back to the bottom end of C1 carries a current which undergoes a high rate of change. Reducing this loop area reduces noise on the input power lines. Other examples are the loops defined by each secondary winding and the corresponding output rectifiers. Cross regulation of the ±12-V outputs is worsened by the inductance of these loops. Conversely, the inductance of the loop defined by CR3, L2, and C7 is not critical. The parasitic inductance in series with an inductor is of little consequence.

3) Keep noise-sensitive nodes away from noise generators. The drain voltage of Q1 changes rapidly. If the trace between T1 (primary) and Q1 (drain) runs adjacent to the feedback input (pin 14) of U1, then noise is capacitively coupled into the feedback. The noise current is proportional to the parasitic capacitance by i = Cdv/dt. Injected noise currents are worse when the driving point impedance is high. Pins 1, 13, and 14 of the switchmode controller are such high-impedance nodes. Too much noise injection causes a random instability in the control loop.

Following these guidelines reduces headaches as well as costly design time. Using BiC/DMOS PWM controllers reduces component count and failure rates of dc/dc converters in distributed power systems.

References

1) Middlebrook, R.D., "Topics in Multiple-Loop Regulators and Current-Mode Programming," IEEE Power Electronics Specialists Conference, 985 Record, pp. 716-732 (IEEE Publication 85CH2117-0).

2) Hsu, et al., "Modelling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current-Programmed Mode," IEEE Power Electronics Specialist Conference, 1979 Record, pp. 284-301, (IEEE Publication 79CH1461-3 AES).

3) McLyman, Col. W. T., "Magnetic Core Selection for Transformers and Inductors," Marcel Dekker,1982.

Appendix A

Proper operation of the Si9110 requires that a programming resistor, R_{BIAS}, be connected from pin 1 to $-V_{IN}$, which is assumed here to be ground. This resistor programs internal current sources in the analog portion of the control circuitry. The value of the bias current depends upon two parameters, V_{CC} and R_{BIAS}, as shown in the circuit provided in Figure 1. The characteristic curve of the PMOS FET follows the familiar square law (I_D is proportional to V_{GS} squared). However, over the region of interest, between 5 µA and 50 µA, the curve can closely be approximated by a straight line, as shown in Figure 2. This line is defined by its slope (50 kΩ) and its point of intersection with the X-axis (3.5 V). The intersection of this curve with the load line defined by V_{CC} and R_{BIAS} determines the value of I_{BIAS}. The load line in Figure 2 identifies the conditions which are specified in the data sheet. When V_{CC} = 10 V and R_{BIAS} = 390 kΩ, I_{BIAS} = 15 µA.

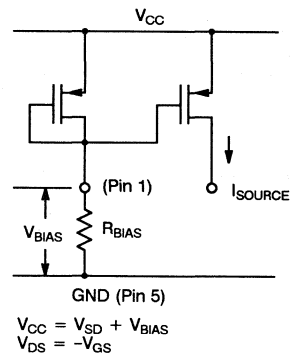


Figure 1. Internal Current Source Programming

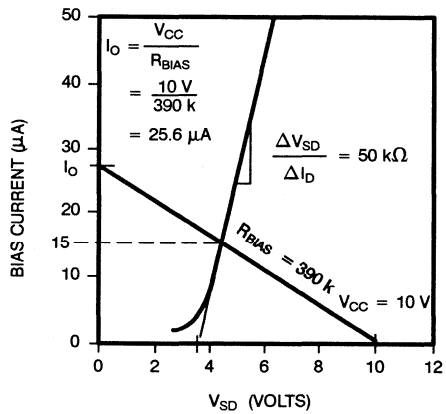


Figure 2. Programmable Current Regulator Characteristics

If the pre-regulator is used continuously, as in the forward converter example above, then V_{CC} has a nominal value of 8.5 V. The 1-MΩ bias resistor gives I_{BIAS} = 5 µA. This is the lowest value recommended. On the high end, not much performance improvement in terms of comparator speed is obtained for I_{BIAS} above 30 µA (see Figure 6).

Appendix B

The supply current requirements of PWM controller ICs are specified at one operating frequency, with no load being driven. In many cases, it may be useful for the circuit designer to determine the supply current requirements needed to drive a specific MOSFET at a given frequency. The Si9110 has been well characterized in this regard.

Equation 1 provides a quick calculation of the supply current drawn by the Si9110.

$$I_{CC} = 60\ \mu A + \left[1.5\ \mu A\ \frac{f_S}{1000}\right] + \left[30 \times I_{BIAS}\right] + \left[Q_g \times f_S\right] \qquad (1)$$

Each of the components has a straightforward explanation.

a. The voltage reference requires a constant current which is neither frequency nor load dependent. It has a typical value of 60 µA.

b. CMOS circuitry only uses power when a change in logic state occurs. Therefore, the quiescent current requirements of the oscillator and logic gates is proportional to the switching frequency. The proportionality constant is typically 1.5 µA per kHz.

c. The analog circuitry (error amplifier and comparators) utilizes constant-current sources which are programmed by the bias resistor connected from pin 1 to ground. Setting R_{BIAS} equal to 390 kΩ and V_{CC} = 10 V programs the bias current at 15 µA. At this current, the internally generated voltage reference levels (for undervoltage lockout, V_{REF}, and V_{CL}) have the best compensation over temperature. This is also the value at which the data sheet parameters are guaranteed.

d. The output drive current is typically the largest component of I_{CC}. The drive stage has been designed to minimize shoot-through current of the output inverter. Thus, the current requirement can be calculated as $I_{gate} = C_L V_{CC} f_S$. A MOSFET gate is a capacitive load, but a non-linear one. Therefore, MOSFET manufacturers specify the total gate charge required to turn a MOSFET on. In this case, $I_{CC} = Q_{g(on)} \times f_S$, where fs is the switching frequency.

For the forward converter example, the supply current should be

Voltage reference			60 µA
Oscillator and logic			
	(1.5 µA)/kHz x 100 kHz	=	150 µA
Analog circuitry	30 x 5 µA	=	150 µA
Gate drive	15 nC x 100 kHz	=	1500 µA
Total supply current		=	1860 µA

The measured value was 2.1 mA.

Appendix C

The gain of the error amplifier plus the feedback isolation circuit is

$$A_V = \left(\frac{R_9}{R_7}\right)(CTR)\left(\frac{R_{11}}{R_{10}}\right)\left(\frac{R_4}{R_{12}}\right)$$

$$= \left(\frac{5.1\ k\Omega}{1\ k\Omega}\right)(0.07)\left(\frac{47\ k\Omega}{1\ k\Omega}\right)\left(\frac{150\ k\Omega}{180\ k\Omega}\right) = 14$$

which is approximately equal to the gain of the non-isolated feedback circuit analyzed above.

The TL431C has a voltage reference with 2% accuracy equal to 2.5 V. R_7 and R_8 were both chosen to be 1 kΩ to establish a dc current much greater than the input bias current of U2, which is 4 µA. C_{10} causes the amplifier of U2 to behave as an integrator with a high dc gain, thus ensuring the accuracy of the output voltage. R_9 causes the gain of U2 to remain constant at R_9/R_7 above the crossover frequency, $1/(2\pi R_9 C_{10})$.

The minimum current transfer ratio (CTR) of U3 is 0.07. CTR is defined as the ratio of output current to anode current for the optical isolator. The small-signal variation of the LED current is equal to the output voltage of U2 divided by R_{10}. The output voltage of U3 is equal to the output current of U3 times R_{11}. Therefore, the gain from the output of U2 to the output of U3 is given by $CTR(R_{11}/R_{10})$. R_{11} was chosen to establish a dc operating current for U3 given approximately by

$$\frac{V_{REF}}{R_{11}} = \frac{4\ V}{47\ k\Omega} = 85\ \mu A$$

Likewise, R_{10} establishes the dc operating point for the LED at approximately 1 mA. R_9 and R_{12} are chosen last to achieve the desired overall gain.

Efficient ISDN Power Converters Using the Si9100

James Blanc

One of the latest technology revolutions, an integrated worldwide telecommunications network, will be accompanied by another advance in power conversion technology. The integrated services digital network (ISDN) will allow different forms of information (voice, computer data, video, facsimile, etc.) to be transmitted over the telephone network. The International Consultative Committee for Telephone and Telegraph (CCITT) has proposed standards for the interfaces required to implement ISDN. Although the standards have yet to be formally adopted, telecommunications companies are moving ahead with pilot test programs, and semiconductor makers are developing chip sets to build ISDN hardware. Every network terminator (NT), signal regenerator (RG), and terminal equipment (TE) unit used for the implementation of ISDN will require a power converter.[1]

A major requirement of these telecom applications (due to the need for emergency-mode operation from a high-impedance source) is high-efficiency energy conversion at fractional-watt power levels. Minimization of parts count, another key factor for the design of these power converters, is sought to simultaneously achieve low cost and high reliability.

BiC/DMOS integrated circuit technology is ideally suited for the power requirements of ISDN. The analog and digital logic functions needed for pulse-width modulation can be implemented in CMOS to minimize quiescent current to the controller. DMOS transistors provide high-voltage power switching with both very low dynamic and gate drive losses. Integration of the CMOS controller on the DMOS power device yields the best overall performance at the lowest cost and component count.

Design Objectives

While some differences exist between designs, there are several requirements in addition to efficiency which are common to ISDN power converter applications. These include:

- reliable start-up and operation from the high source impedance of telephone subscriber lines (U-interface only)
- current limiting to prevent failure of other network terminals when one power converter output is shorted (S-interface only)
- a free-running internal oscillator for start-up as well as independent operation, which can be synchronized to an external clock signal
- electromagnetic interference (EMI) filtering to limit conducted emissions during both start-up and normal operation, as well as during equipment connections and disconnections.

The Si9100 power IC facilitates compliance with these design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested. Measured efficiency was greater than 80% for a wide range of loads, and 60% efficiency was achieved with only a 15-mW load. Before describing the circuit concepts in detail, it is instructive to note the main features of the ISDN power-feeding concept which has been endorsed by the CCITT.

ISDN Power Feeding

Figure 1 is a block diagram of the ISDN basic access configuration. The two-wire transmission line defined at the U-interface provides a 192 k-bits-per-second (bps) digital data path which connects subscriber equipment to the local telephone exchange. Although ISDN permits many new services to be offered, the basic service of voice transmission remains a vital function. Therefore, the network power feeding from batteries in the local telephone exchange remains an essential part of modern telephone system planning. The network terminal (NT) connects the local loop, called the S-bus, to the U-interface at the customer's premises. ISDN-compatible terminals (TE1) communicate at a standard 64 k-bps rate over the four-wire S-bus. Non-ISDN-compatible terminal equipment (TE2), such as analog phones, must connect to the S-bus via a terminal adapter (TA).

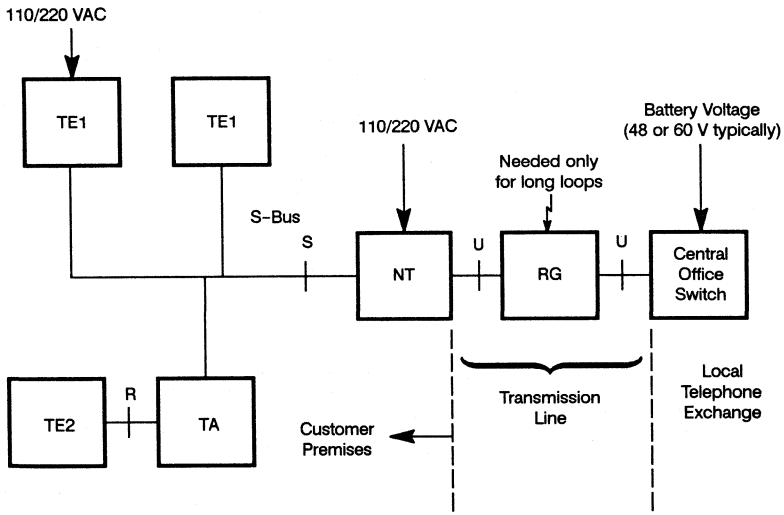


Figure 1. ISDN Basic Access Configuration

To minimize noise-coupling problems, the S-bus must be galvanically isolated from the two-wire U-interface. The CCITT recommendations call for an off-line power converter in the NT to supply 4 W at 40 V nominal to the S-bus during normal operation (for up to four telephones with full features). Other terminal equipment (e.g., fax terminals) would be fed solely from local ac power lines. In the event of a power outage, one telephone at the customer premises must be fed from the central office battery. This procedure is accomplished by reversing the voltage polarity on the S-bus. Non-priority terminals have a diode input which isolates them during emergency-mode operation. A single telephone terminal is fed via a full diode bridge, allowing it to operate during the emergency.

A signal regenerator may be required for long loops (U-interface). The Deutsche Bundespost (DBP) proposes to increase the feeding voltage from 60 V to 93 V to compensate for voltage drops on long lines requiring signal regeneration. The standard telephone line voltage used in many other parts of the world is 48 V. Whatever the voltage, the problem for power converters connected to telephone subscriber lines remains the same--they are fed from a high-impedance source.

Source Impedance Effects

The impedance of telephone subscriber lines limits the amount of power that can be supplied to the load. Referring to Figure 2, for a battery voltage, V_S, and line resistance, R_S, the maximum power to the converter is given by Equation 1, since the power limit occurs when source and load impedances are equal.

$$P_{MAX} = \frac{V_1^2}{R_e} = \frac{(V_S/2)^2}{R_e} = \frac{V_S^2}{4R_e} \qquad (1)$$

R_e is defined as the effective low-frequency input impedance of the power converter.

For a flyback converter, with waveforms as shown in Figure 3, the calculation of the low-frequency input impedance is straightforward. The coupled inductor is designed to ensure operation in the discontinuous conduction mode (DCM). This operation requires that the core flux be reset to zero during each cycle. The current is zero at turn-on and ramps up at a rate given by $di/dt = V_1/L_p$. The maximum value of the peak primary current, I_{pk}, is

$$I_{pk} = \frac{di}{dt}(t_{ON(MAX)}) = \frac{V_1}{L_p}\frac{T_S}{2} \qquad (2)$$

The 50% maximum duty ratio imposed by the Si9100 controller limits the "on" time of Q1 to one-half of the switching period. The average value of the current waveform in Figure 3 is the dc current in the inductor, L1. The current ripple in L1 is small, and the average inductor current, I_{DC}, during start-up is one-fourth the peak current value, as given by

$$I_{DC} = (I_{pk}/2)(D_{(MAX)}) = I_{pk}/4 \qquad (3)$$

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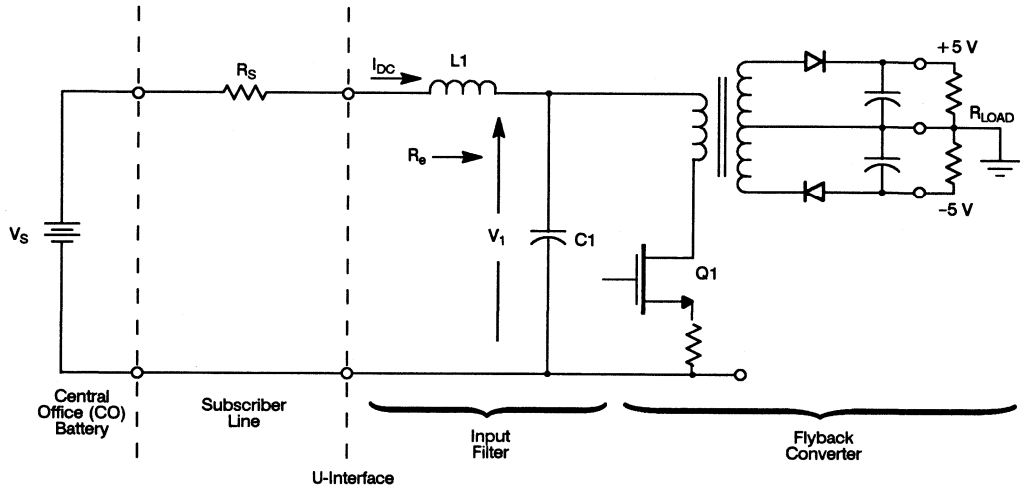

Figure 2. Power Converter with High Source Impedance

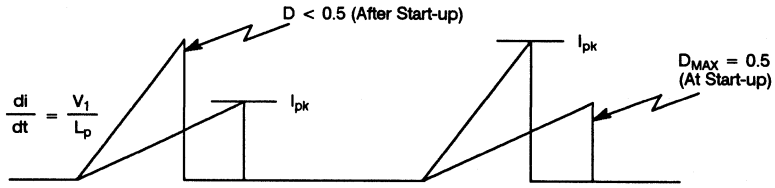

Figure 3. Primary Side Current Waveforms

Substituting this result into Equation 2 gives R_e in terms of the primary inductance, L_S, and switching frequency, f_S ($f_S = 1/T_S$).

$$R_e = \frac{V_1}{I_{DC}} = 8\,L_p f_S \qquad (4)$$

L_p effectively acts as a current limiter during start-up, thus eliminating the need for active current limiting circuitry. The value of L_p must be chosen between a minimum value, which sufficiently limits start-up current, and a maximum value, which permits the rated throughput power to the load. Assume, for example, the maximum load condition given in Table 1.[2] The input power to the converter is the output power divided by the efficiency.

$$P_{IN} = P_O/\eta = \frac{0.650}{0.80} = 0.813\ \text{W} \qquad (5)$$

Worst-case efficiency at maximum load is assumed to be equal to 80%. The input power to the converter is given by

$$P_{IN} = \tfrac{1}{2}\,L_p\,I_{pk}^2\,f_S \qquad (6)$$

As seen from Figure 3, if L_p is doubled, I_{pk} is reduced by half. Therefore, P_{IN} varies in inverse proportion to L_p. Referring again to Figure 1, the dc analysis of the input characteristics gives

$$V_1 = V_S - I_{DC}\,R_S \qquad (7)$$

Table 1. ISDN Power Requirements

Operating Mode	Load			Measured Efficiency
	+5 V Current	-5 V Current	Output Power	
Normal -- Active	100 mA	30 mA	650 mW	87%
Normal -- Power Down	11 mA	3 mA	70 mW	79%
Emergency -- Active	55 mA	9 mA	320 mW	88%
Emergency -- Power Down	3 mA	0 mA	15 mW	60%

Equations 2, 6, and 7 can be combined to give a quadratic equation which yields the maximum and minimum values for L_p. A graphical approach, however, gives the same answer and, at the same time, provides more insight into system behavior. After start-up has occurred, the power converter no longer presents a constant impedance at the input terminals. Instead, a constant power characteristic pertains, given by

$$P_{IN} = (V_1)\,(I_{DC}) = \text{constant} \qquad (8)$$

The demonstration flyback converter was designed to operate from a battery voltage of 48 V and a maximum line resistance of 600 Ω. The constant power curve for $(V_1)\,(I_{DC}) = 0.813$, with the load line defined by $V_S = 48$ V and $R_S = 600\ \Omega$, are plotted in Figure 4. The intersection of the load line with the constant power curve determines two operating points, A and B, which occur at (V_1, I_{DC}) = (14.6 V, 55.7 mA) and (33.4 V, 24.3 mA). If V_S is slowly increased from zero, V_s and I_{DC} increase along the line, whose slope is R_e, from the origin to the constant power curve. This analysis is an oversimplification since a step increase in voltage is more likely to occur at power-up. However, worst-case start-up conditions occur at maximum R_S, which guarantees that the input filter is heavily overdamped. Therefore, the increase in V_1 is monotonic, and the results of the simplified analysis are valid.

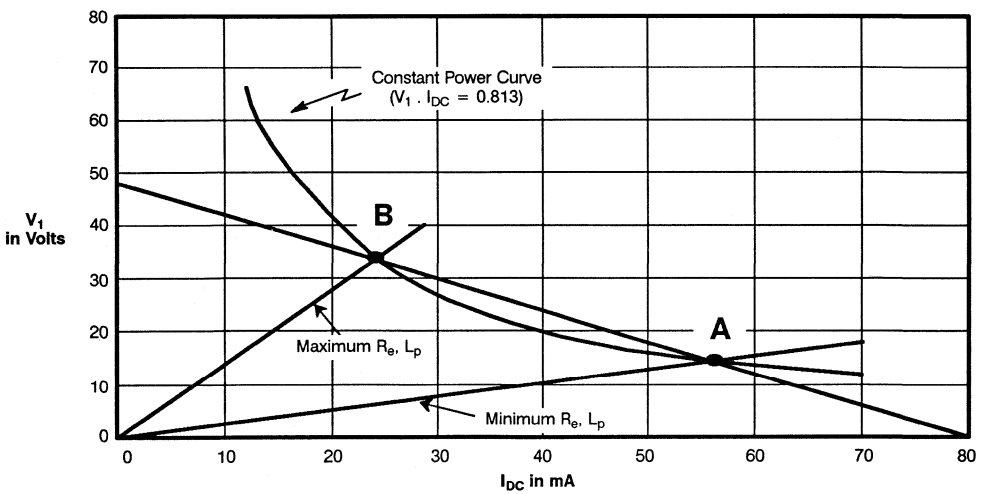

Figure 4. Flyback Converter Operating States

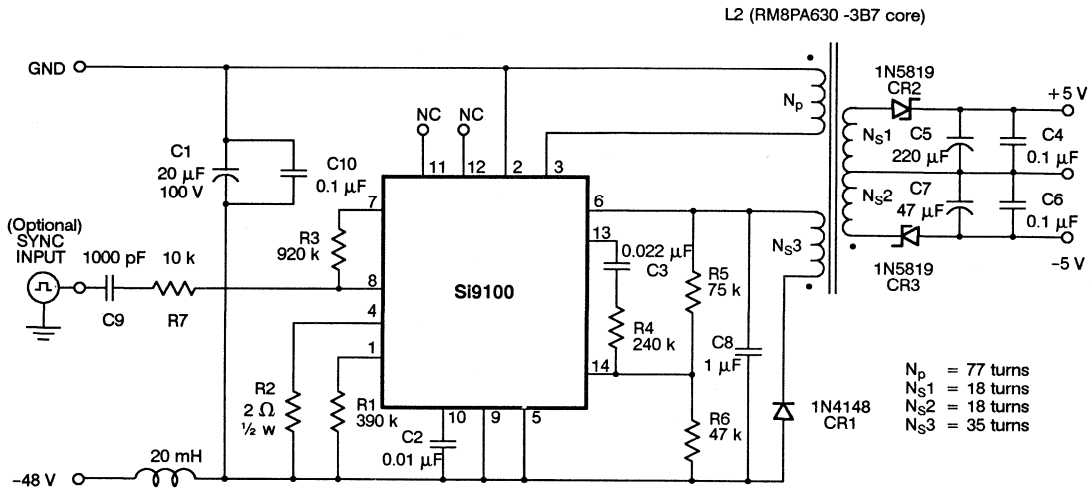

Figure 5. ISDN Flyback Converter

The lines from the origin to points A and B define the minimum and maximum values for R_e, and with Equation 4, also determine the limits for L_p.

$$R_{e(min)} = 14.6/0.0557 = 263\ \Omega$$
$$R_{e(max)} = 33.4/0.0243 = 1.37\ k\Omega$$

For a switching frequency design value equal to 20 kHz, Equation 4 gives

$$L_{p(min)} = 1.64\ mH$$
$$L_{p(max)} = 8.65\ mH$$

L_p may be chosen near the upper end of the permissible range for maximum start-up current limiting, or it may be chosen for maximum power transfer on a high-resistance line. Setting $R_e = R_S = 600\ \Omega$ for maximum power transfer gives

$$L_p = R_e/8\ f_S = \frac{600}{(8)\ (20{,}000)} = 3.75\ mH$$

The latter approach was chosen for the demonstration converter (see schematic in Figure 5). The Si9100 functional diagram is given in Figure 6 for reference.

Converter Performance

Measured efficiency data for the flyback converter is given in the last column of Table 1. Most notable is the 60% efficiency at a load of only 15 mW, which is allowed by the low quiescent current requirement of the CMOS control circuitry in the Si9100. Although power converters can operate at much higher frequencies, the dynamic losses incurred reduce the efficiency during the power-down state. The switching speed (30 ns typical) of the DMOS output transistor in the Si9100 permits operation above audible frequencies with very low dynamic and drive losses. Such performance cannot be achieved with bipolar transistors. A single resistor, R3, sets the oscillator frequency at approximately 34 kHz. A positive sync pulse (5 V amplitude and 0.5 µs pulse width) at 40 kHz was fed through R7 and C9 to pin 8 to demonstrate the principle of synchronization with an external clock. Typically, the free-running frequency should be set at 10 to 20% below the external clock frequency (note that the switching frequency is ½ of the oscillator frequency).

Start-up characteristics were verified by connecting a 600-Ω resistance from a dc power supply to the converter input terminals. Reliable start-up was demonstrated at maximum load for supply voltages as low as 44 V. With zero source resistance inserted in the line, the converter maintained regulation down to an input voltage of 23 V. In both cases, the maximum operating voltage is 70 V for the Si9100. The inductor, L1, was wound with 540 turns of #32 magnet wire on a #55206 molypermalloy powder core.

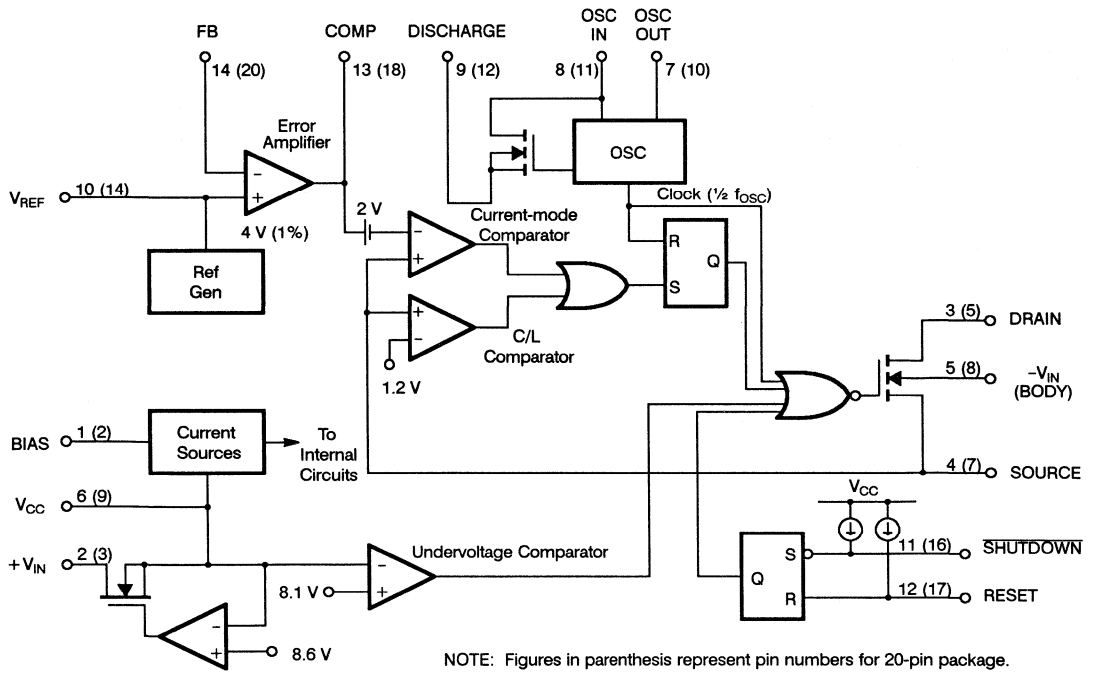

Figure 6. Si9100 Functional Diagram

The relatively high series resistance of this inductor (6 Ω) provides series damping of the input filter. This damping reduces peaking of the filter output impedance, preventing degradation of the control loop response at the filter resonant frequency when the supply is operated from a low-resistance source.

Measured ripple on both outputs was less than 50 mV peak to peak, and regulation was better than 5% over line and load. The -5-V output increases from -5.05 V to -5.75 V when totally unloaded.

The current-mode controller of the Si9100 provides fast current-limiting response in the event of a shorted output. With either output shorted to ground, the measured value of short-circuit current drawn at the converter input was 30 mA. Any output terminal can be shorted for an indefinite period with no resulting high stress condition on the Si9100. Normal operation resumes when the short circuit is removed.

The input filtering provided by L1 and C1 provides a calculated attenuation of 68 dB at the fundamental of the switching frequency. This allows compliance with FCC Class B and VDE-0871/B requirements; however, conformance testing to these specifications was not performed. Common-mode noise coupling is minimized by the Si9100 since the MOSFET drain is electrically isolated from the package case (a 14-pin DIP). Therefore, very little parasitic capacitance exists from drain to ground. Since the Si9100 places both the driver and MOSFET on the same chip, gate driver lead lengths are reduced from a few centimeters for discrete designs to a few hundred microns.

The 5-mA/μs dynamic current limit required during connection of equipment to the S-bus[3] is met by selecting a suitably high value, 20 mH, for L1. Since several ohms of series resistance is desired, a small wire gauge is used and the inductor is not prohibitively large. A smaller value may be chosen for L1 where the EMI requirements are less critical.

Summary

BiC/DMOS power IC technology is ideally suited for the requirements of low-power dc/dc converters, such as those required for the implementation of ISDN. A circuit design for an 85%-efficient power converter using the Si9100 SMARTPOWER IC has been presented here. Measured performance data is given, along with a graphical analysis method for ensuring reliable start-up when power is fed from a high-impedance source.

References

1. Rosenbaum, D. and K.H. Stolp. "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct.14-17, 1985, 505-512.
2. Sigloch, R. "Requirements for Small High Efficiency dc/dc Converters in Complex Communication Networks," IEEE INTELEC Conference Proceedings, Toronto, Canada, Oct 19-22, 1986, 197-202.
3. Krautkramer, W. and B. Schickling. "Remote Power Feeding of ISDN-Terminals at the Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct. 14-17, 1985, 513-519.

A 1-Watt Flyback Converter Using the Si9100

James Blanc

The Si9100 is a monolithic BiC/DMOS SMARTPOWER IC which combines high-efficiency CMOS logic, a high-voltage switching transistor and high-voltage pre-regulator on a single die. It is the first low-cost, high efficiency regulator designed to operate directly from unregulated high-voltage dc power sources in areas such as telecommunications and avionics. The primary application will be in feature phones and ISDN terminals to power the logic components without exceeding the load limits set by the telecommunications industry. Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduced parts count decreases system cost, improves reliability, and simplifies circuit design.

The flyback converter presented here uses the Si9100 to provide an isolated ±5 V supply rated at 1 W. Specifications for this supply are as follows:

Input Voltage ..... 15 to 70 V_{DC}

Maximum load ..... +5 V @ 167 mA,
-5 V @ 33 mA

Minimum load ..... +5 V @ 32 mA,
-5 V @ 8 mA
Regulation ..... ±5%
Maximum Ripple ..... 100 mV p-p
Switching Frequency .. 100 kHz
Efficiency ..... 80% min for 1 W load
75% min for 0.2 W load

A schematic for the flyback converter is found in Figure 1, with a parts list provided in Appendix B. However, before discussing the details of the power supply design, it is instructive to review the functions of the Si9100 integrated circuit.

Si9100 DESCRIPTION

As shown in the block diagram of Figure 2, the Si9100 combines an oscillator, pre-regulator/start-up circuit, precision voltage reference, error amplifier, current-mode controller, and a MOSFET switching transistor into one 14-pin dual-in-line package. Overcurrent protection, undervoltage lockout, and logic inputs for both latched and unlatched shutdown modes are also included.

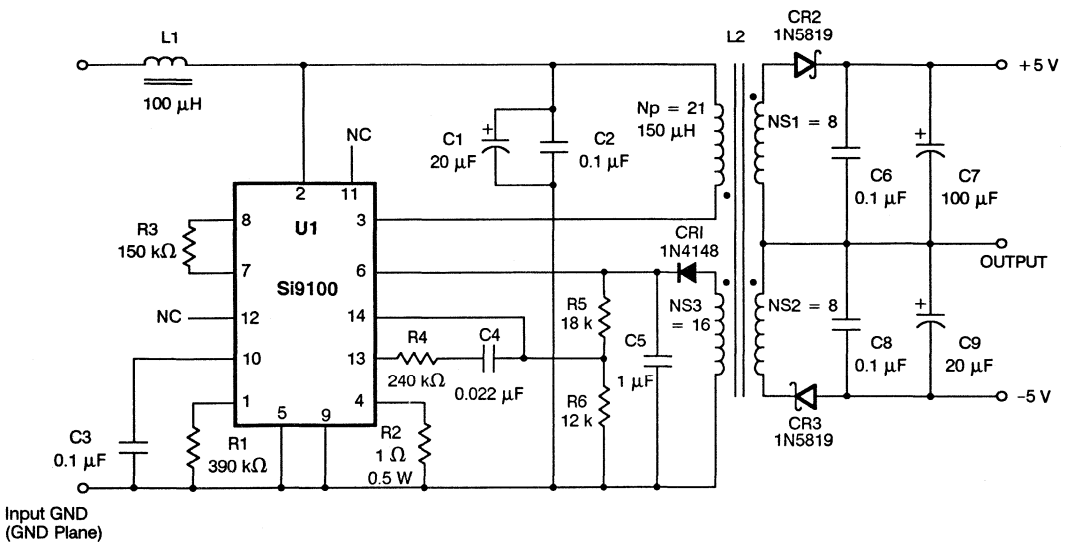

Figure 1. Schematic Diagram of the Si9100 Discontinuous Flyback Converter Circuit

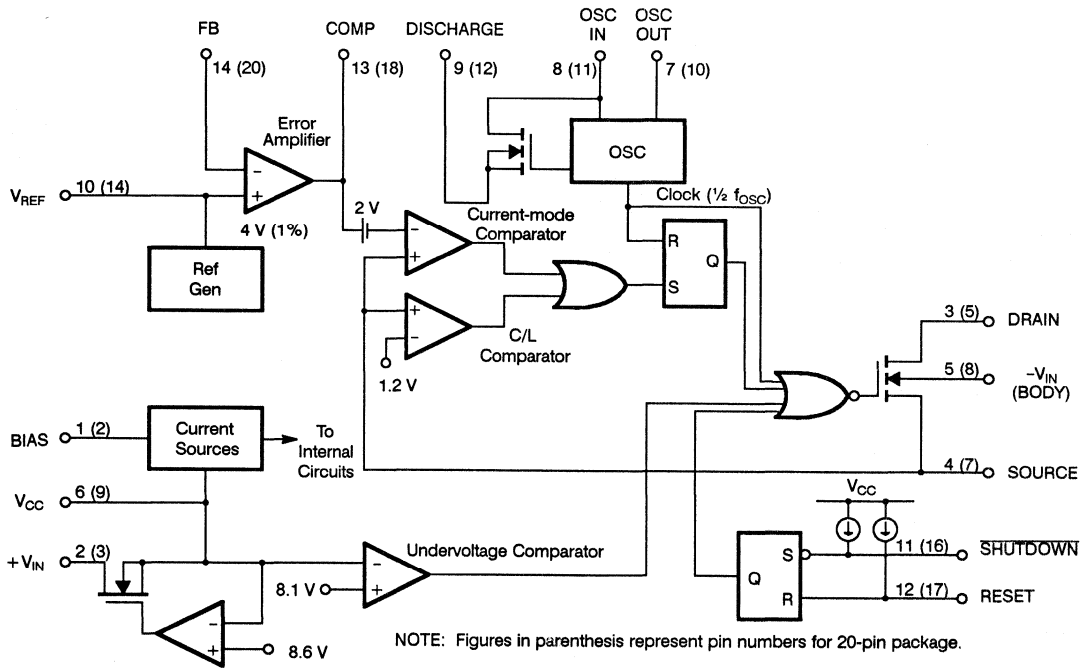

Figure 2. Si9100 Simplified Block Diagram

Start-up/Preregulator Circuit

A unique start-up/preregulator circuit, which is shown in Figure 3, permits the Si9100 to operate over a wide input voltage range (10 to 70 V). The input voltage for the device is connected between the $+V_{IN}$ (pin 2) and $-V_{IN}$ (pin 5) terminals. The high-voltage depletion-mode (normally ON) MOSFET acts as a current source during start-up, charging the capacitance at the V_{CC} terminal (pin 6) directly from the input source. When V_{CC} exceeds the 8.1 V undervoltage threshold, the output switch is enabled to provide well-defined start-up characteristics. V_{CC} is then regulated to 8.6 V by the pre-regulator circuit. If an external voltage source greater than 8.6 V is fed to the V_{CC} terminal, the depletion-mode MOSFET is shut off to reduce power drain from the input power source.

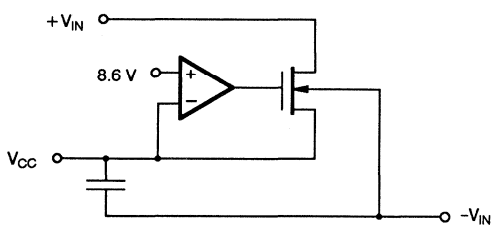

Figure 3. Schematic Diagram of the start-up section of the Si9100

Oscillator

The oscillator requires a single resistor to set its frequency. The requirements of flux reset in single-ended converters generally dictates a maximum duty cycle of 50%. With the oscillator frequency set at two times the desired switching frequency, a flip-flop divides the clock signal by two, and the logic disables the output during every other clock cycle.

MOSFET Switch

The MOSFET switching transistor has typical $r_{DS(ON)}$ and $V_{(BR)DSS}$ characteristics of 4 Ω and 180 V, respectively. Worst case specifications are 5 Ω and 150 V. The device is a lateral DMOS structure which has external connections for the DRAIN (pin 3) and SOURCE (pin 4). The body of the MOSFET is internally tied to the $-V_{IN}$ terminal, which must be connected to the most negative input potential in the circuit.

Error Amplifier

The error amplifier permits compensation of control loops for stable regulator operation. The amplifier uses PMOS input transistors to provide high input impedance (2 MΩ minimum), and is internally compensated for unity gain stability, with 1 MHz (typical) bandwidth and 60° phase margin.

Protection

In addition to the undervoltage lockout function already described, the Si9100 provides overcurrent protection and inputs for external logic control. With a sense resistor (typically 1 to 2 Ω) connected from the MOSFET source to the $-V_{IN}$ terminal, the voltage at pin 4 is proportional to the output current. When this voltage exceeds a 1.2 V reference the overcurrent comparator disables the output MOSFET. The shutdown delay is typically 100 ns (200 ns maximum).

Logic inputs $\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) permit the use of latched or unlatched shutdown modes. Internal current source pull-ups normally hold both logic pins high. If the $\overline{\text{SHUTDOWN}}$ pin is pulled low while the RESET is high, then the output switch will be disabled until the $\overline{\text{SHUTDOWN}}$ pin is again allowed to go high. This is the unlatched shutdown mode. If, however, the RESET pin is pulled low while the $\overline{\text{SHUTDOWN}}$ pin is also pulled low, then the converter will be latched off until RESET goes high again.

FLYBACK CONVERTER OPERATION

Start-up

Applying input voltage to the circuit initiates charging of capacitor, C_1, through the filter inductor, L_1. The depletion-mode MOSFET, as described above, supplies current to capacitor C_5 through the V_{CC} terminal of the IC. When V_{CC} reaches the undervoltage threshold (8.1 V), then transistor switching begins. The 4 V reference and the voltage divider ratio formed by R_5 and R_6 cause the feedback winding, N_{S3}, to be regulated to +10 V. After start-up is complete the feedback voltage trips the comparator to turn off the pre-regulator circuit, and the Si9100 derives its bias power from the feedback winding. The power saved by this bootstrap technique is equal to the product of the IC supply current times the difference between V_{IN} and V_{FB}:

Power Saved = (600 μA) (48 V - 10 V) = 23 mW

While this is not a great deal of power, it does represent 2.3% of the output for a 1 W supply. Integrated Services Digital Network (ISDN) applications require such techniques for bias power minimization in order to meet emergency-mode limits for the power-down state.

Flyback Operation

Flyback converter operation is illustrated by the basic waveforms shown in Figure 4. When the MOSFET switch is turned on, current will ramp up in the primary at a rate given by:

$$\frac{di}{dt} = \frac{V}{L} = \frac{I_{pk}}{t_{ON}}$$

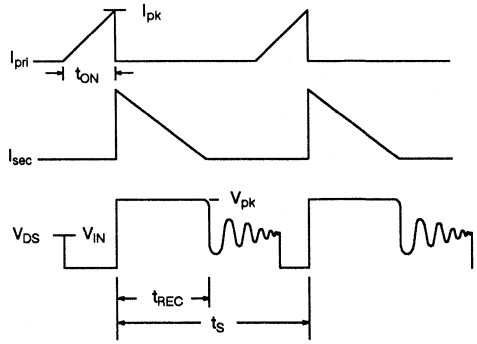

Figure 4. Flyback converter waveforms

Stored energy, given by ½ L_P I_{pk}^2, is present in L_2 at the time the MOSFET is switched off. This energy is released to the secondary windings, N_{S1} through N_{S3}, during the off time, as shown by the total secondary current, I_{sec}, in Figure 4. This is the flyback principle in its simplest terms. A transformer is designed to transfer energy directly from the primary to the secondary, with as little stored energy as possible. A flyback inductor receives energy during one interval of the switching cycle, then releases this stored energy at a later interval of the switching cycle.

During the time that the secondaries are conducting, shown as t_{REC}, the magnetic flux recovers, or "resets" to zero, and the MOSFET must block the sum of the reflected voltage from the secondary and the input voltage. This requires a worst case blocking voltage of:

$$V_{pk} = V_{IN} + \frac{N_P}{N_{S1}} (V_O + V_D)$$

$$= 70 + \frac{21}{8} (5.0 + 0.5) = 85\ V$$

A leakage inductance spike appears at the leading edge of the V_{DS} waveform. The spike is less than the 150 V minimum $V_{(BR)DSS}$, and no snubber network is required. Since the flux is reset to zero before the end of each switching cycle, current flow through the secondary is discontinuous. Consequently, this circuit is called a discontinuous-conduction-mode (DCM) flyback converter.

Regulator Control Loop

The function of the regulator control loop is to maintain the output voltages constant as either the input line voltage or load current vary. These are termed "line regulation" and "load regulation", respectively.

A sense winding has been chosen to close the regulator loop and provide output isolation. Since the secondary windings are coupled on a common core, the volts/turn ratio is the same for N_{S1}, N_{S2} and N_{S3}. The resulting secondary voltages will track each other quite closely. There is, however, some degradation in load regulation due to leakage (uncoupled) inductance between the ±5 V output windings and the sense winding. This effect becomes progressively worse as the switching frequency is increased. The coupled inductor used here has been designed for good coupling between output and sense windings in order to maintain better than 5% regulation over the 0.2 W to 1 W load range. Design details for the coupled inductor are included in Appendix A.

To analyze the system closed loop response, begin by reflecting the filter capacitance and load resistance from each output winding to the feedback winding.

$$C_{eff} = C_5 + \left(\frac{N_{S1}}{N_{S3}}\right)^2 \bullet \left(C_7 + C_9\right)$$

$$= 1\ \mu F + \left(\frac{8}{16}\right)^2 (100\ \mu F + 20\ \mu F) = 31\ \mu F$$

The effective load resistance, R_{eff}, can be found by assuming that the entire 1 W load is connected across the sense winding output:

$$R_{eff} = \frac{V_S^2}{P_O} = \frac{(10\ V)^2}{1\ W} = 100\ \Omega$$

The effective load impedance is determined at low frequency by the 100 Ω resistance and at high frequency by the capacitive reactance given by $X_C = 1/\omega C_{eff}$. The control-to-output transfer function thus has a pole at:

$$f_p = \frac{1}{2\pi\ R_{eff}\ C_{eff}} = \frac{1}{2\pi\ (100)\ (31 \bullet 10^{-6})} = 51\ Hz$$

To calculate the low frequency gain of the power stage, assume a 1 mV change in the error voltage, V_e, at the output of the error amplifier, and calculate the voltage change, ΔV_S, which results at the feedback winding. Then combine the power stage gain with the error amplifier gain (including the voltage divider) to yield the total loop response. Assume for these calculations that the converter efficiency remains constant at 83.33%.

$$P_{IN} = \frac{P_O}{\eta} = \frac{1\ W}{0.8333} = 1.2\ W$$

The power input to the converter is the product of the stored inductive energy times the switching frequency.

$$P_{IN} = \tfrac{1}{2}\ L_p\ (I_{pk})^2 \bullet f_s$$

Rearranging to solve for I_{pk} gives:

$$I_{pk} = \sqrt{\frac{2\ P_{IN}}{L_P \bullet f_s}} = \sqrt{\frac{2\ (1.2)}{(150\ \mu H)\ 10^5}} = 0.4\ A$$

Since the current sense resistor, R_2, equals 1 Ω, a 1 mV change in the error voltage (at pin 13) will result in a 1 mA change in the peak inductor current, i.e., $\Delta I_{pk} = \Delta V_e$. A 1 mA increase in I_{pk} causes P_{IN} to increase to:

$$P_{IN} = \tfrac{1}{2}\ L_p\ (I_{pk} + \Delta I_{pk})^2 \bullet f_s =$$

$$\tfrac{1}{2} \bullet 150 \bullet 10^{-6}\ (0.400 + 0.001)^2 \bullet 10^5 = 1.206\ W$$

Assuming efficiency remains constant,

$$P_O = (0.833) \bullet P_{IN} = 1.005\ W$$

This translates to an increase in the sense voltage to:

$$V_S = \sqrt{P_O \bullet R_{eff}} = \sqrt{(100 \bullet 1.005)} = 10.025\ V$$

The gain is given by:

$$\frac{\Delta V_S}{\Delta V_e} = \frac{10.025\ V - 10\ V}{1\ mV} = 25$$

At full load the low frequency gain of the power stage is 25 (28 dB), with a single pole in the transfer function at 51 Hz. Performing a similar calculation at the 20% load condition yields a gain of 56 (35 dB) with a pole at 10 Hz. There will also be a zero in the transfer function at approximately 30 kHz due to capacitor ESR.

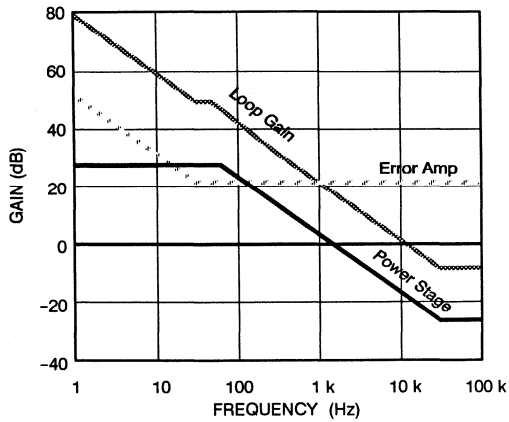

Figure 5. Loop gain at 100% load

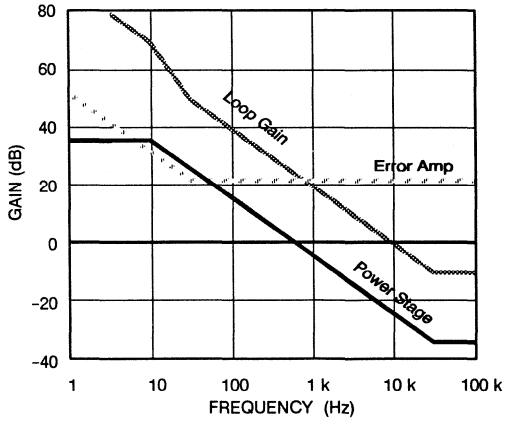

Figure 6. Loop gain at 20% load

The solid line in Figure 5 represents the transfer function of the converter power stage at full load. The corresponding curve at a 20% load is shown in Figure 6. To complete the analysis of the control loop requires accounting for the resistive voltage divider and the error amplifier. The resistor R_6 sets the dc bias condition, but does not enter into the samll signal analysis.

At high frequencies the gain is R_4/R_5, with a zero occurring in the transfer function at

$$f_z = \frac{1}{2\pi\ (240\ k\Omega)\ (0.022\ \mu F)} = 30\ Hz$$

The error amplifier response is shown in Figures 5 and 6 as dashed lines. The error amplifier response times the power stage gain gives the total loop gain, which is shown as the gray line for full load in Figure 5 and light load in Figure 6. Actual measurements of loop gain and phase yielded a loop bandwidth of 14 kHz with 68 degrees phase margin. Figure 7 shows the response of the +5 V output as the load is stepped between 20% and 100% of full load. Response time is under 200 µs with no overshoot.

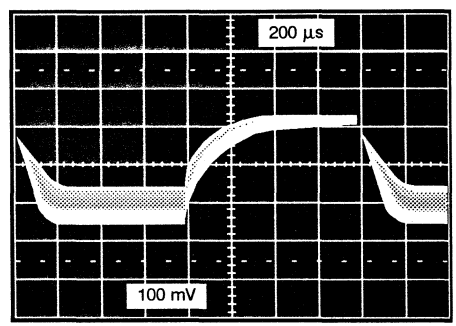

Figure 7. Step load response

Table I. ISDN Power Requirements

Operating Mode	Maximum Input Power to TE	Efficiency Target
Normal-active	900 mW	70%
Normal-power down	100 mW	60%
Emergency-active	400 mW	70%
Emergency-power down	25 mW	40%

ISDN APPLICATIONS

Integrated Services Digital Network (ISDN) poses some unique problems to telecom systems design engineers. Standards proposed by the International Telephone and Telegraph Consultative Committee (CCITT) recommend that input power to ISDN terminal equipment (TE) meet the limits outlined in Table I[1].

The 25 mW limit during emergency power-down mode operation may be especially troublesome[2]. In order to supply 10 mW to the TE for such functions as memory back-up, total converter losses must be less than 15 mW. Under such light load conditions the major power loss is in the PWM controller. Only controllers implemented in CMOS can presently be expected to meet this requirement.

Although the converter circuit of Figure 1 was not designed specifically for use in ISDN terminals, with some modifications it can be used in these applications. Since CMOS logic circuits consume power only during switching transitions, the first modification which is recommended is to decrease the switching frequency. The coupled inductor, L_2, can be operated at 40 to 50 kHz (change R_3 from 150 kΩ to 390 kΩ) without a redesign. Decreasing the frequency further requires a larger core size.

A second circuit modification which is recommended is to increase the resistances used in the voltage divider network (R_5 and R_6). The values used in the 1 W converter will dissipate $(10)^2/(18\,k\Omega + 12\,k\Omega) = 3.33$ mW. This loss is negligible for the 1 W converter, but it is nearly one fourth of the budgeted power loss for the ISDN supply during the emergency power-down state. Setting R_5 = 51.1 kΩ and R_6 = 34.0 kΩ reduces the voltage divider dissipation to 1.2 mW. With these two minor changes the flyback converter meets the efficiency specifications of Table I. Figure 8 illustrates the efficiency improvement at light load levels which results from the circuit changes outlined above.

Other Si9100 Applications Circuits

The Si9100 has been called a "One Watt High-Voltage Switchmode Regulator" in order to describe its most appropriate type of application--low power converters. The device is not, however, limited to 1 W designs. Figure 9 shows the maximum achievable output power as a function of minimum input voltage for several types of converters, two of which are discussed below.

CCM Flyback Converter

By redesigning the magnetics for continuous conduction, the flyback circuit of Figure 1 can be made to provide 3 W of output power. Operation in the continuous conduction mode (CCM) introduces a right-half-plane (RHP) zero into the control-to-output transfer function of the power stage. The RHP zero incurs a phase lag without the corresponding gain rolloff caused by left-half-plane poles, and lead compensation cannot be used. Instead, the gain must be rolled off to unity (0 dB) below the RHP zero frequency. The continuous-mode flyback will, therefore, have a slower dynamic response than the DCM flyback. Also, to maintain the same output ripple for the 3 W converter, it is necessary to increase the size of the output filter capacitors.

Forward Converter

Forward converters are not normally used for power supplies rated under 50 W, due to the additional cost of the output filter chokes. However, for 2 to 4 W converter applications requiring ultra-low ripple, the cost of the additional inductor may be warranted. One such application is low power instrumentation for avionics.

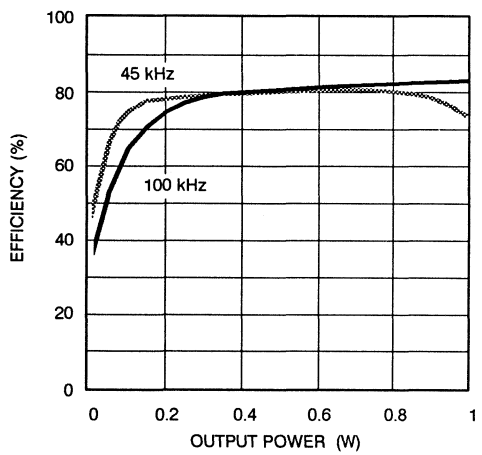

Figure 8. Efficiency vs. load curves for the flyback converter

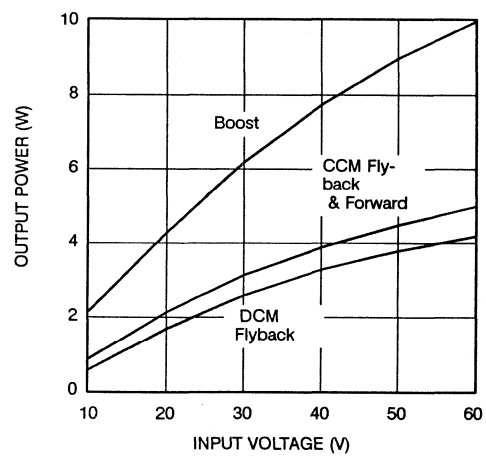

Figure 9. Maximum output power vs. minimum input voltage

The forward converter of Figure 10 was designed to operate from 28 V aircraft power (MIL-STD-704D) to provide 2.5 W at 80% efficiency. A single core with multiple windings has been used to decrease cost and board space required for the output filter inductors. The input voltage range is 18 to 32 V_{DC}; regulation is 5%; and the switching frequency is 100 kHz. Measured peak-to-peak voltage ripple was 8 mV for the +15 V output, 4 mV for the −15 V output, and 13 mV for the +5 V output, at maximum load.

Toroidal cores were used for both the transformer and the coupled output inductor to achieve very low leakage inductance. The transformer winding data is as follows:

Core - Ferroxcube #768T188-3C8

Windings - N1 = 31 turns (AWG26)
N2 = 31 turns (AWG34)
N3 = 22 turns (AWG32)
N4 = 64 turns (AWG32)
N5 = 43 turns (AWG34)

The primary and clamp windings are placed on the core first, wound bifilar to minimize leakage inductance. The +5 V output is wound next, followed by the ±15 V outputs wound bifilar. The 10 V winding was placed on the outside. Each winding is spread over the entire circumference of the toroidal core for optimum magnetic coupling.

Coupled inductors must have the same turns ratios as the transformer secondaries or high circulating currents result in very high output ripple. The coupled inductor, L_2, is a molypermalloy powder (MPP) toroid (Magnetics #55120) with three times the number of turns as each of the T1 secondaries.The inductor winding data is as follows:

+5 V - 66 turns (AWG30)
+15 V - 192 turns (AWG30)
−15 V - 192 turns (AWG34)
+10 V - 129 turns (AWG34)

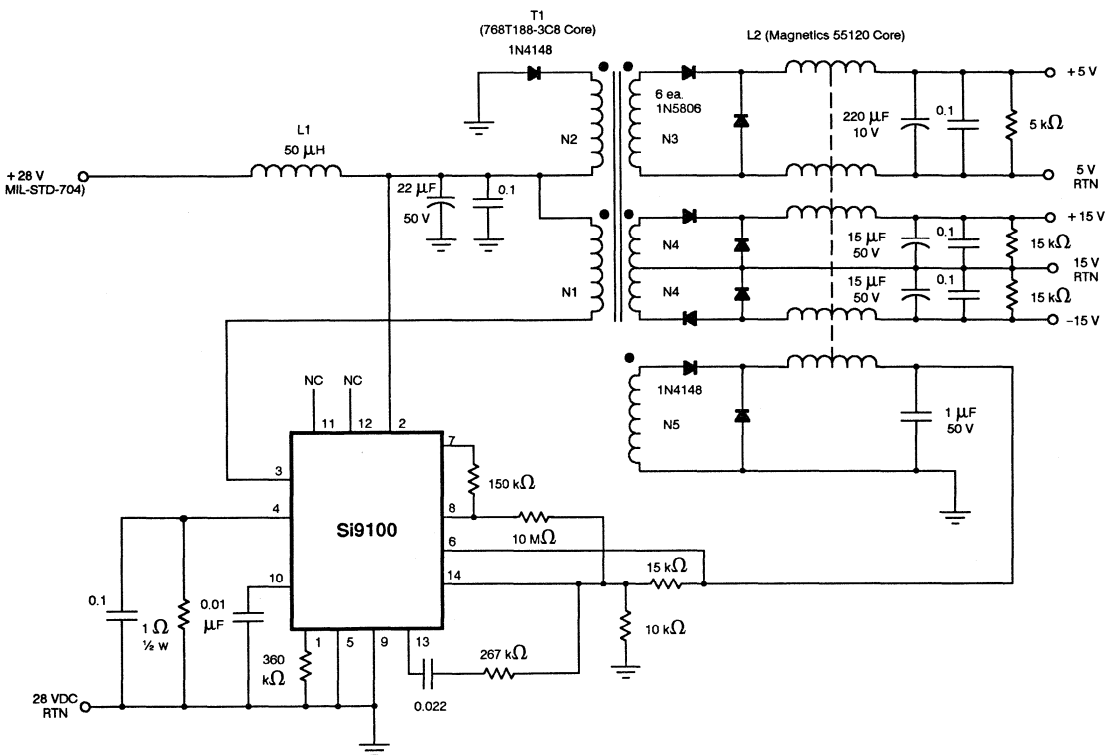

Figure 10. 2.5 W forward converter using the Si9100

It should be mentioned here that MIL-STD-461 EMI testing was not performed for this supply. To meet CE03 and CS01 limits, some input filter redesign is required. Although current-mode control exhibits excellent audio-susceptibility performance, it is still necessary to damp the input filter to reduce peaking of its output impedance at the resonant frequency (Reference 3 provides useful design information regarding these requirements).

References

1) Rosenbaum, D. and Stolp, K. H., "The Feeding Conception of the ISDN Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17, 1985, pp. 505-512.

2) Krautkramer, W. and Schickling, B., "Remote Power Feeding of ISDN Terminals at the Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17,1985, pp. 513-519.

3) Middlebrook, R. D., "Input Filter Considerations in Design and Application of Switching Regulators," IEEE Industry Applications Society Annual Meeting, Oct. 11-14, 1976.

APPENDIX A
FLYBACK INDUCTOR DESIGN

Inductance Calculation

The first step is to calculate the maximum primary inductance for discontinuous conduction at maximum load. Input power to the coupled inductor is approximately:

$$P_{IN} = \frac{1\ W}{0.8} = 1.25\ W \qquad (1)$$

Input power is also equal to the product of the stored energy in the magnetic field times the switching frequency:

$$P_{IN} = \tfrac{1}{2} L_P (I_{pk})^2 \cdot f_s \qquad (2)$$

The minimum primary current slope occurs at the minimum input voltage condition.

$$\left.\frac{di}{dt}\right|_{MIN} = \frac{V_{IN(MIN)}}{L_{P(MAX)}}$$

If a maximum duty ratio of 0.45 is assumed, then the minimum current peak is given by:

$$I_{pk} \leq \left.\frac{di}{dt}\right|_{MIN} \cdot 0.45\ T_S$$

or

$$I_{pk} \leq \frac{V_{IN(MIN)}}{L_{P(MAX)}} \cdot 0.45\ T_S \qquad (3)$$

Combining equations 2 and 3 gives:

$$P_{IN(MAX)} = \tfrac{1}{2} L_{P(MAX)} I_{pk(MIN)}^2 \cdot f_s$$

$$= \tfrac{1}{2} L_{P(MAX)} \left(\frac{V_{IN(MIN)}}{L_{P(MAX)}}\right)^2 \left(0.45\ T_S\right)^2 f_s$$

$$= \tfrac{1}{2} \frac{V_{IN(MIN)}^2}{L_{P(MAX)}} \cdot (0.45\ T_S)^2 f_s$$

$$\therefore L_{P(MAX)} = \tfrac{1}{2} \frac{V_{IN(MIN)}^2}{P_{IN(MAX)}} \cdot (0.45\ T_S)^2 f_s$$

$$= \tfrac{1}{2} \frac{(15)^2}{1.25} \cdot (0.45\ T_S)^2\ 10^5 = 182\ \mu H$$

To allow for component tolerances choose a nominal primary inductance of 150 µH. Equation 2 then gives $I_{pk} \approx 0.4$ A.

Core Selection

The area product method was used to determine the inductor core size. Refer to "Magnetic Core Selection for Transformers and Inductors" by McLyman, for more information on magnetics design methods (Marcel Dekker, Inc., 1982).

APPENDIX A (Cont'd)

$$A_P = \left(\frac{2\ E \bullet 10^4}{B_m \bullet K_u \bullet K_j} \right)^{1.14}$$

where:

E = Core energy storage requirement
B_m = Maximum flux density
K_u = Window utilization factor
K_j = Current density coefficient

$$E = \tfrac{1}{2} L_P I_{pk}^2$$

Let B_m = 1500, gauss = 0.15 tesla, and K_u = 0.10

$$A_P = \left(\frac{2 \bullet \tfrac{1}{2} \bullet 150 \bullet 10^{-6} (0.4)^2\ 10^4}{0.15\ (0.10)\ (433)} \right)^{1.14}$$

$$= 0.0233\ cm^4$$

Since the empirical equation given above applies for the area product of simple one-winding inductors, multiply by 2 for a coupled inductor. All of the secondaries combined will handle the same energy as the primary, and can therefore be allotted equal portions of the window area. The area product requirement is thus:

$$A_P = 2 \bullet 0.0233\ cm^4 = 0.0466\ cm^4$$

The EP-13 core has an area product of 0.049 cm^4, which meets this requirement. Also, this EP core can be tube-loaded for automatic insertion in high volume manufacturing applications, and is available from multiple sources (Siemens, TDK, and Amperex Ferroxcube).

Core A_L Value Determination

The number of primary turns is found from:

$$L = \frac{N_P \Phi}{I_{pk}} = \frac{N_P B_m A_C}{I_{pk}}$$

Limiting the peak flux density to 0.15 Tesla gives:

$$N_P = \frac{L_P I_{pk}}{B_m A_C} = \frac{(150 \bullet 10^{-6})\ (0.4) \bullet 10^4}{(0.15)\ (0.195\ cm^2)}$$

$$= 20.5\ turns \simeq 21\ turns$$

This gives the following value for A_L:

$$A_L = \left(\frac{1000}{21} \right)^2 (150 \bullet 10^{-6}) = 340\ mH\ per\ 1000\ turns$$

Secondary Turns Calculation

The core flux is reset to zero during the off time for each switching cycle. To guarantee discontinuous conduction mode at the maximum load condition, it is necessary to limit the inductance of the secondary windings to some maximum value. Worst case conditions occur at the maximum switching frequency (110 kHz) and maximum A_L value (374 mH/1000 turns for 10 % tolerance). The voltage across N_{S1} during the diode conduction interval is $V_O + V_D = 5.0 + 0.5 = 5.5$ V, and the negative current slope is

$$\frac{di}{dt} = \frac{I_{S1}}{t_{REC}} = \frac{V_O + V_D}{L_{S1}}$$

where I_{S1} is the peak current in the N_{S1} winding, t_{REC} is the conduction time of CR2, and L_{S1} is the inductance of N_{S1}. The rectifier conduction duty ratio is defined as:

$$d_r = \frac{t_{REC}}{T_S}$$

The load current is related to the peak secondary current and duty ratio by the equation:

$$I_{S1} = \frac{2 \bullet I_O}{d_r}$$

Combining these equations solves for the rectifier conduction duty ratio in terms of load current, inductance, and output voltage.

$$d_r = \sqrt{\frac{2 \bullet I_O \bullet L_{S1}}{(V_O + V_D) \bullet T_S}}$$

Setting the duty ratio < 0.45 gives:

$$d_r = \sqrt{\frac{2\ (0.167) \bullet L_{S1}}{5.5\ (9.09)\ 10^{-6}}} \leq 0.45$$

9

Therefore, $L_{S1} < 30.3\ \mu H$. Since $AL_{(MAX)} = 374$ mH/1000 turns,

$$L_{S1} = \left(\frac{N_{S1}}{1000}\right)^2 \cdot (0.374) \leq 30.3\ \mu H$$

$$\therefore\ N_{S1} \leq 9 \text{ turns}$$

Use $N_{S1} = N_{S2} = 8$ turns:

$$N_{S3} = (10\ V + 0.7\ V)\ \frac{N_{S1}}{5.5\ V}$$

$$= 15.6 \text{ turns} \simeq 16 \text{ turns}$$

Winding Order

The primary winding (1-2) is placed first over the bobbin using one strand of AWG31 magnet wire (21 turns). The highest current secondary (3-4) is wound over the primary using two strands of AWG31 (8 turns). The 10 V sense winding (7-8) is put down next, using one strand of AWG36 (16 turns). The −5 V output (5-6) is wound last using one strand of AWG31 wire (8 turns).

APPENDIX B
Si9100 FLYBACK CONVERTER PARTS LIST

U1	Si9100
L1	Inductor, 100 µH @ 75 mA dc
L2	Coupled Inductor, GFS Mfg. # 85-787-4*
C1	20 µF, 100 V, Aluminum Electrolytic, Sprague # 30D + TE1409
C2, C3, C6, C8	0.1 µF ceramic
C4	0.022 µF ceramic
C7	100 µF, 10 V, tantalum, Sprague # 196D107X9010P
C9	20 µF, 10 V, tantalum, Sprague # 196D226X9010J
C5	1 µF, 50 V, WIMA MKS2
CR1	1N4148
CR2, CR3	1N5819, Schottky rectifier
R1	390 kΩ, ¼ W Carbon
R2	1 Ω, ½ W Carbon
R3	150 kΩ, ¼ W Carbon
R4	240 kΩ, ¼ W Carbon
R5	18 kΩ, ¼ W Carbon
R6	12 kΩ, ¼ W Carbon

* GFS Manufacturing Company, 21 Crosby Road, Dover, NH, USA 03820-1409

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